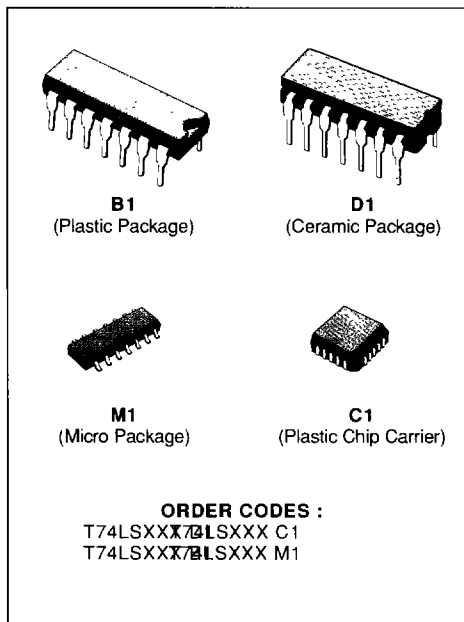
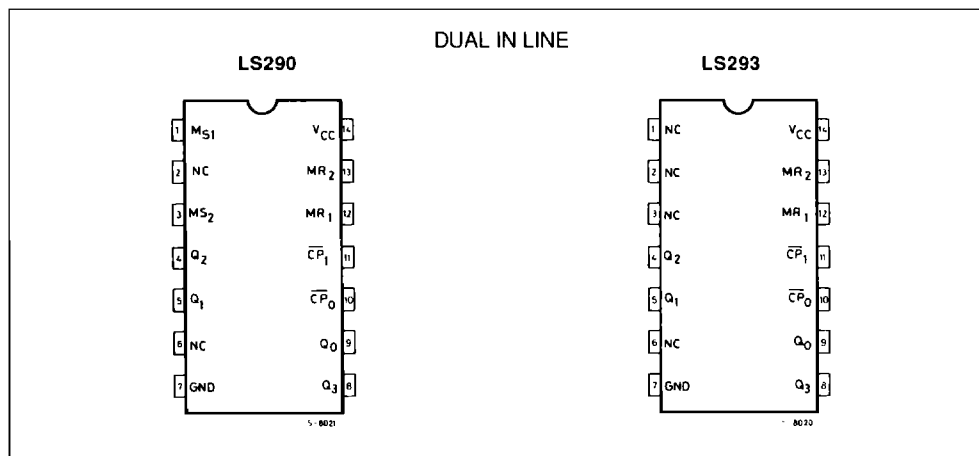


LS290-DECADE COUNTER
LS293-4-BIT BINARY COUNTER

- CORNER POWER PIN VERSION OF THE LS90 AND LS93
- LOW POWER CONSUMPTION... TYPICALLY 45mW
- HIGH COUNT RATES... TYPICALLY 50MHZ
- CHOICE OF COUNTING MODES... BCD, BI-QUINARY, BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

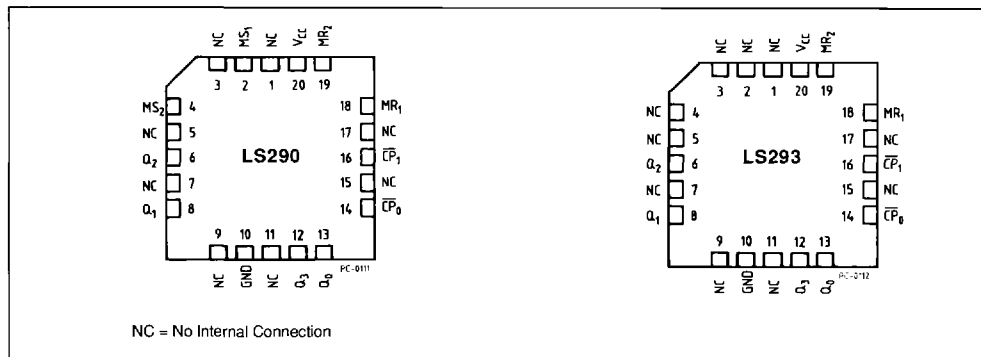
The T74LS290 and T74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divided-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to \overline{CP}) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).


PIN CONNECTION (top view)


PIN NAMES

\overline{CP}_0	CLOCK (active LOW going edge) INPUT TO + 2 SECTION
\overline{CP}_1	CLOCK (active LOW going edge) INPUT TO + 5 SECTION (LS290)
\overline{CP}_1	CLOCK (active LOW going edge) INPUT TO + 8 SECTION (LS293)
MR ₁ , MR ₂	MASTER RESET (clear) INPUTS
MR ₁ , MR ₂	MASTER RESET (preset-9 LS290) INPUTS
Q ₀	OUTPUT FROM - 2 SECTION
Q ₁ , Q ₂ , Q ₃	OUTPUTS FROM - 5 & - 8 SECTIONS

CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	Input Voltage, for \overline{CP}	- 0.5 to 5.5	V
V _O	Output Voltage, Applied to Output	- 0.5 to 10	V
I _I	Input Current, into Inputs	- 30 to 5	mA
I _O	Output Current, into Outputs	50	mA

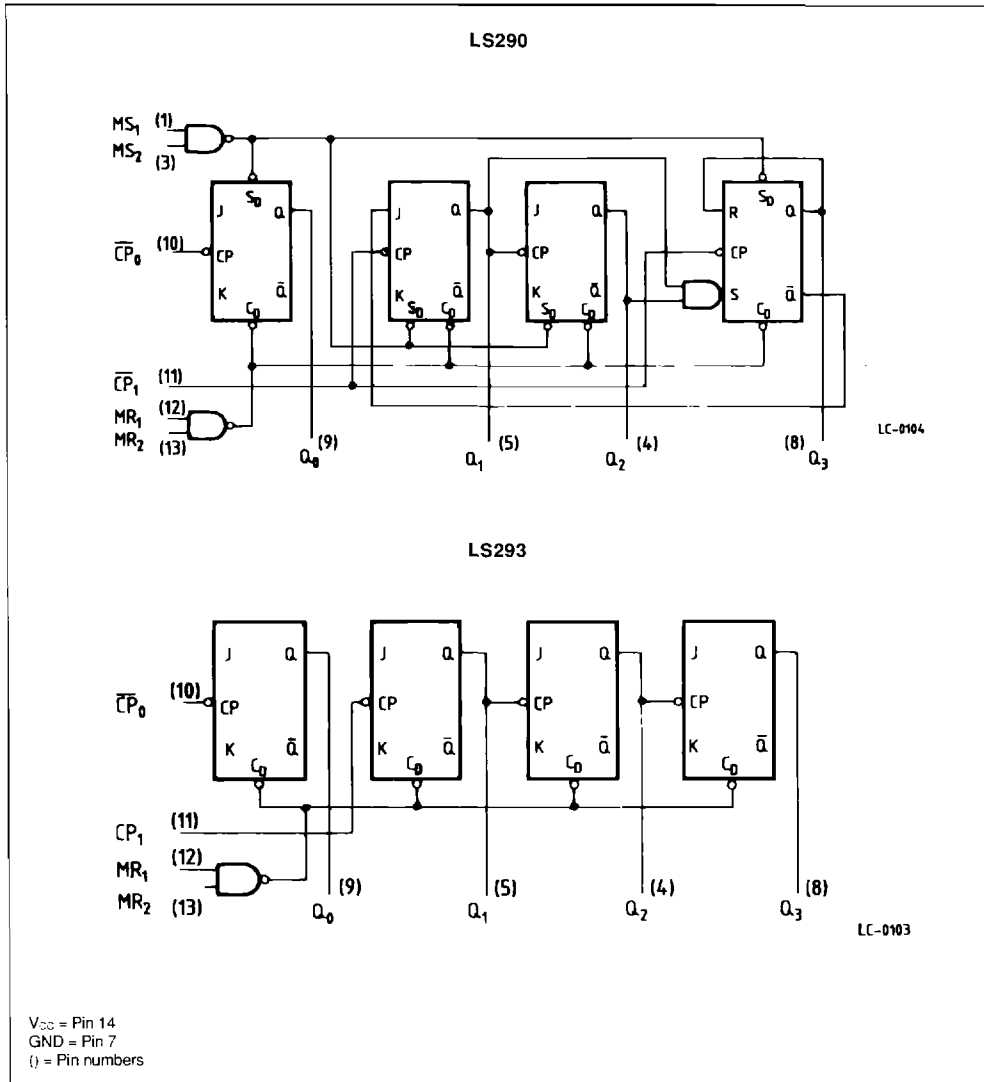
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

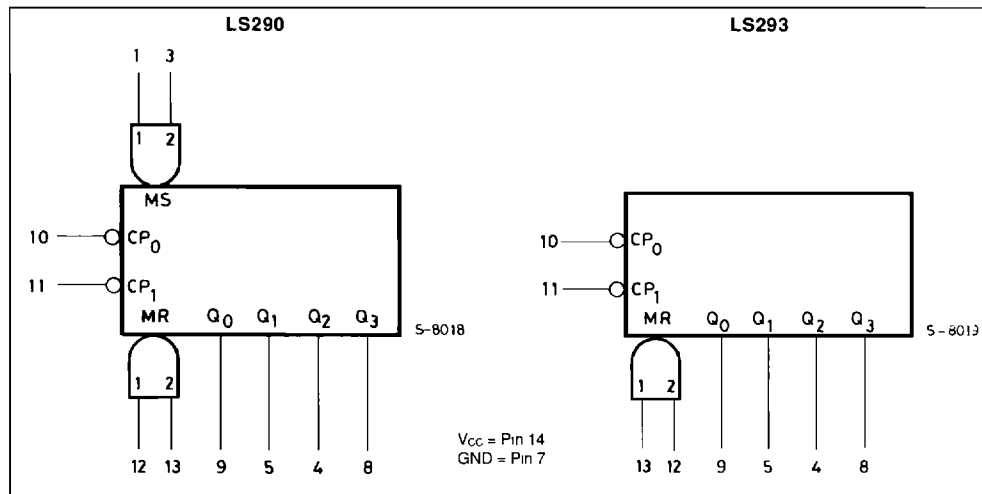
Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS290/293XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

LOGIC DIAGRAMS



LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple Decade, and 4-bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the \overline{CP}_1 input of device.

A gated AND asynchronous Master Reset (MR_1, MS_2) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous master Set (MS_1, MS_2) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes :

LS290

- A. BCD Decade (8421) Counter-the \overline{CP}_1 input must be externally connected to the Q_0 output. The CP_0 input receives the incoming count and BCD count sequence is produced.

- B. Symmetrical Bi-quinary Divide-By-Ten Counter -The Q_3 output must be externally connected to the CP_0 input. The input count is then applied to the CP_1 input and a divide-by-ten square is obtained at output Q_0 .
- C. Divide-By-Two and Divide-By-Five Counter- No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two functions (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain binary divide-by-five operation at the Q_3 output.

LS293

- A. 4-Bit Ripple Counter-The output Q_0 must be externally connected to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous division of 2, 4, 8, and 16 are performed at the $Q_0, Q_1, Q_2,$ and Q_3 outputs as shown in the truth table.
- B. 3-Bit Ripple Counter-The input count pulses are applied to input CP_1 . Simultaneous frequency divisions of 2, 4, and 8 are available at the $Q_0, Q_1, Q_2,$ and Q_3 outputs. Independent of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

BCD COUNT SEQUENCE LS290

Count	Output			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note : Output Q₀ is Connected to Input CP1 for BCD Count

MODE SELECTION LS290

Reset/Set Inputs				Outputs			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X				Count
X	L	X	L				Count
L	X	X	L				Count
X	L	L	X				Count

TRUTH TABLE LS293

Count	Output			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note : Output Q₀ is Connected to Input CP1.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

MODE SELECTION LS293

Reset Inputs		Outputs			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H				Count
H	L				Count
L	L				Count

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit	
		Min.	Typ. (*)	Max.			
V _{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs	V	
V _{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs	V	
V _{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V _{CC} = MIN. I _{IN} = -18 mA	V	
V _{OH}	Output HIGH Voltage	2.7	3.4		V _{CC} = MIN. I _{OH} = - 400 μA V _{IN} = V _{IH} or V _{IL} per Truth Table	V	
V _{OL}	Output LOW Voltage		0.25	0.4	I _{OL} = 4.0 mA	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
			0.35	0.5	I _{OL} = 8.0 mA		V
I _{IH}	Input HIGH Current MS, MR CP ₀ CP ₁ (LS290) CP ₁ (LS293)			20 40 80 40	V _{CC} = MAX, V _{IN} = 2.7 V	μA	
	MS, MR CP ₀ CP ₁ (LS290) CP ₁ (LS293)			0.1 0.2 0.4 0.2	V _{CC} = MAX, V _{IN} = 5.5 V	mA	
I _{IL}	Input LOW Current MS, MR CP ₀ CP ₁ (LS290) CP ₁ (LS293)			- 0.4 - 2.4 - 3.2 - 1.6	V _{CC} = MAX. V _{IN} = 0.4 V	mA	
	Output Short Circuit Current (note 2)	- 20		- 100	V _{CC} = MAX V _{OUT} = 0 V	mA	
I _{CC}	Power Supply Current		9	15	V _{CC} = MAX	mA	

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_a = 25 °C.

AC SET-UP REQUIREMENTS: T_A = 25 °C, V_{CC} = 5.0 V

Symbol	Parameter	Limits				Note	Units
		LS290		LS293			
		Min.	Max.	Min.	Max.		
t _w	CP ₀ Pulse Width	15		15		Fig. 1	ns
t _w	CP ₁ Pulse Width	30		30		Fig. 1	
t _w	MR Pulse Width	30		30		Fig. 2	
t _w	MS Pulse Width	30				Fig. 2, 3	
t _{rec}	Recovery Time MR to CP	25		25		Fig. 2	
t _{rec}	Recovery Time MS to CP	25				Fig. 2, 3	

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH data to Q output

AC CHARACTERISTICS : $T_A = 25\text{ }^\circ\text{C}$

Symbol	Parameter	Limits				Test Conditions	Unit		
		LS290		LS293					
		Min.	Max.	Min.	Max.				
f_{MAX}	$\overline{\text{CP}}_0$ Input Count Frequency	32		32		Fig. 1	MHz		
f_{MAX}	$\overline{\text{CP}}_1$ Input Count Frequency	16		16		Fig. 1	MHz		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}_0$ Input to Q_0 Output		16 18		16 18	Fig. 1	$V_{\text{CC}} = 5.0\text{ V}$ $C_L = 15\text{ pF}$	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}_1$ Input to Q_1 Output		16 21		16 21			ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}_1$ Input to Q_2 Output		32 35		32 35			ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}_1$ Input to Q_3 Output		32 35		51 51			ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}_0$ Input to Q_3 Output		48 50		70 70			ns	
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30					Fig. 3	ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		40					Fig. 2	ns
t_{PHL}	MR Input to any Output		40		40	Fig. 2	ns		

AC WAVEFORMS

Figure 1.

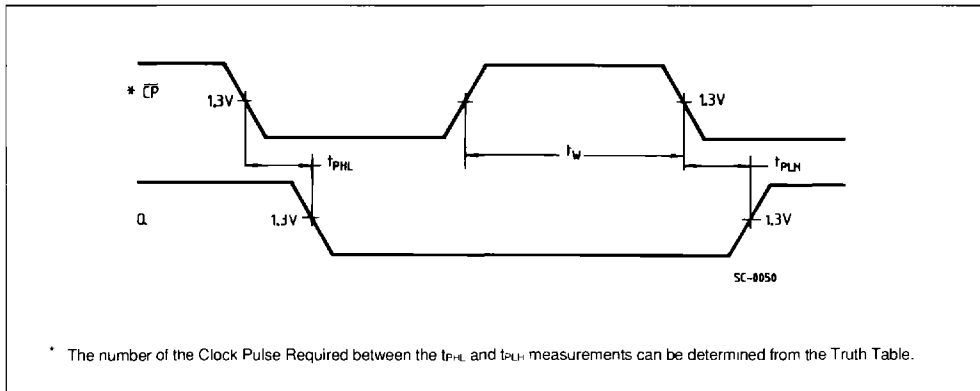


Figure 2.

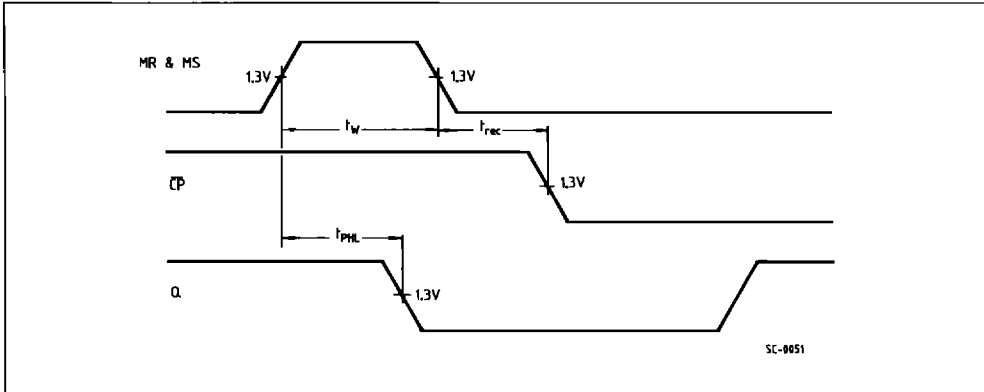


Figure 3.

