

**Driver / MOSFET Combination**  
**DEIC-515 Driver combined with a DE375-102N12A MOSFET**  
**Gate driver matched to MOSFET**

**1000 Volts**  
**12 A**  
**0.7 Ohms**

### Features

- Isolated Substrate
  - high isolation voltage (>2500V)
  - excellent thermal transfer
  - Increased temperature and power cycling capability
- IXYS advanced Z-MOS process
- Low  $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- Low Quiescent Supply Current

### Advantages

- Optimized for RF and high speed
- Easy to mount—no insulators needed
- High power density
- Single package reduces size and heat sink area

### Description

The IXZ4DF12N100 is a CMOS high speed high current gate driver and a MOSFET combination specifically designed Class D, E, HF, RF applications at up to 40MHz, as well as other applications. The IXZ4DF12N100 in pulse mode can provide 72A of peak current while producing voltage rise and fall times of less than 5ns, and minimum pulse widths of 8ns. The input of the driver is fully immune to latch up over the entire operating range. Designed with small internal delays, the IXZ4DF12N100 is suitable for higher power operation where combiners are used. Its features and wide safety margin in operating voltage and power make the IXZ4DF12N100 unmatched in performance and value.

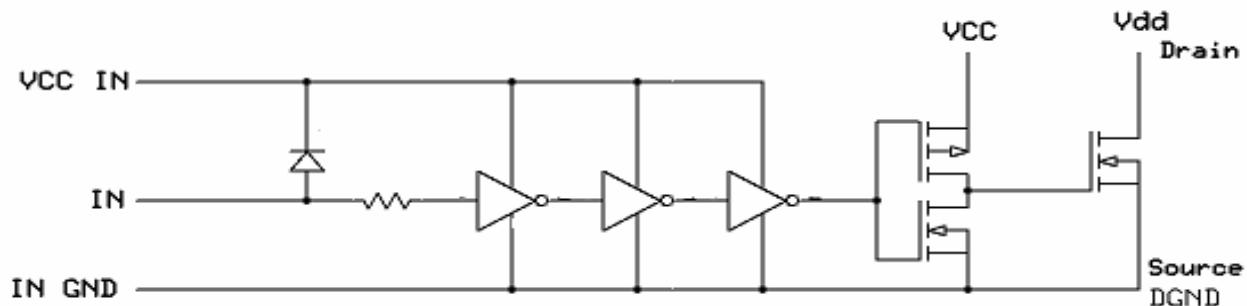
The IXZ4DF12N100 is packaged in DEIs low inductance RF package incorporating DEI's RF layout techniques to minimize stray lead inductances for optimum switching performance. The IXZ4DF12N100 is a surface-mountable device.



### Applications

- Class D or E Switching Amplifier
- Multi MHz Switch Mode Power Supplies (SMPS)

**Figure 1.**  
**Functional Diagram**



# PRELIMINARY

**Device Specifications**

Parameter	Value
Maximum Junction Temperature	150°C
Operating Temperature Range	- 40°C to 85°C
Weight	5.5g

Symbol	Test Conditions	Maximum Ratings
$f_{MAX}$	$I_D = 0.5I_{DM25}$	40MHz
$V_{DSS}$		1000V
$V_{CC}, V_{CCIN}$		20V
$I_{DSS}$	$V_{DS} = 0.8V_{DSS}$ $T_J = 25^\circ C$ $V_{GS} = 0V$ $T_J = 125^\circ C$	50uA 1mA
$I_{DM25}$	$T_C = 25^\circ C$	12A
$I_{DM}$	$T_C = 25^\circ C$ , Pulse limited by $T_{JM}$	72A
$I_{AR}$	$T_C = 25^\circ C$	12A
$P_T$ (MOSFET and Driver)	$T_C = 25^\circ C$	TBD 500W
$R_{thJC}$		0.25 °C/W
$R_{thJHS}$		TBD °C/W

**Device Performance**

Symbol	Test Condition	Minimum	Typical	Maximum
$R_{ds(ON)}$	$V_{CC} = 15V, I_D = 0.5I_{DM25}$ Pulse Test, $t \leq 300\mu S$ , Duty Cycle $\leq 2\%$		0.7 $\Omega$	
$V_{CC}, V_{CCIN}$		8V	15V	20V
$I_N$ (Signal Input)		- 5V		$V_{CCIN} + 0.3V$
$V_{IH}$ (High Input Voltage)		$V_{CCIN} - 2V$		$V_{CCIN} + 0.3V$
$V_{IL}$ (Low Input Voltage)			0.8V	
$Z_{IN}$	$f = 1MHz$		7960 $\Omega$	
$C_{stray}$	$f = 1MHz$ Any one pin to the back plane metal		46pf	
$C_{OSS}$	$V_{GS} = 0V,$ $V_{DS} = 0.8V_{DSS(max)},$ $f = 1MHz$		150pf	
$t_{ONDLY}$	$T_C = 25^\circ C$ $V_{CC}, V_{CCIN}, V_{IN} = 15V$ 1 $\mu S$ Pulse,		20nS	
$t_{OFFDLY}$	$V_{DS} = 50V, R_L = 2.5\Omega$		22.6nS	
$t_R$	$T_C = 25^\circ C$ $V_{CC}, V_{CCIN}, V_{IN} = 15V$ 1 $\mu S$ Pulse,		3nS	
$t_F$	$V_{DS} = 50V, R_L = 2.5\Omega$		4.5nS	

**PRELIMINARY**

Fig. 2

Extended Output Characteristics @ 25°C

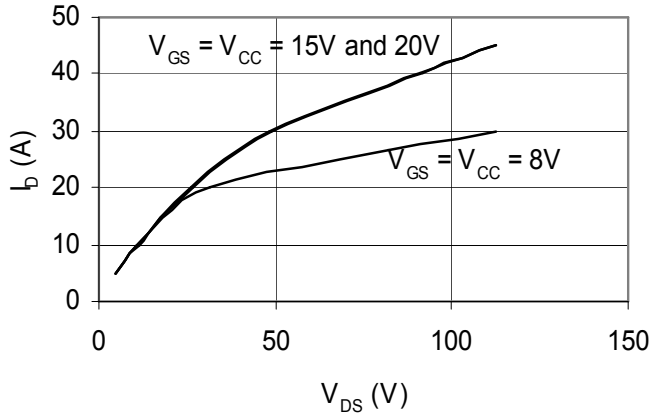


Fig. 3

$R_{DS(ON)}$  vs. Temperature  
 $I_D = 0.5I_{DM}$

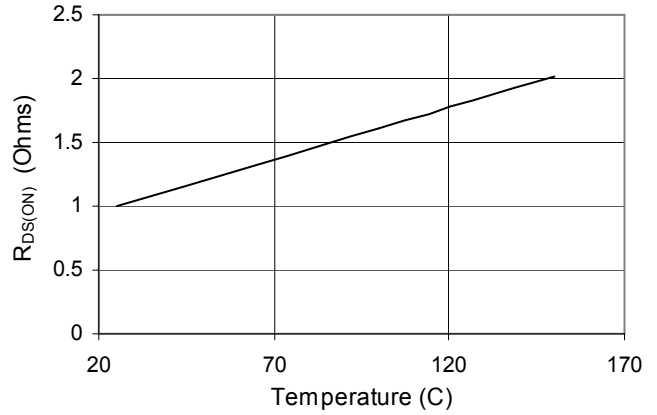


Fig. 4

Propagation Delay ON vs. Supply Voltage  
 $I_D = 0.5I_{DM}$

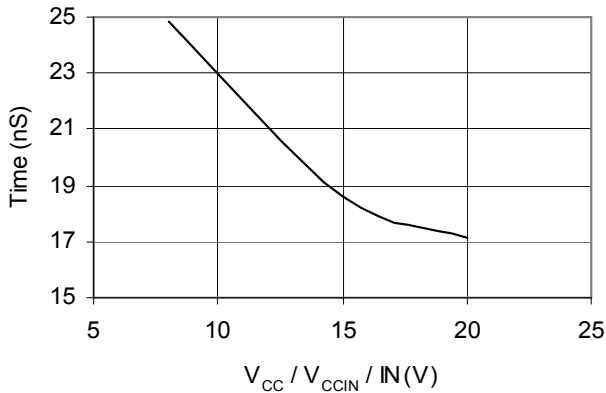


Fig. 5

Propagation Delay OFF vs. Supply Voltage

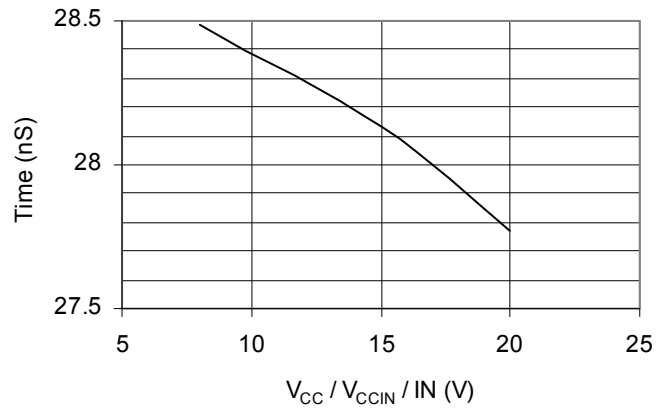


Fig. 6

Propagation Delay ON vs. Temperature  
 $I_D = 0.5 I_{DM}$ ,  $V_{CC} / V_{CCIN} / IN = 15V$

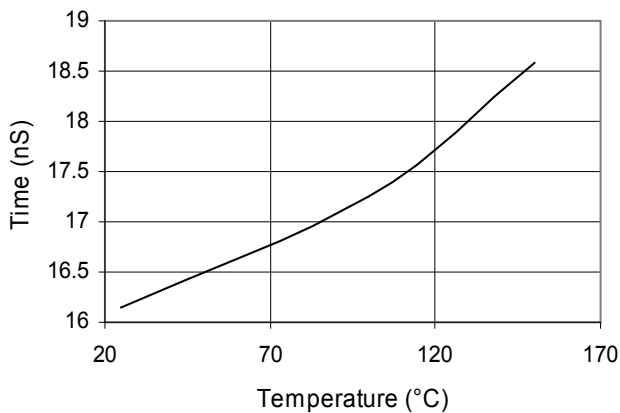
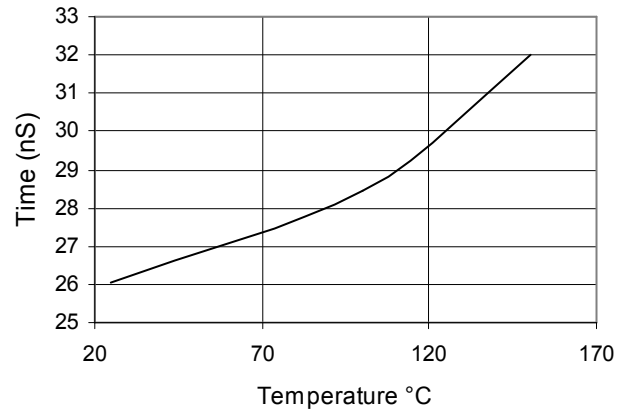


Fig. 7

Propagation Delay OFF vs. Temperature  
 $I_D = 0.5 I_{DM}$ ,  $V_{CC} / V_{CCIN} / IN = 15V$



**PRELIMINARY**

Fig. 8 Rise Time vs. Supply Voltage  
 $I_D = 0.5 I_{DM}$

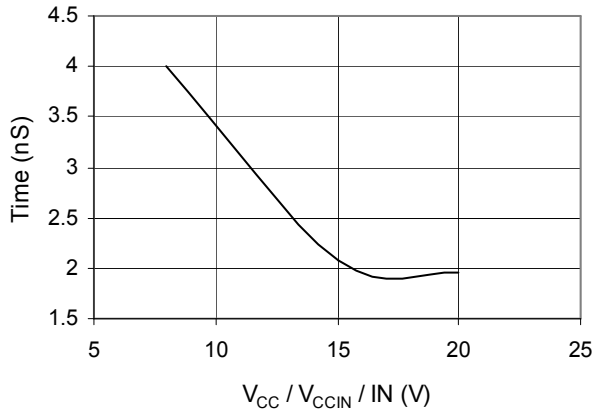


Fig. 9 Fall Time vs. Supply Voltage  
 $I_D = 0.5 I_{DM}$

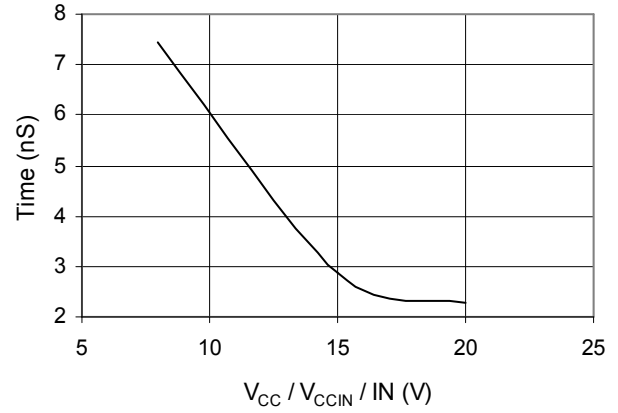


Fig. 10 Rise Time vs. Temperature  
 $I_D = 0.5 I_{DM}, V_{CC}/V_{CCIN}/IN = 15V$

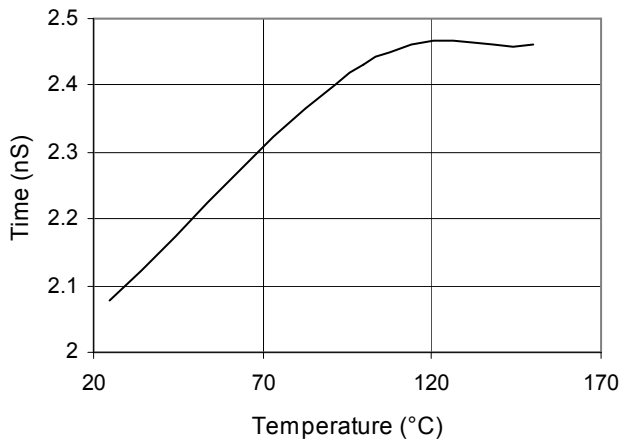


Fig. 11 Fall Time vs. Temperature  
 $I_D = 0.5 I_{DM}, V_{CC}/V_{CCIN}/IN = 15V$

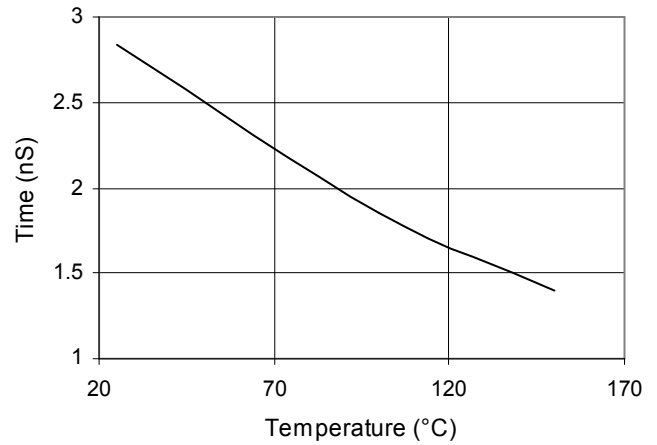


Fig. 12 Output Capacitance vs.  $V_{DS}$  Voltage

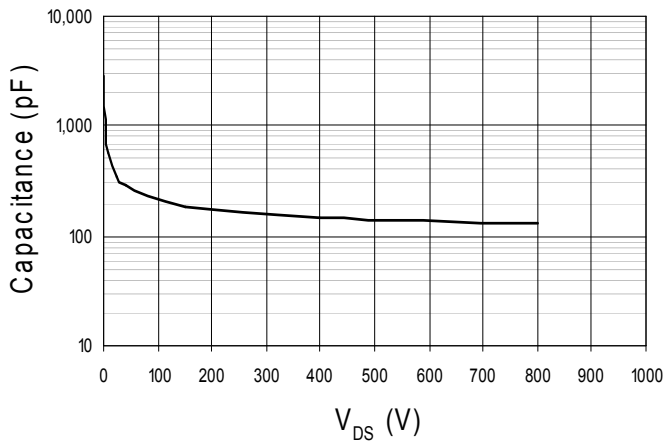
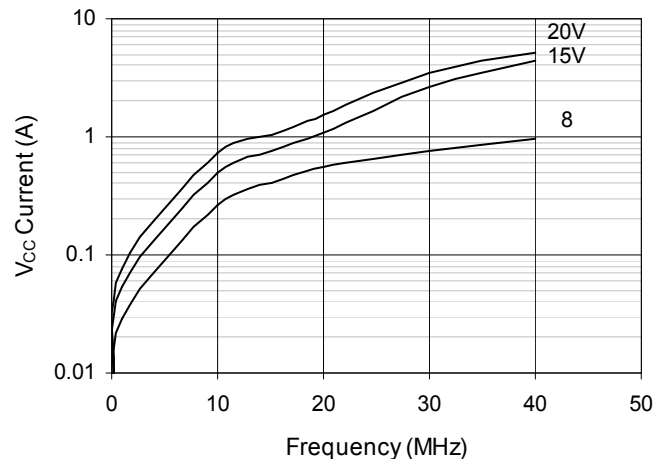
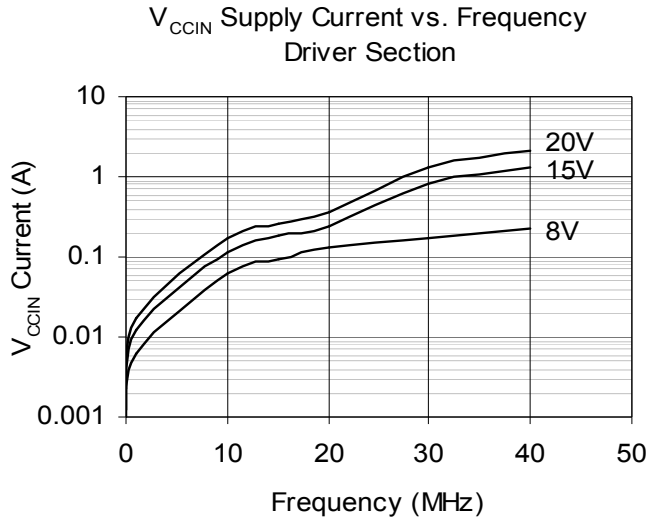


Fig. 13  $V_{CC}$  Supply Current vs. Frequency  
Driver Section



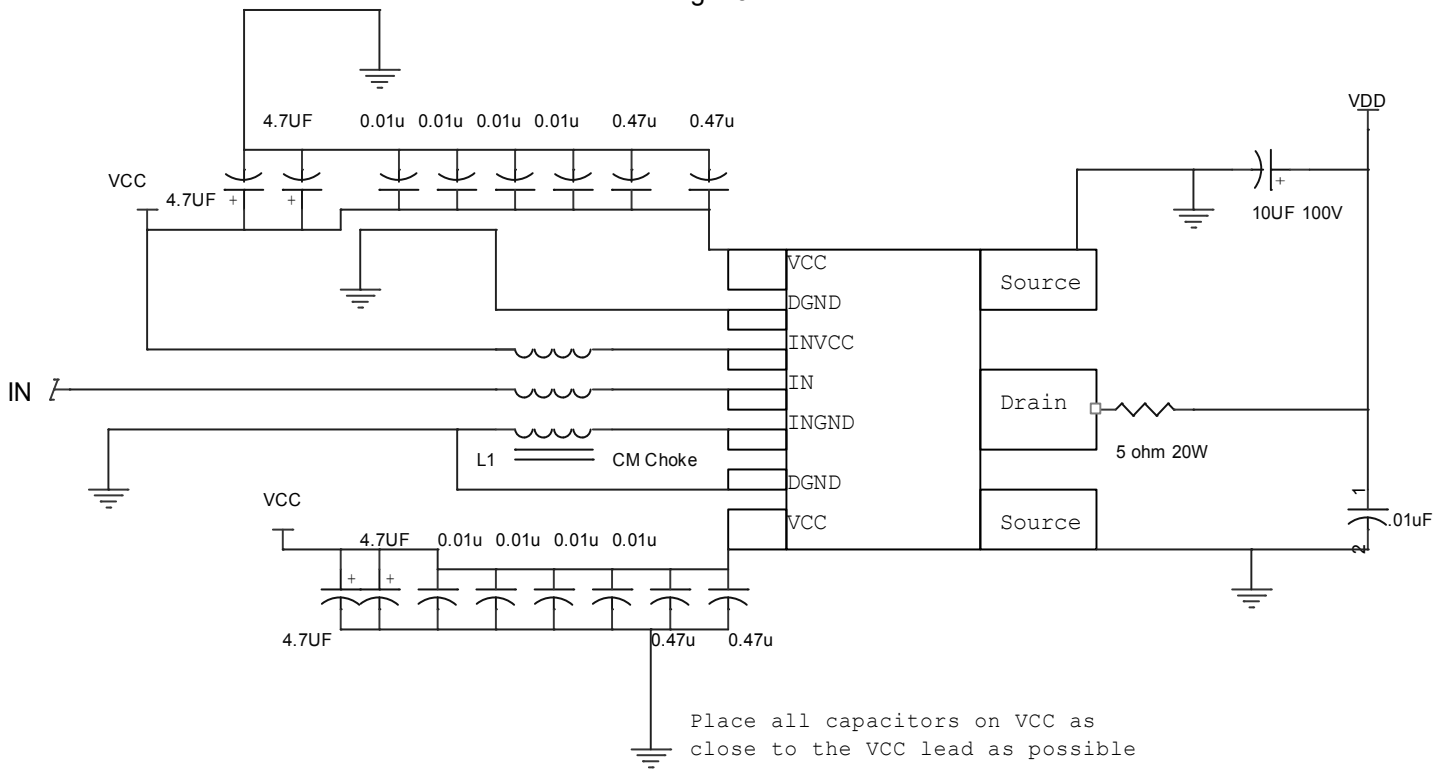
**PRELIMINARY**

Fig. 14



### Test Circuit

Fig. 15



**PRELIMINARY**

**Lead Description**

<b>SYMBOL</b>	<b>FUNCTION</b>	<b>DESCRIPTION</b>
Drain	MOSFET Drain	Drain of Power MOSFET.
Source	MOSFET Source	Source of Power MOSFET. This connection is common to DGND.
VCC	Driver Section Supply Voltage	Power supply input for the driver output section. These leads provide power to the output section of the DEIC515 driver. Both leads must be connected.
VCCIN	Input Section Supply Voltage	Input for the positive input section power-supply voltage. This lead provides power to the input section of the DEIC515 driver. This lead should not be directly connected to VCC.
IN	Input	Input signal.
DGND	Power Driver Ground	The system ground leads. Internally connected to all circuitry, these leads provide ground reference for the entire chip. These leads should be connected to a low noise analog ground plane for optimum performance.
INGND	Input Section Ground	The input section ground lead. This lead is a Kelvin connection internally connected to DGND. This lead must not be connected to DGND as excessive current can damage this lead.

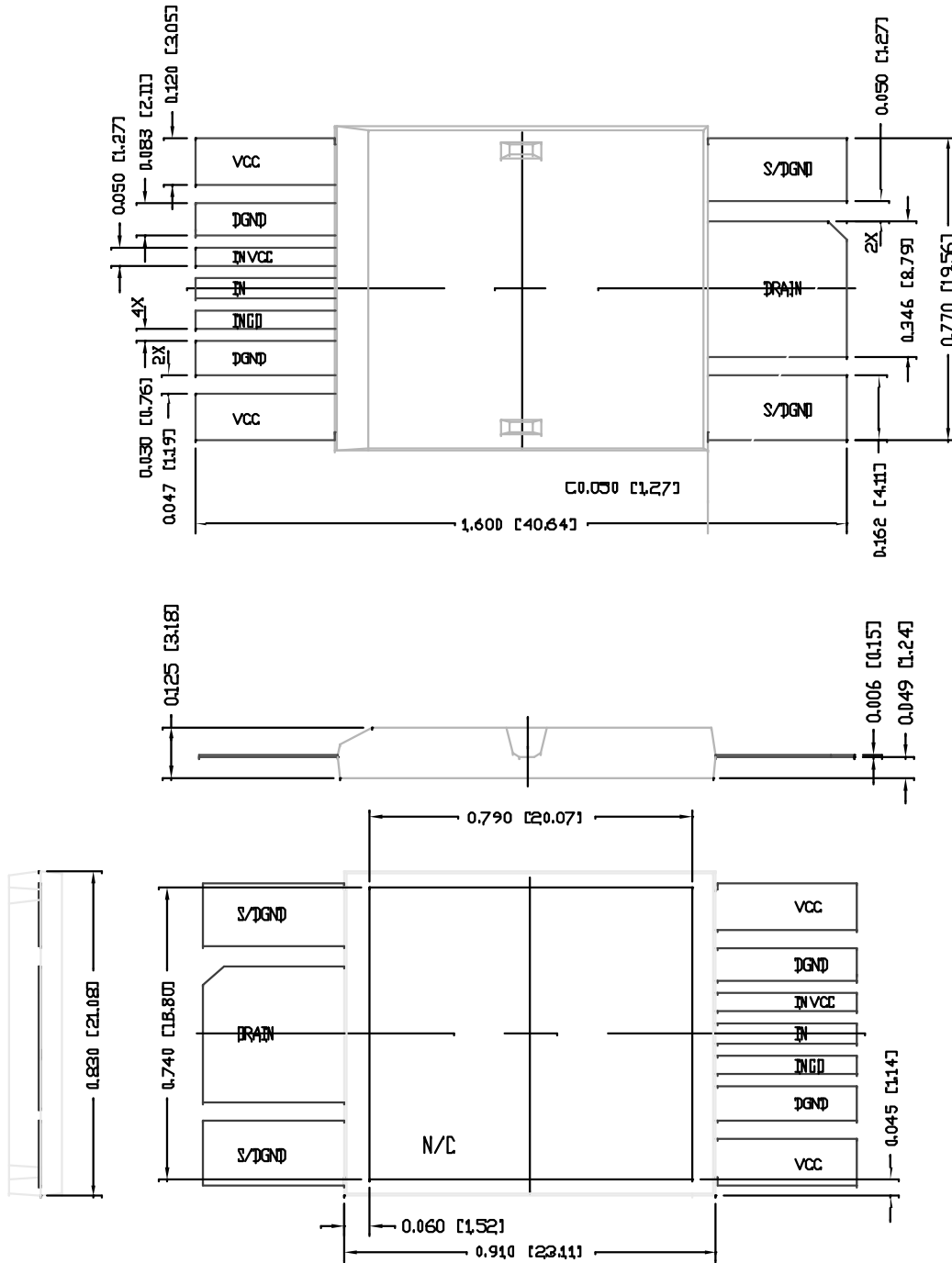
IXYS RF reserves the right to change limits, test conditions and dimensions without notice.

IXYS RF MOSFETS are covered by one or more of the following U.S. patents:

4,835,592    4,860,072    4,881,106    4,891,686    4,931,844    5,017,508  
 5,034,796    5,049,961    5,063,307    5,187,117    5,237,481    5,486,715  
 5,381,025    5,640,045    6,404,065    6,583,505    6,710,463    6,727,585  
 6,731,002

***PRELIMINARY***

Fig. 16 IXZ4DF12N100 Package Outline



IXYS RF  
An IXYS Company  
2401 Research Blvd. Ste. 108, Ft. Collins, CO 80526  
Tel: 970-493-1901; Fax: 970-493-1903  
e-mail: deiinfo@directedenergy.com

**PRELIMINARY**