

# Current Mode PWM Controller

## FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- $\pm 1\%$  Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500kHz Operation

## DESCRIPTION

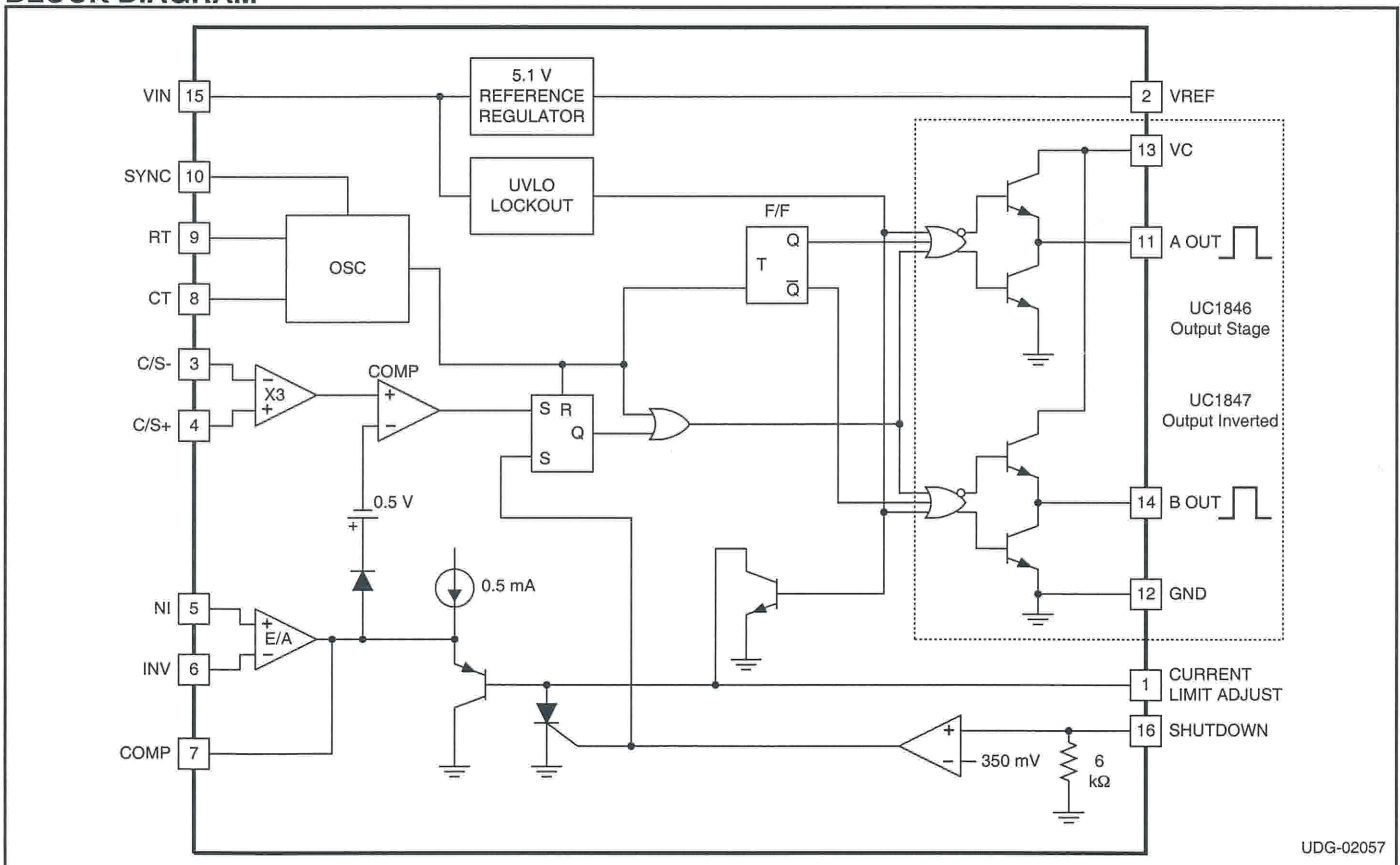
The UC1846/7 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a  $\pm 1\%$  trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

## BLOCK DIAGRAM



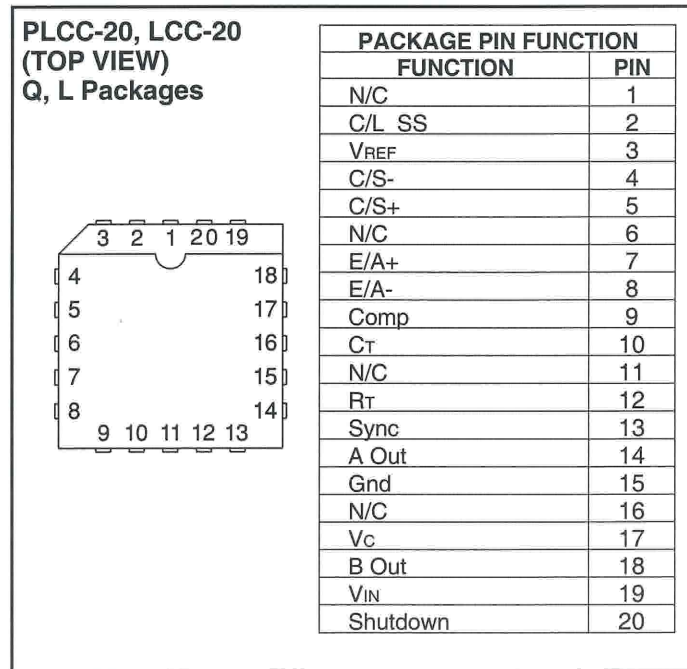
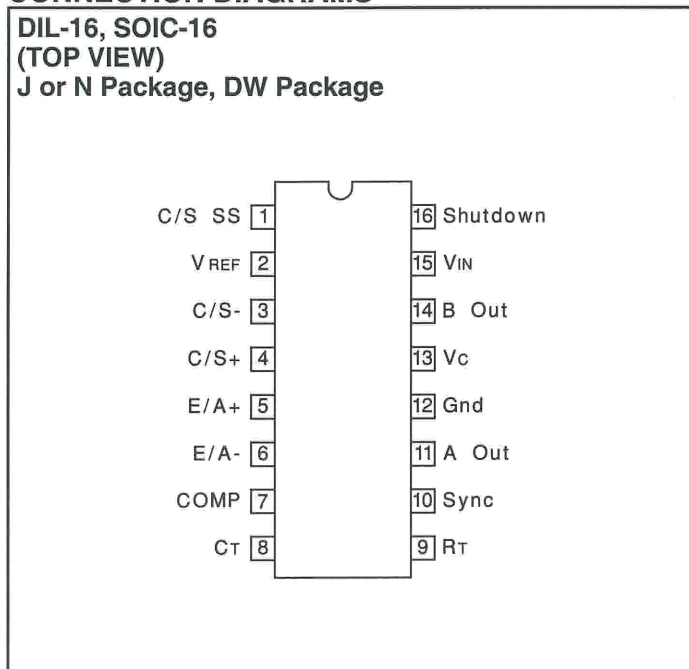
UDG-02057

### ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15)	+40V
Collector Supply Voltage (Pin 13)	+40V
Output Current, Source or Sink (Pins 11, 14)	500mA
Analog Inputs (Pins 3, 4, 5, 6, 16)	-0.3V to +V <sub>IN</sub>
Reference Output Current (Pin 2)	-30mA
Sync Output Current (Pin 10)	-5mA
Error Amplifier Output Current (Pin 7)	-5mA
Soft Start Sink Current (Pin 1)	50mA
Oscillator Charging Current (Pin 9)	5mA
Power Dissipation at T <sub>A</sub> =25°C	1000mW
Power Dissipation at T <sub>C</sub> =25°C	2000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

### CONNECTION DIAGRAMS



**ELECTRICAL CHARACTERISTICS** (Unless otherwise stated, these specifications apply for T<sub>A</sub>=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V<sub>IN</sub>=15V, R<sub>T</sub>=10k, C<sub>T</sub>=4.7nF, T<sub>A</sub>=T<sub>J</sub>.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<b>Reference Section</b>								
Output Voltage	T <sub>J</sub> =25°C, I <sub>O</sub> =1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V <sub>IN</sub> =8V to 40V		5	20		5	20	mV
Load Regulation	I <sub>L</sub> =1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T <sub>J</sub> =25°C (Note 2)		100			100		μV
Long Term Stability	T <sub>J</sub> =125°C, 1000 Hrs. (Note 2)		5			5		mV
Short Circuit Output Current	V <sub>REF</sub> =0V	-10	-45		-10	-45		mA

**ELECTRICAL CHARACTERISTICS (cont.)** (Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for UC1846/7;  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2846/7; and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3846/7;  $V_{IN} = 15\text{V}$ ,  $R_T = 10\text{k}$ ,  $C_T = 4.7\text{nF}$ ,  $T_A = T_J$ .)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<b>Oscillator Section</b>								
Initial Accuracy	$T_J = 25^\circ\text{C}$	39	43	47	39	43	47	kHz
Voltage Stability	$V_{IN} = 8\text{V}$ to $40\text{V}$		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			3.9			V
Sync Input Low Level	Pin 8=0V			2.5			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5		1.3	1.5	mA
<b>Error Amp Section</b>								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	$\mu\text{A}$
Input Offset Current			40	250		40	250	nA
Common Mode Range	$V_{IN} = 8\text{V}$ to $40\text{V}$	0		$V_{IN} - 2\text{V}$	0		$V_{IN} - 2\text{V}$	V
Open Loop Voltage Gain	$\Delta V_O = 1.2$ to $3\text{V}$ , $V_{CM} = 2\text{V}$	80	105		80	105		dB
Unity Gain Bandwidth	$T_J = 25^\circ\text{C}$ (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	$V_{CM} = 0\text{V}$ to $38\text{V}$ , $V_{IN} = 40\text{V}$	75	100		75	100		dB
PSRR	$V_{IN} = 8\text{V}$ to $40\text{V}$	80	105		80	105		dB
Output Sink Current	$V_{ID} = -15\text{mV}$ to $-5\text{V}$ , $V_{PIN 7} = 1.2\text{V}$	-2	6		-2	6		mA
Output Source Current	$V_{ID} = 15\text{mV}$ to $5\text{V}$ , $V_{PIN 7} = 2.5\text{V}$	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	$R_L = (\text{Pin } 7) 15\text{k}\Omega$	4.3	4.6		4.3	4.6		V
Low Level Output Voltage			0.7	1		0.7	1	V
<b>Current Sense Amplifier Section</b>								
Amplifier Gain	$V_{PIN 3} = 0\text{V}$ , Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ( $V_{PIN 4} - V_{PIN 3}$ )	Pin 1 Open (Note 3) $R_L (\text{Pin } 7) = 15\text{k}\Omega$	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN 1} = 0.5\text{V}$ , Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	$V_{CM} = 1\text{V}$ to $12\text{V}$	60	83		60	83		dB
PSRR	$V_{IN} = 8\text{V}$ to $40\text{V}$	60	84		60	84		dB
Input Bias Current	$V_{PIN 1} = 0.5\text{V}$ , Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	$\mu\text{A}$
Input Offset Current	$V_{PIN 1} = 0.5\text{V}$ , Pin 7 Open (Note 3)		0.08	1		0.08	1	$\mu\text{A}$
Input Common Mode Range		0		$V_{IN} - 3$	0		$V_{IN} - 3$	V
Delay to Outputs	$T_J = 25^\circ\text{C}$ , (Note 2)		200	500		200	500	ns
<b>Current Limit Adjust Section</b>								
Current Limit Offset	$V_{PIN 3} = 0\text{V}$ , $V_{PIN 4} = 0\text{V}$ , Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN 5} = V_{REF}$ , $V_{PIN 6} = 0\text{V}$		-10	-30		-10	-30	$\mu\text{A}$
<b>Shutdown Terminal Section</b>								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		$V_{IN}$	0		$V_{IN}$	V
Minimum Latching Current (IPIN 1)	(Note 6)	3.0	1.5		3.0	1.5		mA

**ELECTRICAL CHARACTERISTICS (cont.)**

(Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for UC1846/7;  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2846/7; and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3846/7;  $V_{IN} = 15\text{V}$ ,  $R_T = 10\text{k}$ ,  $C_T = 4.7\text{nF}$ ,  $T_A = T_J$ .)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<b>Shutdown Terminal Section (cont.)</b>								
Maximum Non-Latching Current ( $I_{PIN 1}$ )	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	$T_J = 25^\circ\text{C}$ (Note 2)		300	600		300	600	ns
<b>Output Section</b>								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	$V_C = 40\text{V}$ (Note 5)			200			200	$\mu\text{A}$
Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 100\text{mA}$		0.4	2.1		0.4	2.1	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{SOURCE} = 100\text{mA}$	12	13.5		12	13.5		V
Rise Time	$C_L = 1\text{nF}$ , $T_J = 25^\circ\text{C}$ (Note 2)		50	300		50	300	ns
Fall Time	$C_L = 1\text{nF}$ , $T_J = 25^\circ\text{C}$ (Note 2)		50	300		50	300	ns
<b>Under-Voltage Lockout Section</b>								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
<b>Total Standby Current</b>								
Supply Current			17	21		17	21	mA

Note 2. These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.

Note 3. Parameter measured at trip point of latch with  $V_{PIN 5} = V_{REF}$ ,  $V_{PIN 6} = 0\text{V}$ .

Note 4. Amplifier gain defined as:  $G = \frac{\Delta V_{PIN7}}{\Delta V_{PIN4}}$ ;  $V_{PIN4} = 0$  to  $1.0\text{V}$

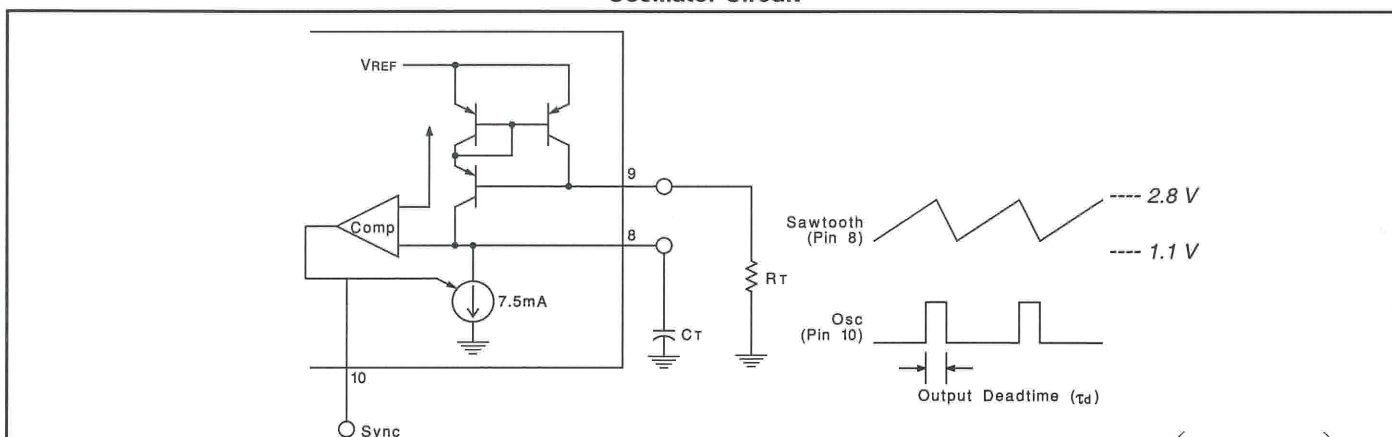
Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.

Note 6. Current into Pin 1 ensured to latch circuit in shutdown state.

Note 7. Current into Pin 1 ensured not to latch circuit in shutdown state.

**APPLICATIONS DATA**

**Oscillator Circuit**



Output deadtime is determined by the external capacitor,  $C_T$ , according to the formula:  $\tau_d (\mu\text{s}) = 145C_T (\mu\text{f}) \left( \frac{I_D}{I_D - \frac{3.6}{RT (\text{k}\Omega)}} \right)$ .

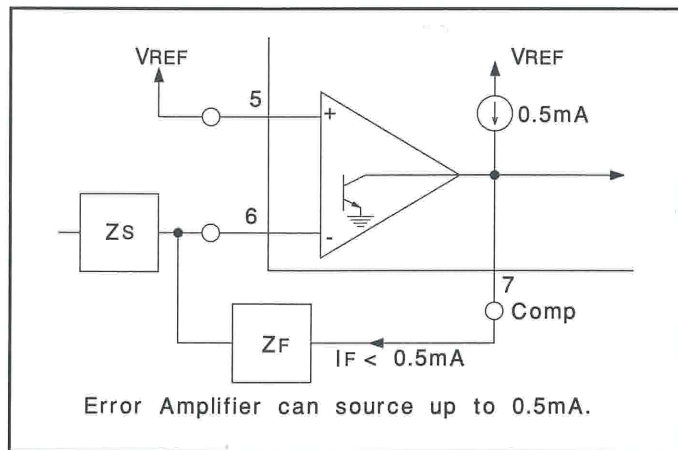
$I_D$  = Oscillator discharge current at  $25^\circ\text{C}$  is typically 7.5.

For large values of  $R_T$ :  $\tau_d (\mu\text{s}) \approx 145C_T (\mu\text{f})$ .

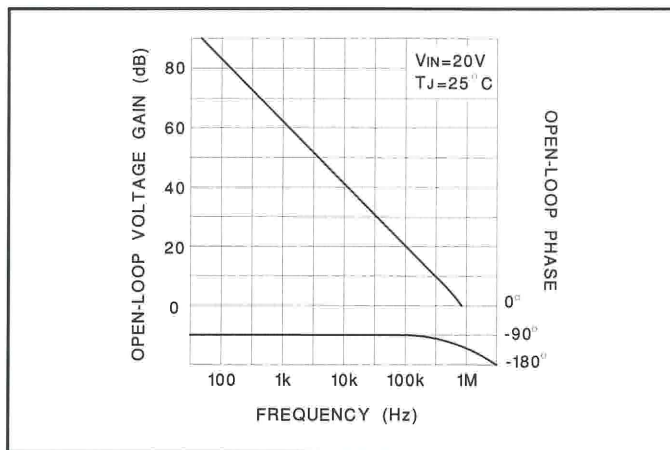
Oscillator frequency is approximated by the formula:  $f_T (\text{kHz}) \approx \frac{2.2}{RT (\text{k}\Omega) \cdot C_T (\mu\text{f})}$ .

APPLICATIONS DATA (cont.)

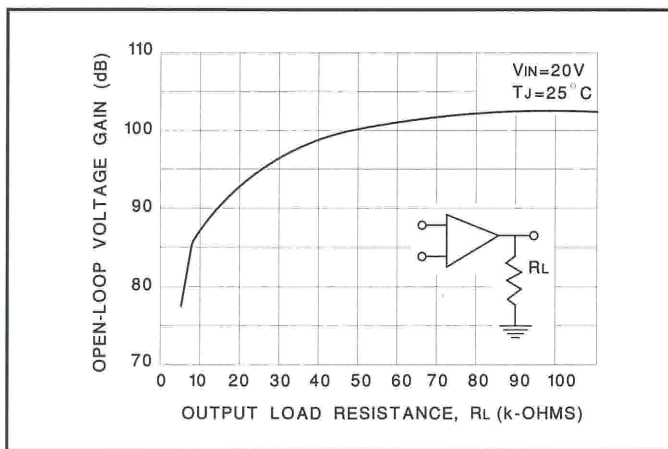
Error Amp Output Configuration



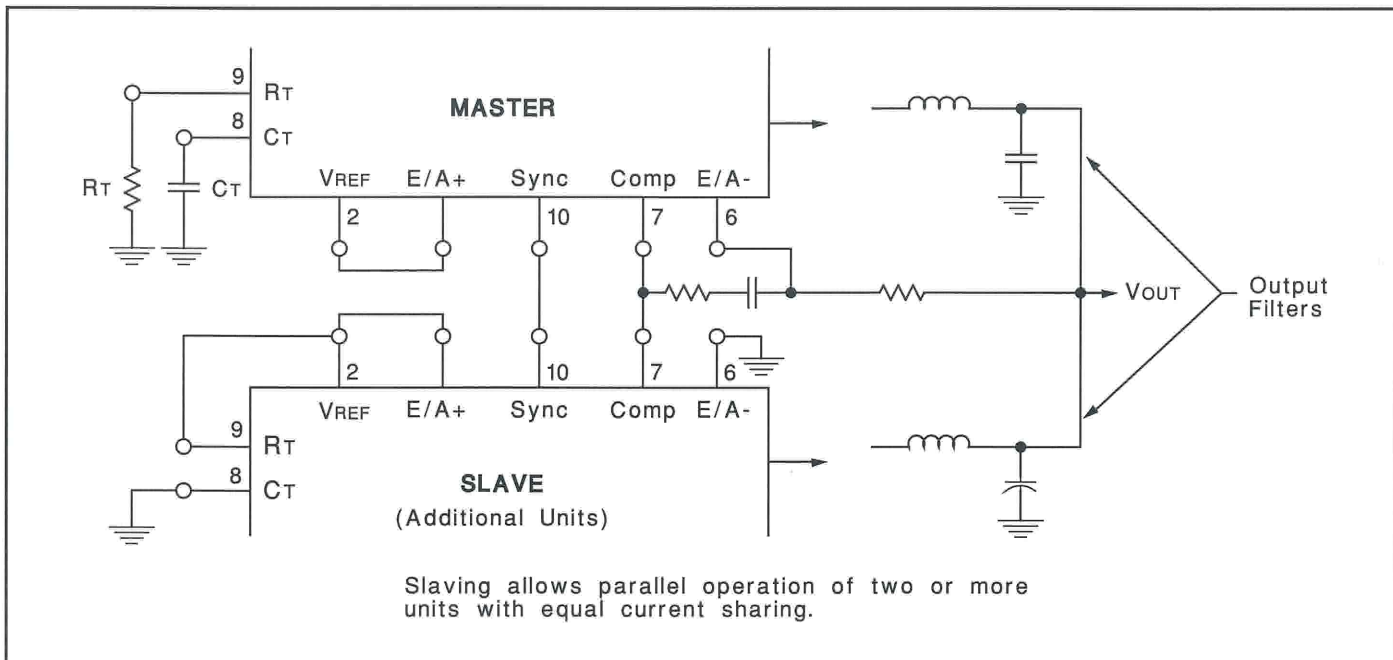
Error Amp Gain and Phase vs Frequency



Error Amp Open-Logic D.C. Gain vs Load Resistance

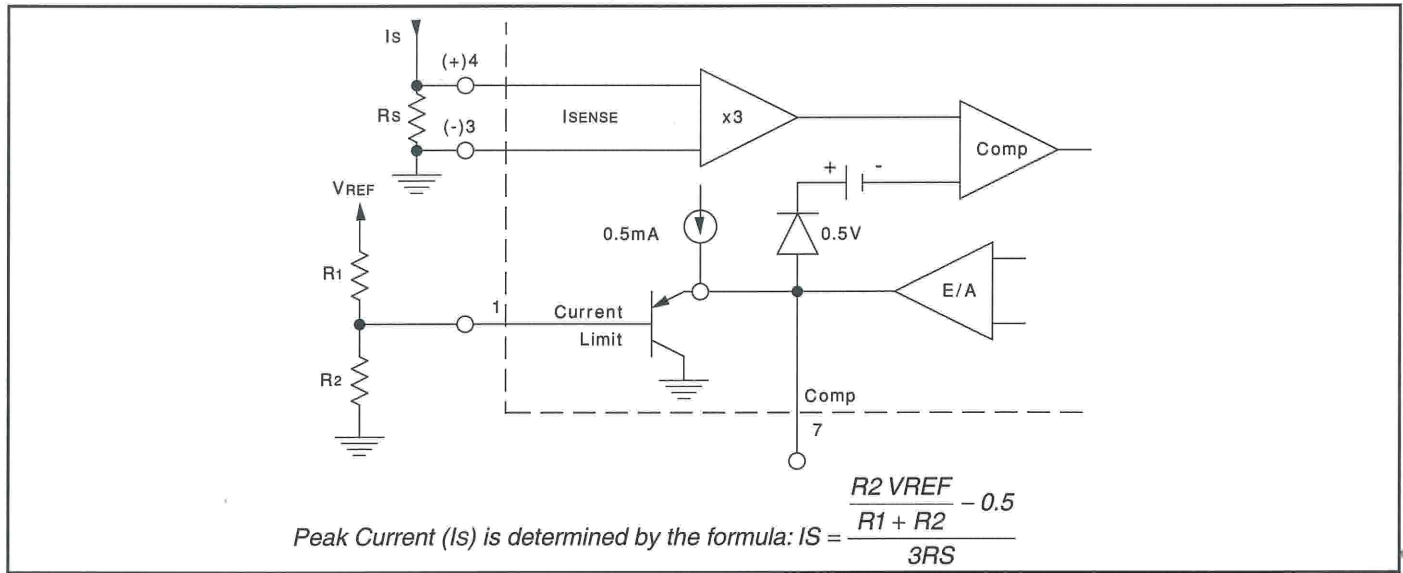


Parallel Operation

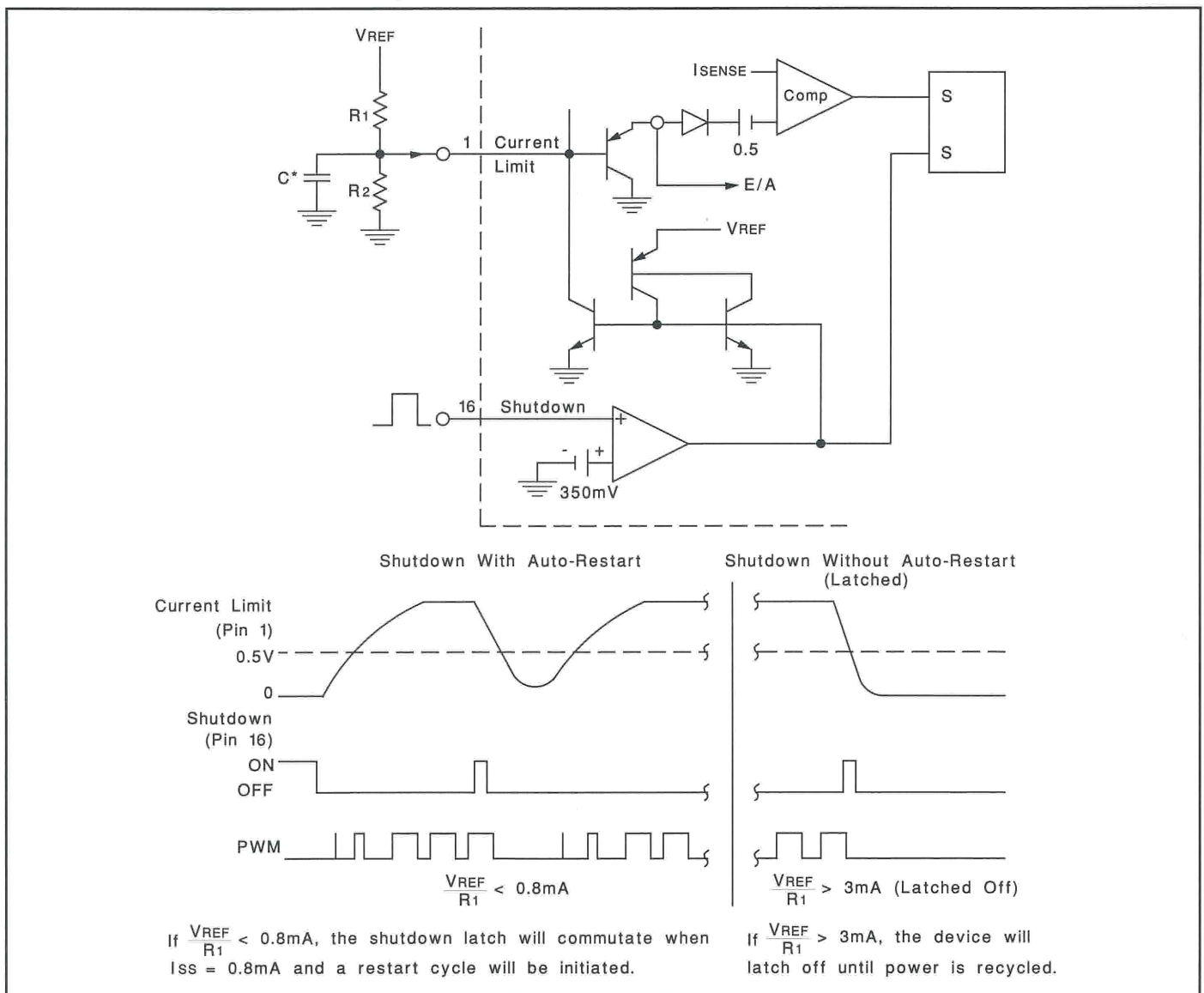


APPLICATIONS DATA (cont.)

Pulse by Pulse Current Limiting

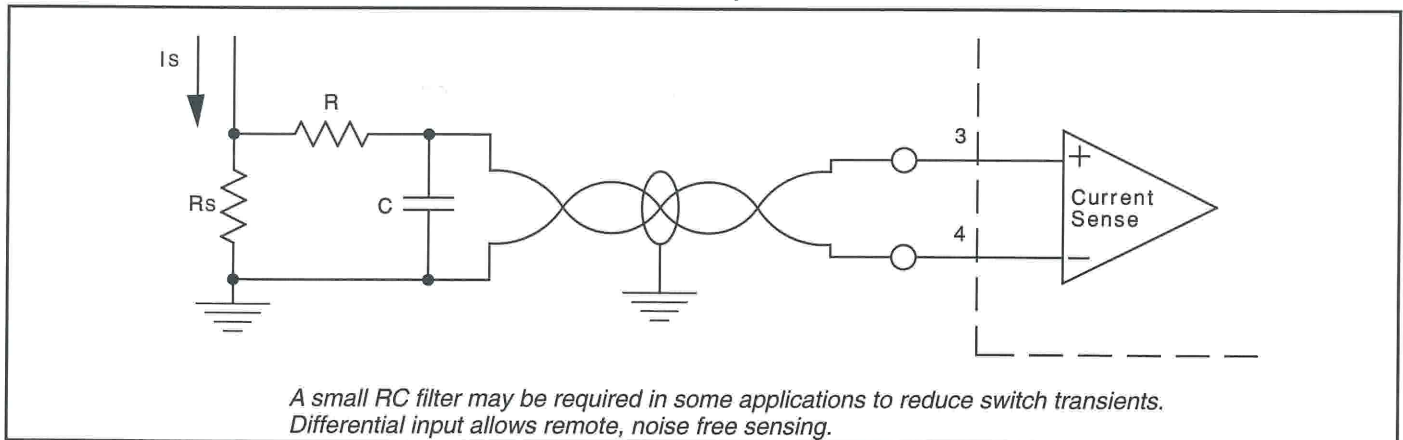


Soft Start and Shutdown /Restart Functions

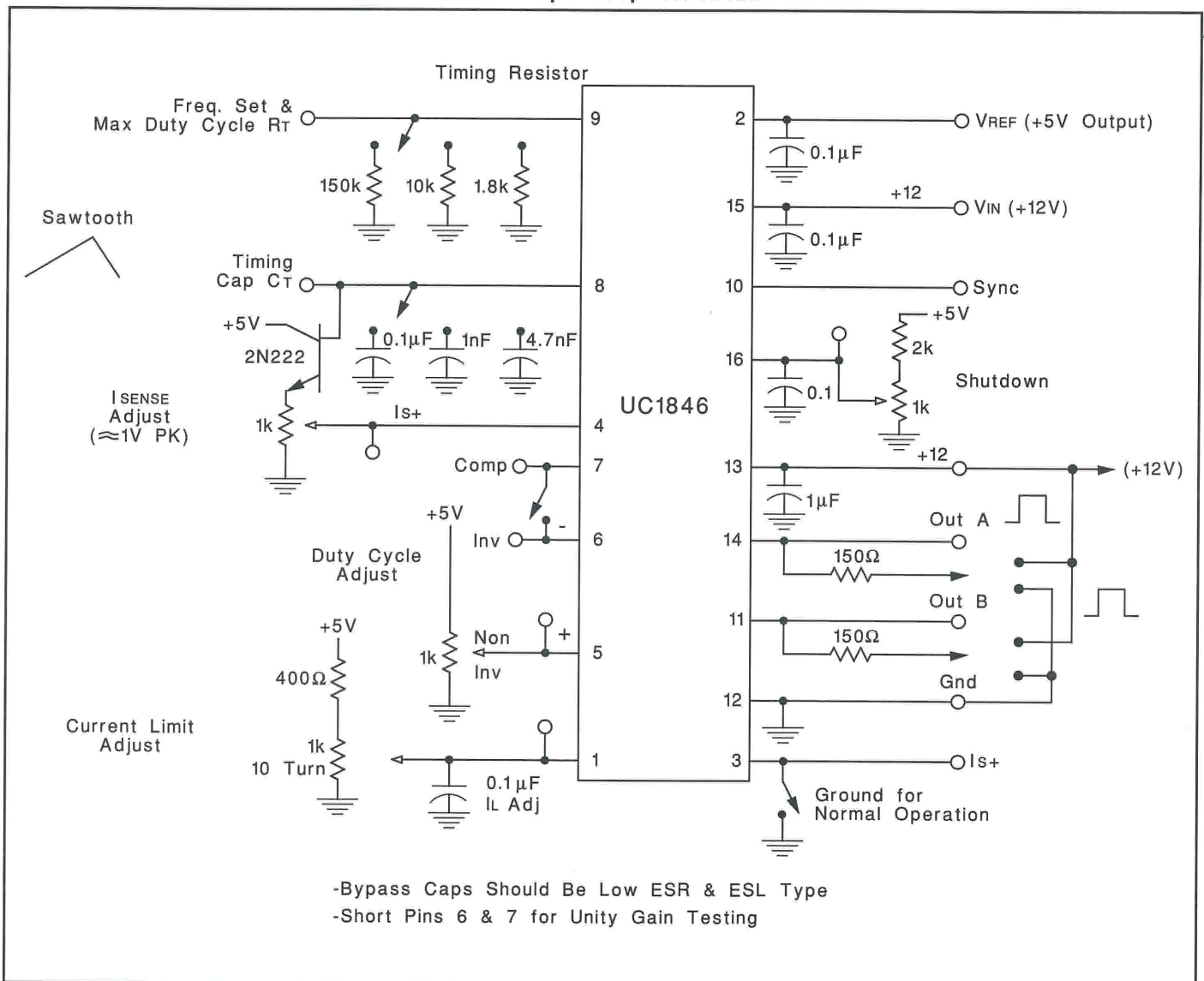


APPLICATIONS DATA (cont.)

Current Sense Amp Connection



UC1846 Open Loop Test Circuit



## REVISION HISTORY

SLUS352A to SLUS352B July 2010:

- 1) Updated block diagram, page 1.
- 2) Added peak and vally voltages to the Oscillator Circuit, page 4.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86806012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86806012A UC1846L/ 883B	<a href="#">Samples</a>
5962-8680601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8680601EA UC1846J/883B	<a href="#">Samples</a>
UC1846J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1846J	<a href="#">Samples</a>
UC1846J/80257	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1846J/80364	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1846J/80619	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1846J883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8680601EA UC1846J/883B	<a href="#">Samples</a>
UC1846L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86806012A UC1846L/ 883B	<a href="#">Samples</a>
UC1847J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1847J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
UC1847L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
UC1847L883B	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
UC2846DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2846DW	<a href="#">Samples</a>
UC2846DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2846DW	<a href="#">Samples</a>
UC2846DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2846DW	<a href="#">Samples</a>
UC2846DWTR/81265	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI			
UC2846DWTR/81265G4	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI			
UC2846DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2846DW	<a href="#">Samples</a>
UC2846J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-40 to 85	UC2846J	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2846N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2846N	<a href="#">Samples</a>
UC2846NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2846N	<a href="#">Samples</a>
UC2846QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	UC2846Q	<a href="#">Samples</a>
UC2847DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2847DW	<a href="#">Samples</a>
UC2847DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2847DW	<a href="#">Samples</a>
UC2847N	NRND	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2847N	
UC3846DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3846DW	<a href="#">Samples</a>
UC3846DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3846DW	<a href="#">Samples</a>
UC3846DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3846DW	<a href="#">Samples</a>
UC3846DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3846DW	<a href="#">Samples</a>
UC3846J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	0 to 70	UC3846J	<a href="#">Samples</a>
UC3846N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3846N	<a href="#">Samples</a>
UC3846NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3846N	<a href="#">Samples</a>
UC3846Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	UC3846Q	<a href="#">Samples</a>
UC3846QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	UC3846Q	<a href="#">Samples</a>
UC3847DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3847DW	<a href="#">Samples</a>
UC3847J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
UC3847N	NRND	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3847N	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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● Catalog: [UC3846](#), [UC3847](#), [UC2846](#), [UC3846M](#), [UC3846](#)

● Enhanced Product: [UC1846-EP](#), [UC1846-EP](#)

- Military: [UC2846M](#), [UC1846](#), [UC1847](#)
- Space: [UC1846-SP](#), [UC1846-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2846DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2846DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

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