LP3985 Micropower, 150-mA Low-Noise Ultra-Low-Dropout CMOS Voltage Regulator

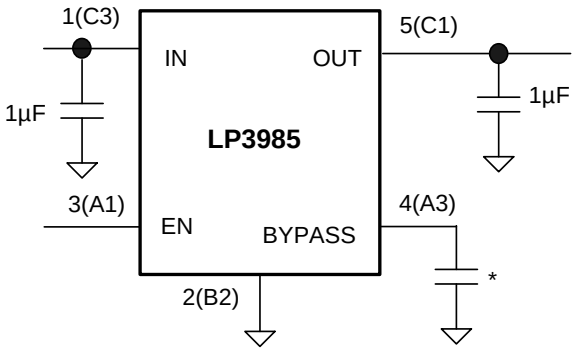
1 Features

- Input Voltage: 2.5 V to 6 V
- 100-mV Maximum Dropout with 150-mA Load
- 150-mA Verified Output
- 50-dB PSRR at 1 kHz at $V_{IN} = V_{OUT} + 0.2$ V
- ≤ 1.5-µA Quiescent Current when Shut Down
- Fast Turn-On time: 200 µs (typ.)
- 30-μV_{RMS} Output Noise (typical) over 10 Hz to 100 kHz
- −40°C to 125°C Junction Temperature Range for Operation
- 2.5-V, 2.6-V, 2.7-V, 2.8-V, 2.85-V, 2.9-V, 3-V, 3.1-V, 3.2-V, 3.3-V, 4.7-V, 4.75-V, 4.8-V and 5-V Outputs Standard
- Logic Controlled Enable
- Stable with Ceramic and High-Quality Tantalum Capacitors
- Fast Turnon
- Thermal Shutdown and Short-Circuit Current Limit

2 Applications

- CDMA Cellular Handsets
- Wideband CDMA Cellular Handsets
- GSM Cellular Handsets
- Portable Information Appliances

Simplified Schematic



Pin Numbers in parenthesis indicate DSBGA package.
* Optional Noise Reduction Capacitor.

3 Description

The LP3985 is designed for portable and wireless applications with demanding performance and space requirements. LP3985 performance is optimized for battery-powered systems to deliver ultra low noise, extremely low dropout voltage, and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

The LP3985 is stable with a small 1-µF ±30% ceramic or high-quality tantalum output capacitor. The DSBGA requires the smallest possible PC board area - the total application circuit area can be less than 2 mm x 2.5 mm, a fraction of a 1206 case size.

An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Fast startup time is achieved by utilizing an internal power-on circuit that actively pre-charges the bypass capacitor.

Power supply rejection is better than 50 dB at low frequencies and starts to roll off at 1 kHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery-powered wireless applications. It provides up to 150 mA, from a 2.5-V to 6-V input. The LP3985 consumes less than 1.5 µA in disable mode and has fast turn-on time less than 200 µs.

The LP3985 is available with fixed output voltages from 2.5 V to 5 V. Contact Texas Instruments Sales for specific voltage option needs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LP3985	DSBGA (5)	1.502 mm x 1.045 mm (MAX)
	SOT-23 (5)	2.90 mm x 1.60 mm (NOM)

(1) For all available packages, see the Package Option Addendum at the end of the datasheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision AD (October 2014) to Revision AE — **Page**

- Changed update pin names to TI nomenclature; replace *Handling Ratings* with *ESD Ratings* ... 1
- Deleted *Voltage Options* table - information in POA ... 1
- Added GND as type for ground pins ... 3
- Added *Thermal Considerations* sub-section ... 17

Changes from Revision AC (May 2013) to Revision AD — **Page**

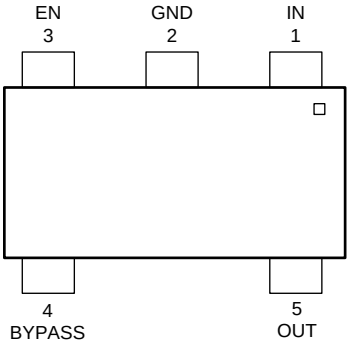
- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section; add new *Thermal Information* ... 1

Changes from Revision AB (May 2013) to Revision AC — **Page**

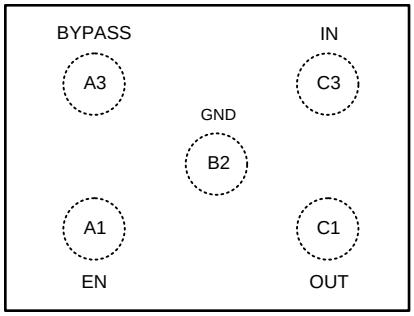
- Changed layout of National Data Sheet to TI format ... 20

5 Pin Configuration and Functions

DBV Package
5 Pin SOT-23
Top View



YZR Package
5 Pin DSBGA
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DSBGA NUMBER(1)	SOT-23 NUMBER		
BYPASS	A3	4	I/O	Optional bypass capacitor for noise reduction
EN	A1	3	I	Enable input logic, enable high
GND	B2	2	GND	Common ground
IN	C3	1	I	Input voltage of the LDO
OUT	C1	5	O	Output voltage of the LDO

(1) The pin numbering scheme for the DSBGA package was revised in April 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purposes, the obsolete numbering scheme had VEN as pin 1, GND as pin 2, VOUT as pin 3, VIN as pin 4, and BYPASS as pin 5.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

		MIN	MAX	UNIT
IN, EN		–0.3	6.5	V
OUT		−0.3	(V_{IN} + 0.3) < 6.5	
Junction temperature			150	°C
Lead temperature			235	
Pad temperature (4)			235	
Maximum power dissipation	SOT-23 (5)		364	mW
	DSBGA (5)		314	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Additional information on lead temperature and pad temperature can be found in Texas Instruments Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).
(5) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A)/R_{\theta JA}$,where T_J is the junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance. The 364-mW rating for SOT23-5 appearing under *Absolute Maximum Ratings* results from substituting the Absolute Maximum junction temperature, 150°C for T_J, 70°C for T_A, and 220°C/W for $R_{\theta JA}$. More power can be dissipated safely at ambient temperatures below 70°C . Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation can be increased by 4.5 mW for each degree below 70°C, and it must be derated by 4.5 mW for each degree above 70°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	2.5 (1)	6	V
V_{EN}	ON/OFF input voltage	0	V_{IN}	V
I_{OUT}	Output current		150	mA
T_J	Operating junction temperature	−40	125	°C

(1) Recommended minimum V_{IN} is the greater of 2.5-V or $V_{OUT(MAX)}$ + rated dropout voltage (max) for operating load current.

6.4 Thermal Information

THERMAL METRIC (1)		LP3985		UNIT
		SOT-23 (DBV)	DSBGA (YZR)	
		5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	255	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.8	0.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.6	107.9	
ψ_{JT}	Junction-to-top characterization parameter	3.1	0.5	
ψ_{JB}	Junction-to-board characterization parameter	31.1	107.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.5$ V, $C_{IN} = 1$ µF, $I_{OUT} = 1$ mA, $C_{OUT} = 1$ µF, $C_{BYPASS} = 0.01$ µF. Minimum (MIN) and Maximum (MAX) values apply over –40°C ≤ T_J ≤ 125°C and typical values are T_A = 25°C, unless otherwise indicated. (1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	I_{OUT} = 1 mA	–2 (3) –3		2 (3) 3	% of $V_{OUT(nom)}$
	Line regulation error	V_{IN} = ($V_{OUT(nom)}$ + 0.5 V) to 6 V, For 4.7-V to 5-V options For all other options	 –0.19 –0.1		 0.19 0.1	%/V
	Load regulation error (4)	I_{OUT} = 1 mA to 150 mA LP3985IM5 (SOT23-5)		0.0025	0.005	%/mA
		LP3985 (DSBGA)		0.0004	0.002	%/mA
	Output AC line regulation	$V_{IN} = V_{OUT(nom)} + 1$ V, I_{OUT} = 150 mA (Figure 1)		1.5		mV_{P-P}
PSRR	Power supply rejection ratio	$V_{IN} = V_{OUT(nom)} + 0.2$ V, f = 1 kHz, I_{OUT} = 50 mA (Figure 2)		50		dB
		$V_{IN} = V_{OUT(nom)} + 0.2$ V, f = 10 kHz, I_{OUT} = 50 mA (Figure 2)		40		dB
I_Q	Quiescent current	V_{EN} = 1.4 V, I_{OUT} = 0 mA For 4.7-V to 5-V options For all other options	 	100 85	165 150	µA
		V_{EN} = 1.4 V, I_{OUT} = 0 to 150 mA For 4.7-V to 5-V options For all other options	 	155 140	250 200	
		V_{EN} = 0.4 V		0.003	1.5	
	Dropout voltage (5)	I_{OUT} = 1 mA		0.4	2	mV
		I_{OUT} = 50 mA		20	35	mV
		I_{OUT} = 100 mA		45	70	mV
		I_{OUT} = 150 mA		60	100	mV
I_{SC}	Short circuit current limit	Output Grounded (Steady State)		600		mA
$I_{OUT(PK)}$	Peak output current	$V_{OUT} \geq V_{OUT(nom)} - 5\%$	300	550		mA
T_{ON}	Turnon time (6)	C_{BYPASS} = 0.01 µF		200		µs
e_n	Output noise voltage (7)	BW = 10 Hz to 100 kHz, C_{OUT} = 1 µF		30		μV_{RMS}
	Output noise density	C_{BP} = 0		230		nV/ $\sqrt{Hz}$
I_{EN}	Maximum input current at EN	V_{EN} = 0.4 V and V_{IN} = 6 V		±1		nA
V_{IL}	Maximum low-level input voltage at EN	V_{IN} = 2.5 V to 6 V			0.4	V
V_{IH}	Minimum high-level input voltage at EN	V_{IN} = 2.5 V to 6 V	1.4			V
TSD	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		°C

(1) All limits are verified. All electrical characteristics having room-temperature limits are tested during production with T_A = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage, which is labeled $V_{OUT(NOM)}$, is the desired voltage option.
(3) T_A = 25°C only.
(4) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(5) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.
(6) Turnon time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.
(7) The output noise varies with output voltage option. The 30 μV_{RMS} is measured with 2.5-V voltage option. To calculate an approximated output noise for other options, use the equation: (30μV_{RMS})(X)/2.5, where X is the voltage option value.

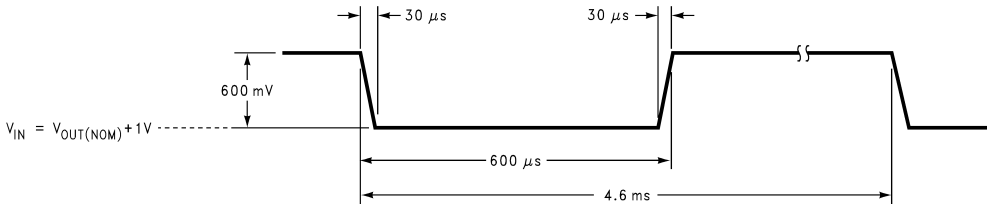


Figure 1. Line Transient Input Test Signal

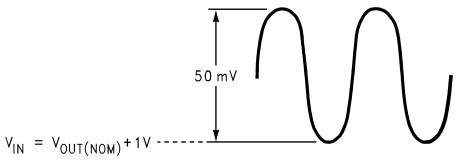


Figure 2. PSRR Input Test Signal

6.6 Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $C_{BYPASS} = 0.01$ µF, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

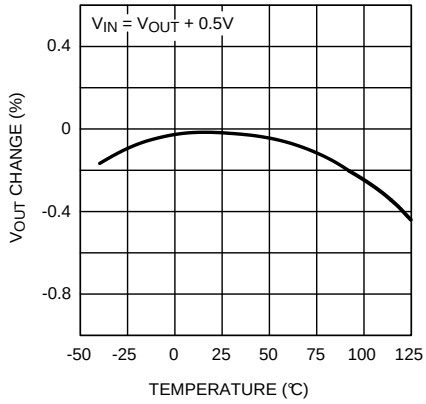


Figure 3. Output Voltage Change vs Temperature

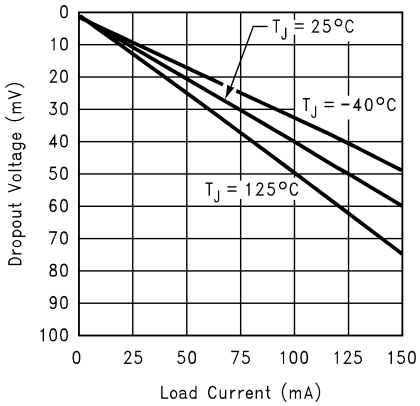


Figure 4. Dropout Voltage vs Load Current

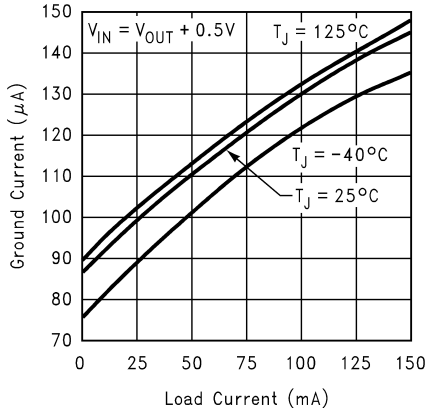


Figure 5. Ground Current vs Load Current

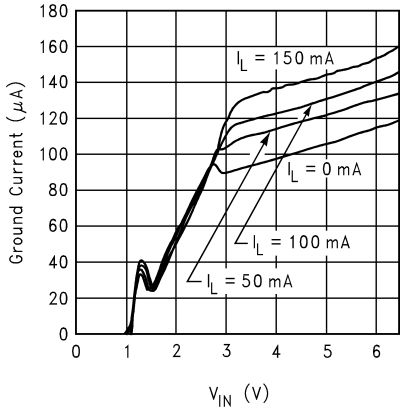


Figure 6. Ground Current vs V_{IN} at 25°C

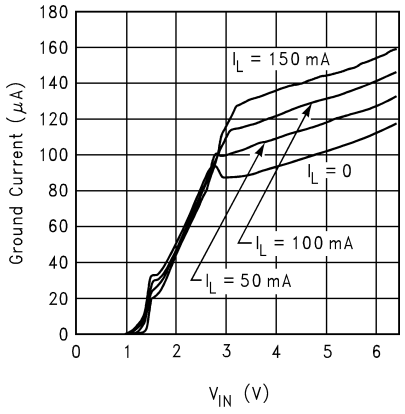


Figure 7. Ground Current vs V_{IN} at −40°C

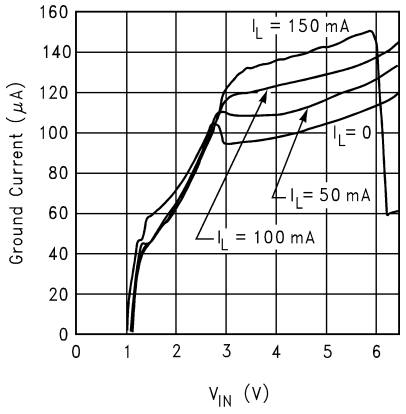


Figure 8. Ground Current vs V_{IN} at 125°C

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $C_{BYPASS} = 0.01$ µF, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

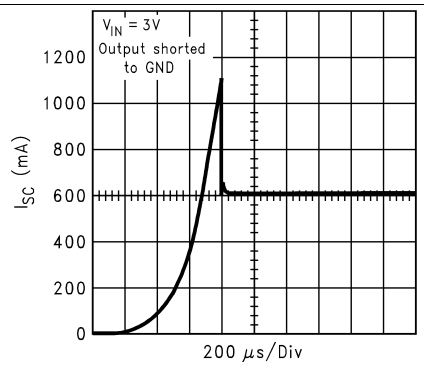


Figure 9. Short Circuit Current (DSBGA)

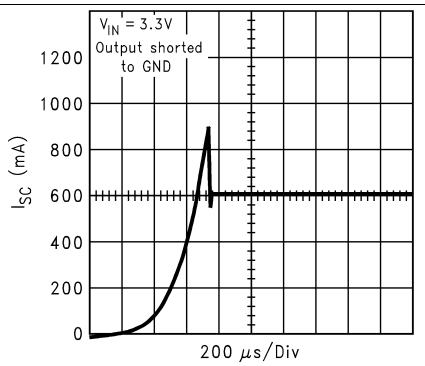


Figure 10. Short Circuit Current (DSBGA)

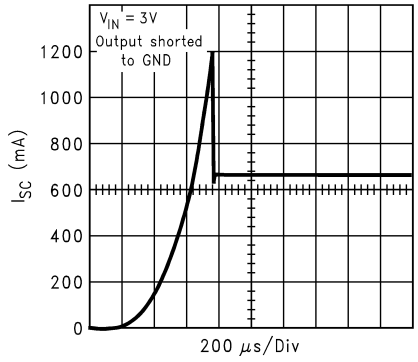


Figure 11. Short Circuit Current (SOT)

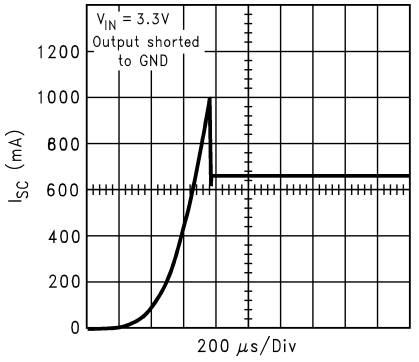


Figure 12. Short Circuit Current (SOT)

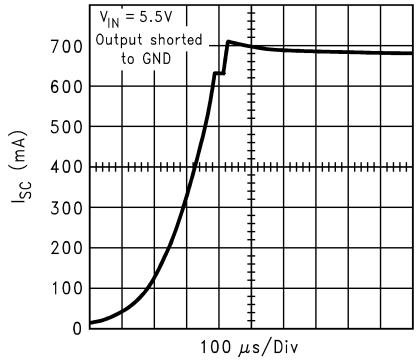


Figure 13. Short Circuit Current (SOT)

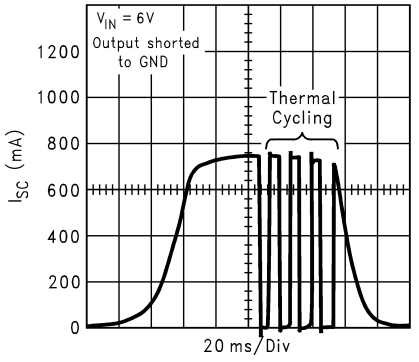


Figure 14. Short Circuit Current (SOT)

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $C_{BYPASS} = 0.01$ µF, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

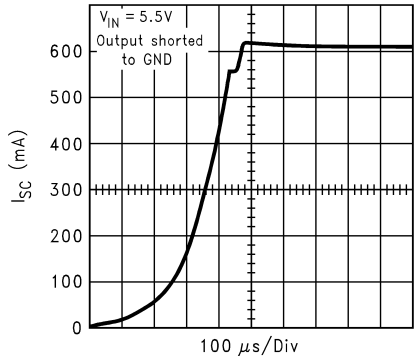


Figure 15. Short Circuit Current (DSBGA)

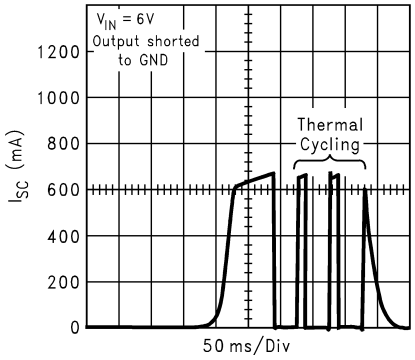


Figure 16. Short Circuit Current (DSBGA)

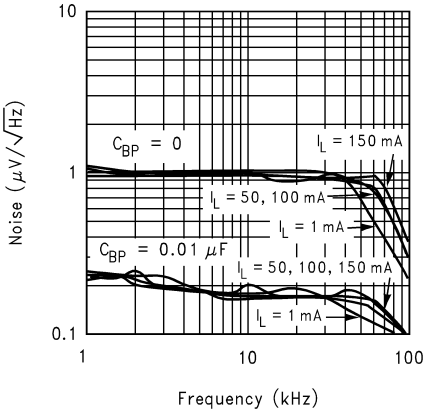
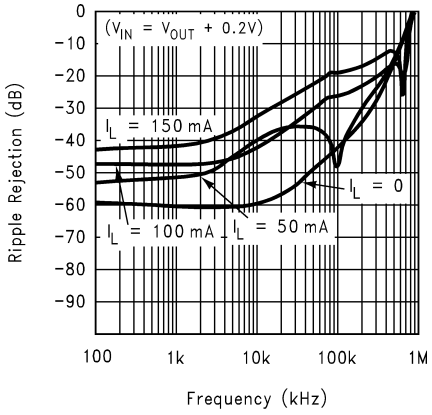
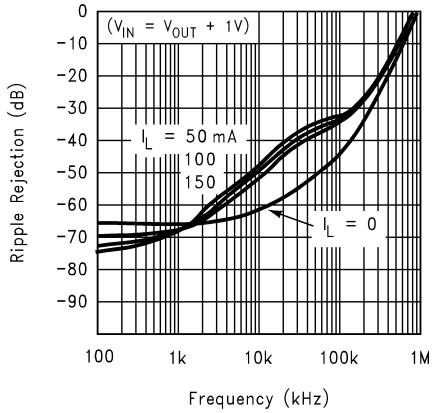


Figure 17. Output Noise Spectral Density



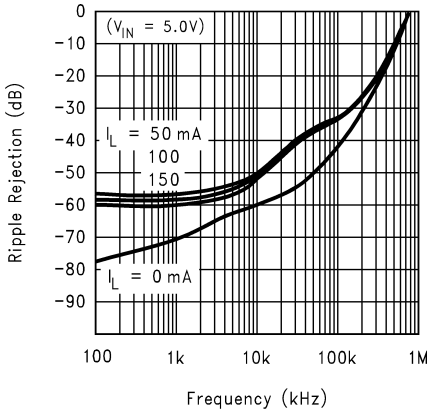
$V_{IN} = V_{OUT} + 0.2$ V

Figure 18. Ripple Rejection



$V_{IN} = V_{OUT} + 1$ V

Figure 19. Ripple Rejection

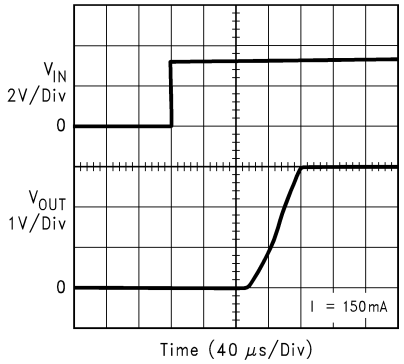


$V_{IN} = 5$ V

Figure 20. Ripple Rejection

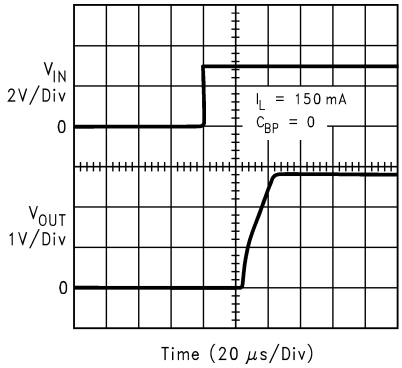
Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $C_{BYPASS} = 0.01$ µF, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.



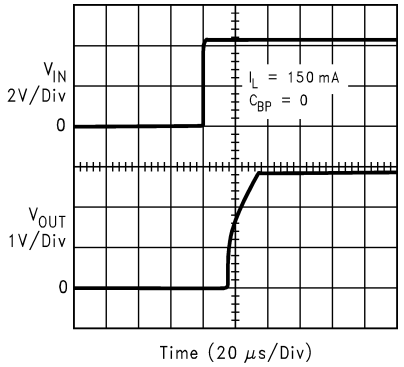
$V_{IN} = V_{OUT} + 0.2$ V

Figure 21. Start-up Time



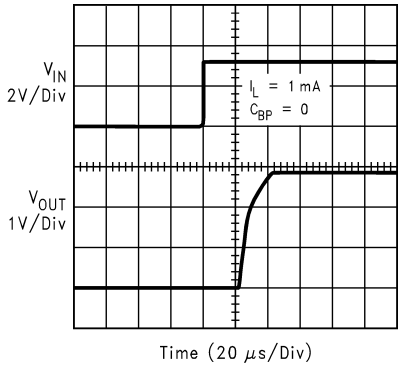
$V_{IN} = V_{OUT} + 0.2$ V

Figure 22. Start-up Time



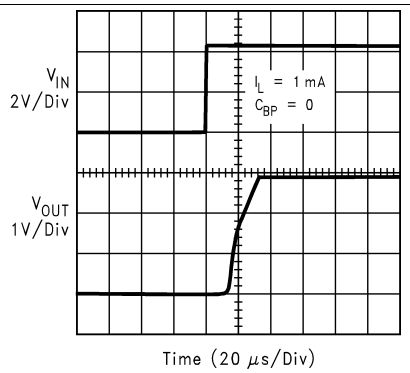
$V_{IN} = 4.2$ V

Figure 23. Start-up Time



$V_{IN} = V_{OUT} + 0.2$ V

Figure 24. Start-up Time



$V_{IN} = 4.2$ V

Figure 25. Start-up Time

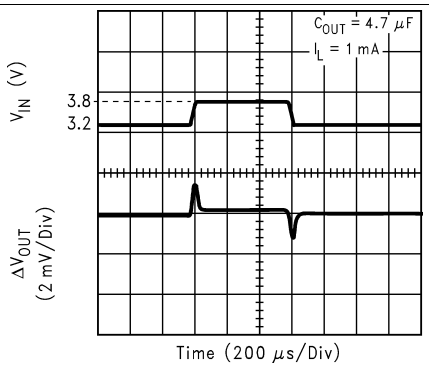


Figure 26. Line Transient Response

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $C_{BYPASS} = 0.01$ µF, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

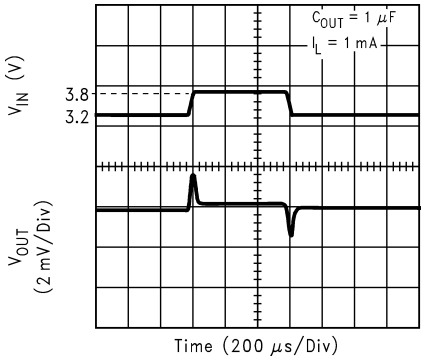
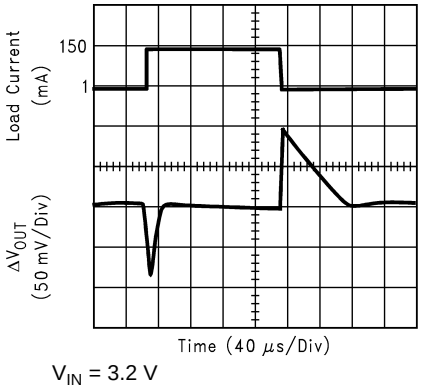
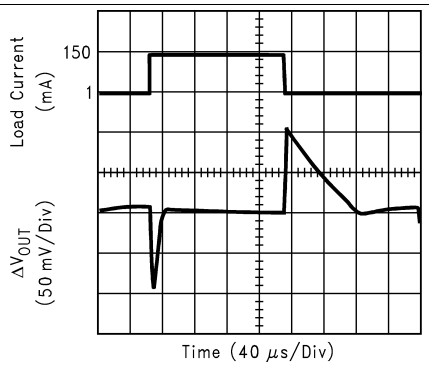


Figure 27. Line Transient Response



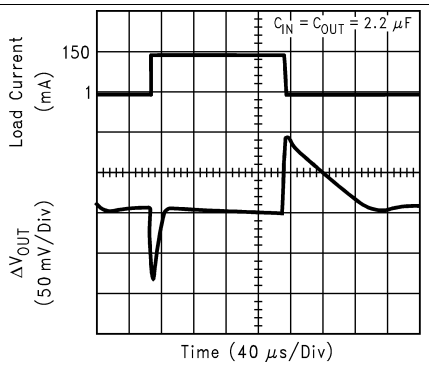
V_{IN} = 3.2 V

Figure 28. Load Transient Response



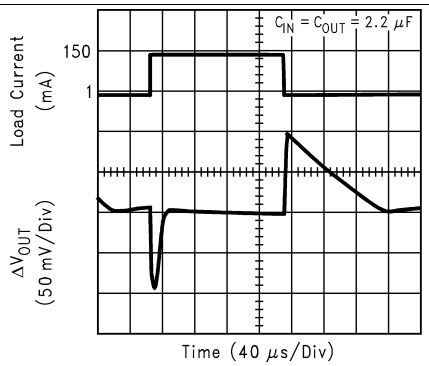
V_{IN} = 4.2 V

Figure 29. Load Transient Response



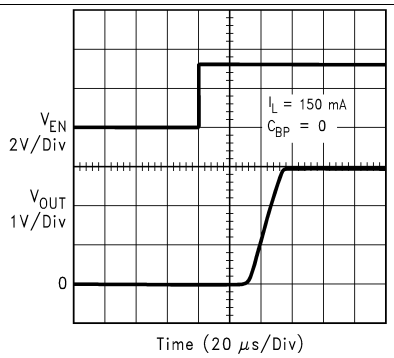
V_{IN} = 3.2 V

Figure 30. Load Transient Response



V_{IN} = 4.2 V

Figure 31. Load Transient Response

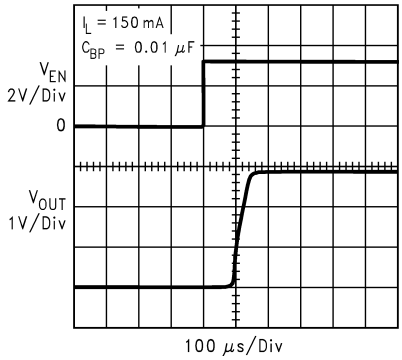


$V_{IN} = V_{OUT} + 0.2$ V

Figure 32. Enable Response

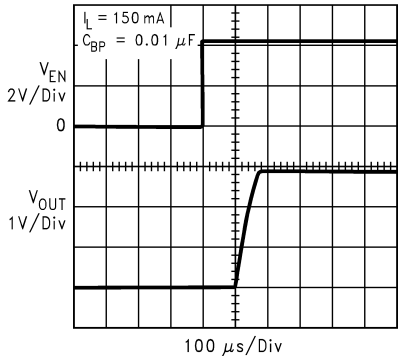
Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $C_{BYPASS} = 0.01$ µF, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.



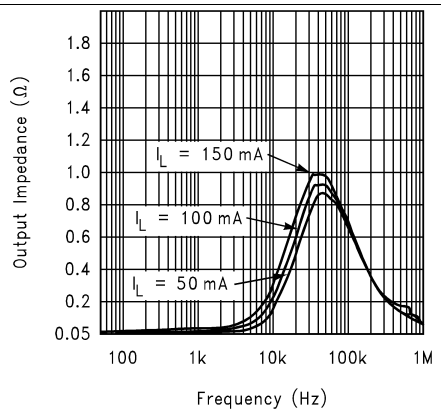
$V_{IN} = V_{OUT} + 0.2$ V

Figure 33. Enable Response



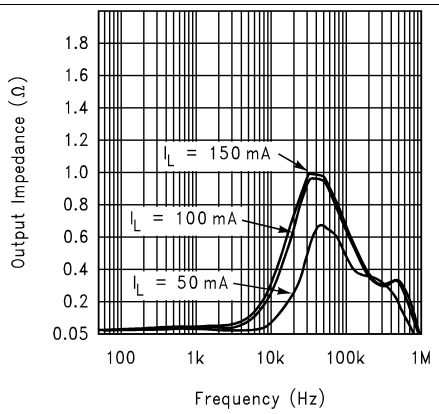
$V_{IN} = 4.2$ V

Figure 34. Enable Response



$V_{IN} = 4.2$ V

Figure 35. Output Impedance



$V_{IN} = V_{OUT} + 0.2$ V

Figure 36. Output Impedance

7 Detailed Description

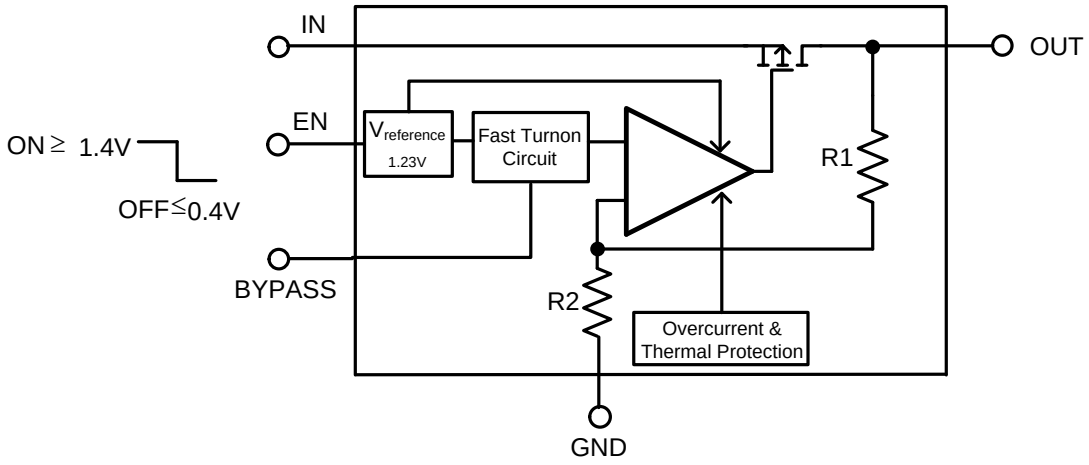
7.1 Overview

The LP3985 family of fixed-output, ultra-low-dropout and low noise regulators offers exceptional, cost-effective performance for battery powered applications. Available in output voltages from 2.5 V to 5 V, the family is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are also included.

The LP3985 contains several features to facilitate battery powered designs:

- Multiple voltage options
- Low dropout voltage, typical dropout of 60 mV at 150-mA load current
- Low quiescent current and low ground current, typically 140 µA at 150-mA load, and 85-µA at 0-mA load
- A shutdown feature is available, allowing the regulator to consume only 0.003 µA typically when the EN pin is pulled low
- Overtemperature protection and overcurrent protection circuitry is designed to safeguard the device during unexpected conditions
- Enhanced stability: The LP3985 is stable with output capacitor, which allows the use of ceramic capacitors on the output
- Power supply rejection is better than 50 dB at low frequencies and starts to roll off at 1 kHz.
- Low noise: A BYPASS pin allows for low-noise operation, with a typical output noise of 30 μV_{RMS}, with the use of a 10-nF bypass capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 No-Load Stability

The LP3985 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

7.3.2 On/Off Input Operation

The LP3985 is turned off by pulling the EN pin low, and turned on by pulling it high. If this feature is not used, the EN pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon/turnoff voltage thresholds listed in *Electrical Characteristics* under V_{IL} and V_{IH}.

Feature Description (continued)

7.3.3 Fast On-Time

The LP3985 output is turned on after V_{REF} voltage reaches its final value (1.23 V, nominal). To speed up this process, the noise reduction capacitor at the BYPASS pin is charged with an internal 70-µA current source. The current source is turned off when the bandgap voltage reaches approximately 95% of its final value. The turnon time is determined by the time constant of the bypass capacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the bypass capacitor.

7.4 Device Functional Modes

7.4.1 Operation with $V_{OUT(TARGET)}$ + 0.3 V ≤ V_{IN} ≤ 6 V

The device operates if the input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 0.3 V. At input voltages below the minimum V_{IN} requirement, the devices does not operate correctly, and output voltage may not reach target value.

7.4.2 Operation Using the EN Pin

If the voltage on the EN pin is less than 0.4 V, the device is disabled, and in this state shutdown current does not exceed 1.5 µA. Raising V_{EN} above 1.4 V initiates the start-up sequence of the device.

8 Application and Implementation

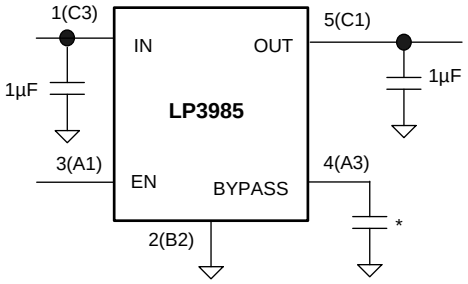
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3985 can provide 150-mA output current with 2.5-V to 6-V input. It is stable with a small 1-µF ±30% ceramic or high-quality tantalum output capacitor. The DSBGA requires the smallest possible PC board area – the total application circuit area can be less than 2 mm x 2.5 mm, a fraction of a 1206 case size. An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Fast startup time is achieved by utilizing an internal power-on circuit that actively pre-charges the bypass capacitor. Typical output noise is 30 μV_{RMS} at frequencies from 10 Hz to 100 kHz. Typical power supply rejection is 50 dB at 1 kHz.

8.2 Typical Application



Pin Numbers in parenthesis indicate DSBGA package.
* Optional Noise Reduction Capacitor.

Figure 37. LP3985 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input voltage	4.2 V, ±10% provided by the DC-DC converter switching at 1 MHz
Output voltage	3 V, ±5%
Output current	150 mA (maximum)
RMS noise, 10 Hz to100 kHz	30 μV_{RMS}
PSRR at 1 kHz	50 dB

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, the LP3985 requires external capacitors for regulator stability. The LP3985 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.2 Input Capacitor

An input capacitance of approximately 1 µF is required between the LP3985 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. A ceramic capacitor is recommended although a good quality tantalum or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain within the operational range over the full range of temperature and operating conditions.

8.2.2.3 Output Capacitor

Correct selection of the output capacitor is important to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC-bias, frequency and temperature. Unstable operation will result if the capacitance drops below the minimum specified value. (See the next section Capacitor Characteristics).

The LP3985 is designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (dialectric type X7R) with ESR between 5 mΩ to 500 mΩ is suitable in the LP3985 application circuit. X5R capacitors may be used but have a narrower temperature range. With these and other capacitor types (Y5V, Z6U) that may be used, selection is dependant on the range of operating conditions and temperature range for that application. (see *Capacitor Characteristics*).

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

It is also recommended that the output capacitor be placed within 1 cm from the output pin and returned to a clean ground line.

8.2.2.4 Capacitor Characteristics

The LP3985 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive, and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3985.

For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general. As an example Figure 38 shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC Bias condition the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table (0.7 µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (for example, 0402) may not be suitable in the actual application.

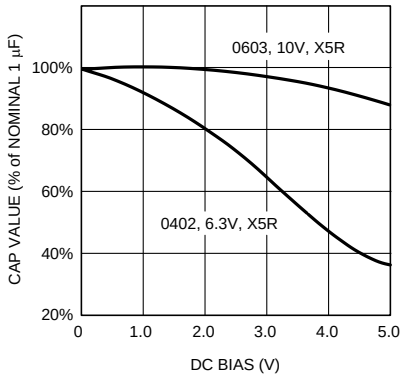


Figure 38. Graph Showing A Typical Variation In Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to 125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to 85°C. Most large value ceramic capacitors (around 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

8.2.2.5 Noise Bypass Capacitor

Connecting a 0.01-µF capacitor between the CBYPASS pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the band gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDOs, addition of a noise reduction capacitor does not effect the load transient response of the device.

8.2.2.6 Thermal Considerations

CAUTION

Due to the limited power dissipation characteristics of the available SOT-23 (DBV) and DSBGA (YZR) packages, all possible combinations of output current (I_{OUT}), input voltage (VIN), output voltage (V_{OUT}), and ambient temperatures (T_A) cannot be ensured.

Power dissipation, P_D is calculated from the following formula: $P_D = ((V_{IN} – V_{OUT}) \times I_{OUT})$.

The LP3985 regulator has internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the recommended maximum operating junction temperature is 125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices. Example: Given an output voltage of 3.3 V, an input voltage range of 4 V to 6 V, a maximum output current of 100 mA, and a maximum ambient temperature of 50°C, what is the maximum operating junction temperature? The power dissipated by the device is found using the formula:

$$P_{D(MAX)} = ((V_{IN(MAX)} – V_{OUT}) \times I_{OUT(MAX)}) \quad (1)$$

where

- $I_{OUT(MAX)}$ = 100 mA
- $V_{IN(MAX)}$ = 6 V
- V_{OUT} = 3.3 V

For example, $P_{D(MAX)}$ = ((6 V – 3.3 V) × 100 mA) = 0.27 W.

Using the 5-pin SOT-23 (DBV) package, the LP3985 junction-to-ambient thermal resistance (RθJA) has a rating of 220°C/W using the standard JEDEC JESD51-7 PCB (High-K) circuit board. The junction temperature rise above ambient is found using the formula:

$$T_{RISE} = P_{D(MAX)} \times R_{\theta JA};$$

for example, $T_{J(MAX)}$ = 50°C + 59.4°C = 109.4°C.

8.2.3 Application Curves

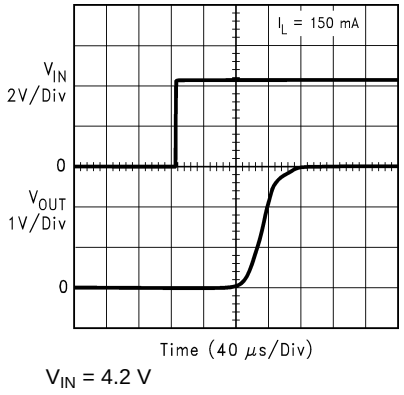


Figure 39. Start-up Time

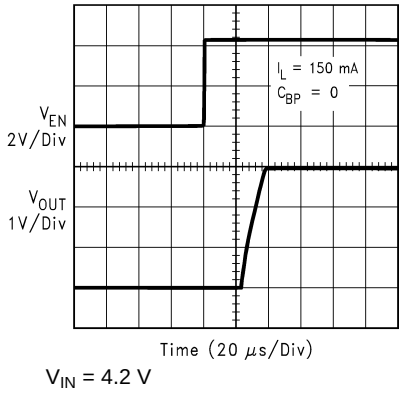


Figure 40. Enable Response

9 Power Supply Recommendations

The LP3985 is designed to operate from an input voltage supply range between 2.5 V and 6 V. The input-voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Examples

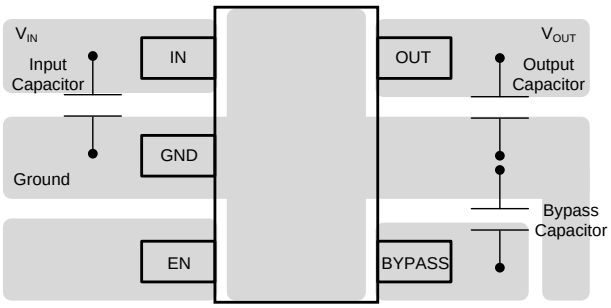


Figure 41. LP3985 SOT-23 Package Typical Layout

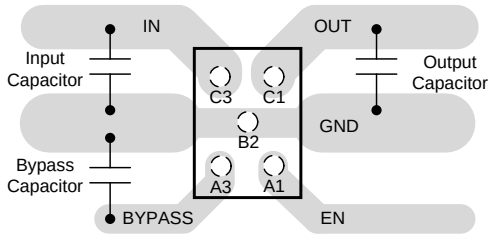


Figure 42. LP3985 DSBGA Package Typical Layout

10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques which are detailed in Texas Instruments Application Note 1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009). Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, it should be noted that the pad style which must be used with the 5-bump package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct sunlight will cause mis-operation of the device. Light sources such as halogen lamps can effect electrical performance if brought near to the device.

DSBGA Light Sensitivity (continued)

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A DSBGA test board was brought to within 1 cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).
- Texas Instruments Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3985IM5-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LCSB	
LP3985IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCSB	Samples
LP3985IM5-2.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCUB	Samples
LP3985IM5-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCJB	Samples
LP3985IM5-2.9/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCYB	Samples
LP3985IM5-3.0	NRND	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	LCRB	
LP3985IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCRB	Samples
LP3985IM5-3.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDPB	Samples
LP3985IM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LDQB	
LP3985IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDQB	Samples
LP3985IM5-4.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDRB	Samples
LP3985IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDSB	Samples
LP3985IM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCSB	Samples
LP3985IM5X-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCJB	Samples
LP3985IM5X-285/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCXB	Samples
LP3985IM5X-3.0	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	LCRB	
LP3985IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCRB	Samples
LP3985IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDQB	Samples
LP3985IM5X-4.7/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDRB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3985IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDSB	Samples
LP3985ITL-2.5/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-2.6/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-2.7/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-2.8/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-2.9/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-285/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-3.0/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-3.1/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-3.3/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITL-4.8/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		5	Samples
LP3985ITL-5.0/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITLX-2.5/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITLX-2.7/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITLX-2.8/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITLX-285/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITLX-3.0/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITLX-3.1/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3985ITLX-3.3/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP3985ITLX-5.0/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

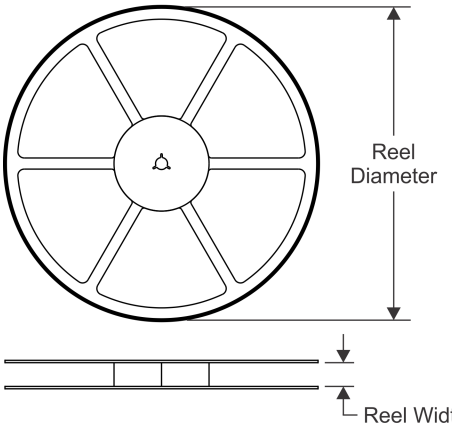
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

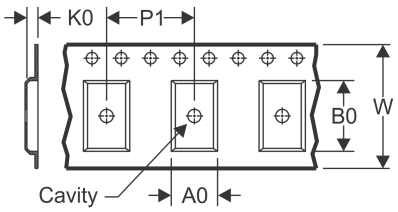
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

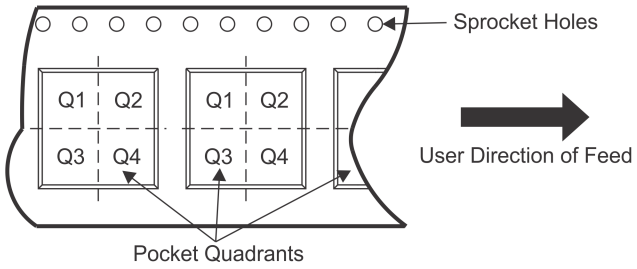


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

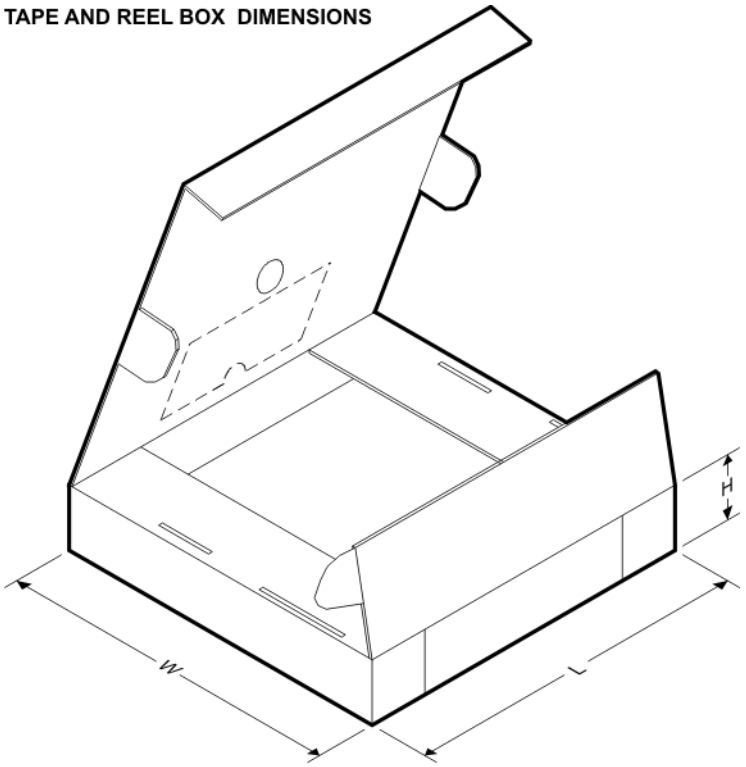


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3985IM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-3.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-4.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5X-285/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5X-3.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985IM5X-4.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3985ITL-2.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-2.6/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-2.7/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-2.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-2.9/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-285/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-3.0/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-3.1/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-3.3/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-4.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITL-5.0/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-2.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-2.7/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-2.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-285/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-3.0/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-3.1/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-3.3/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3985ITLX-5.0/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1

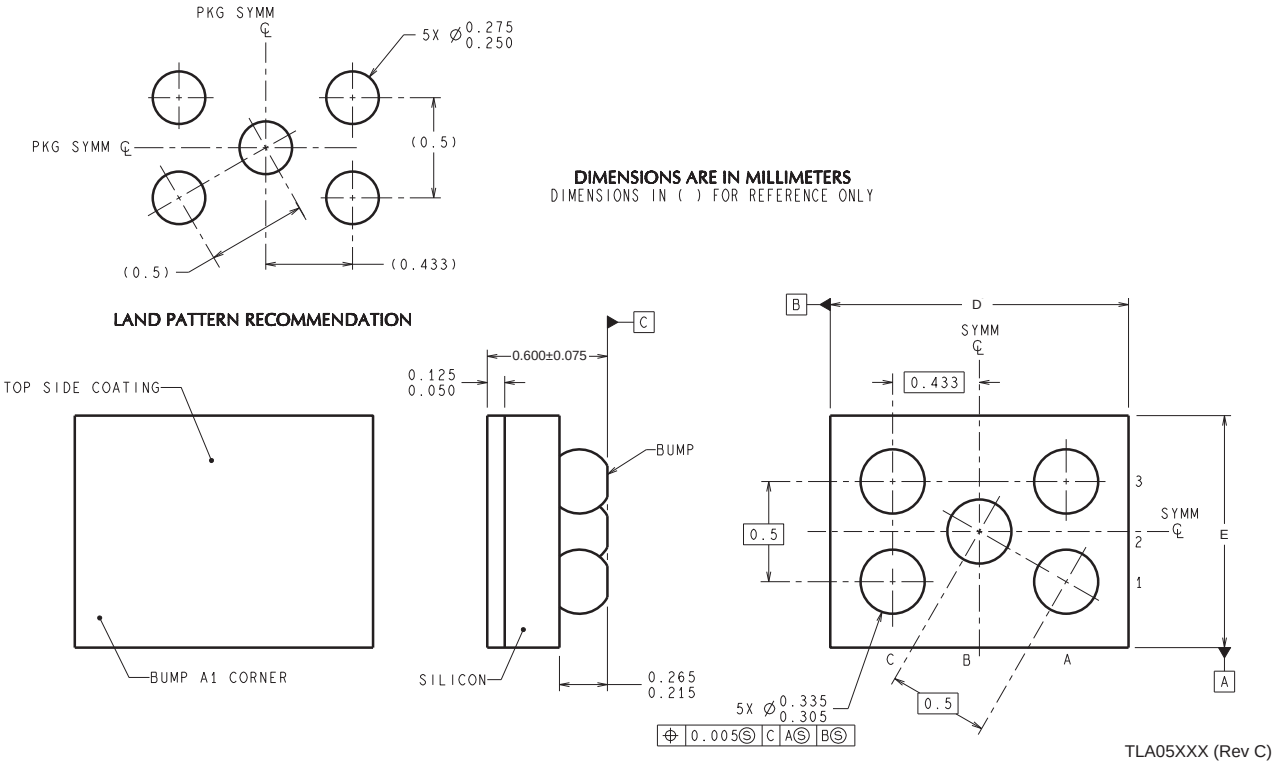
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3985IM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-2.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-2.9/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-3.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-4.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985IM5X-285/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985IM5X-3.0	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985IM5X-4.7/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3985ITL-2.5/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-2.6/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-2.7/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-2.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-2.9/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-285/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-3.0/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-3.1/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-3.3/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-4.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITL-5.0/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3985ITLX-2.5/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3985ITLX-2.7/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3985ITLX-2.8/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3985ITLX-285/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3985ITLX-3.0/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3985ITLX-3.1/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3985ITLX-3.3/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3985ITLX-5.0/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0

YZR0005



D: Max = 1.502 mm, Min =1.441 mm

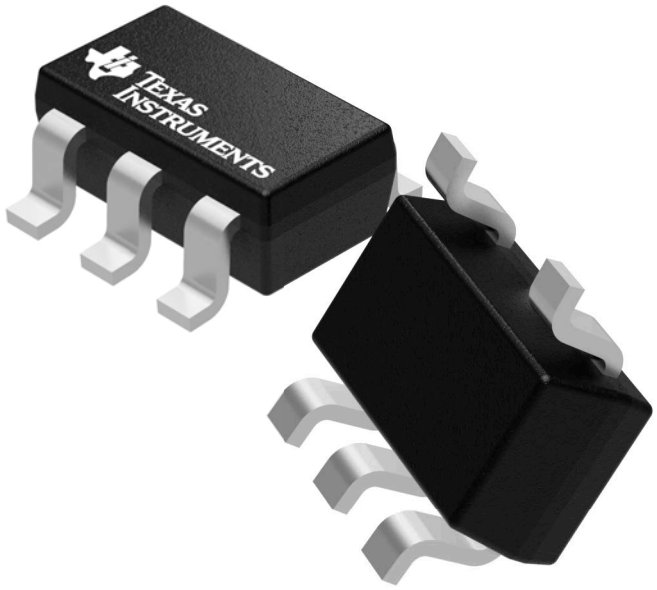
E: Max = 1.045 mm, Min =0.984 mm

4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



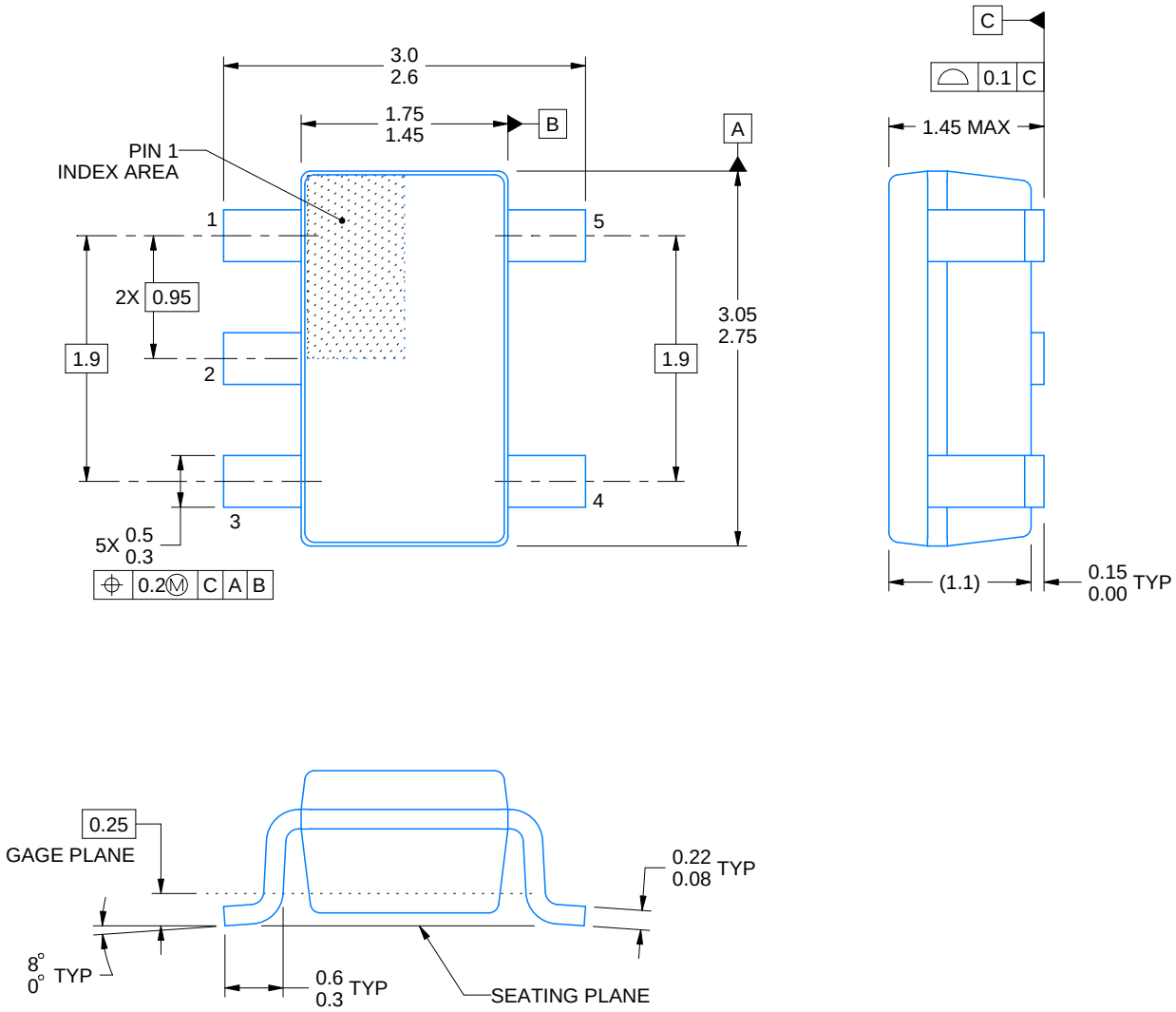
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

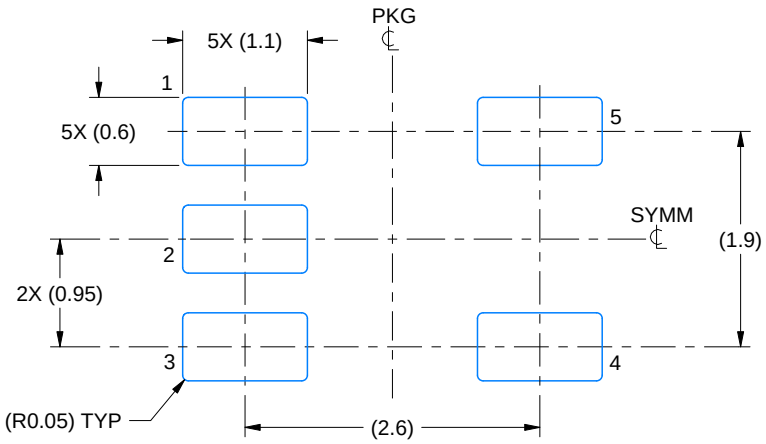
SMALL OUTLINE TRANSISTOR



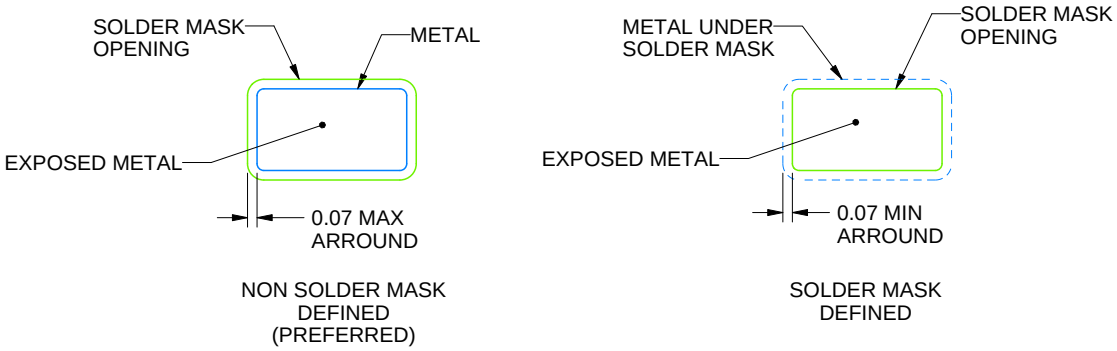
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

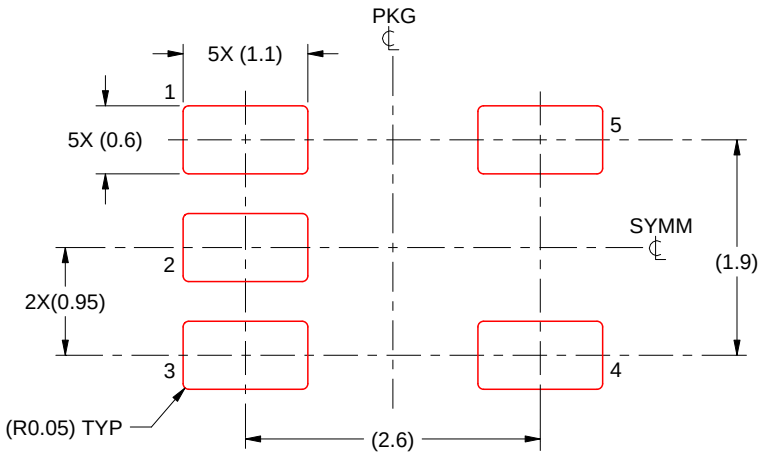


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

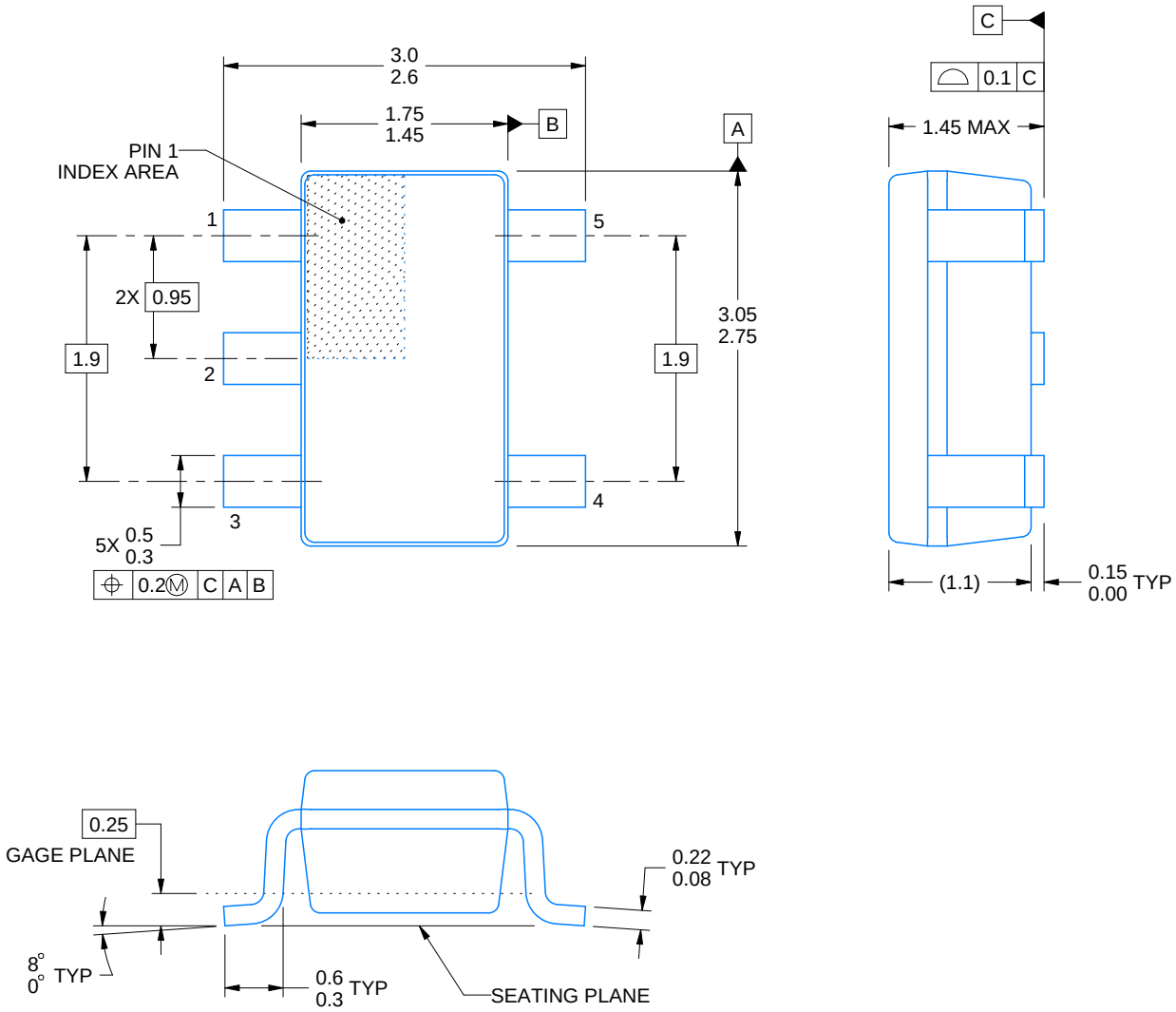
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

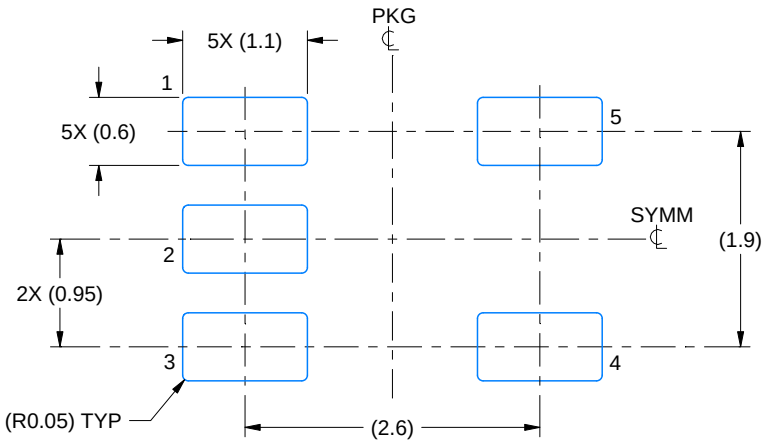
SMALL OUTLINE TRANSISTOR



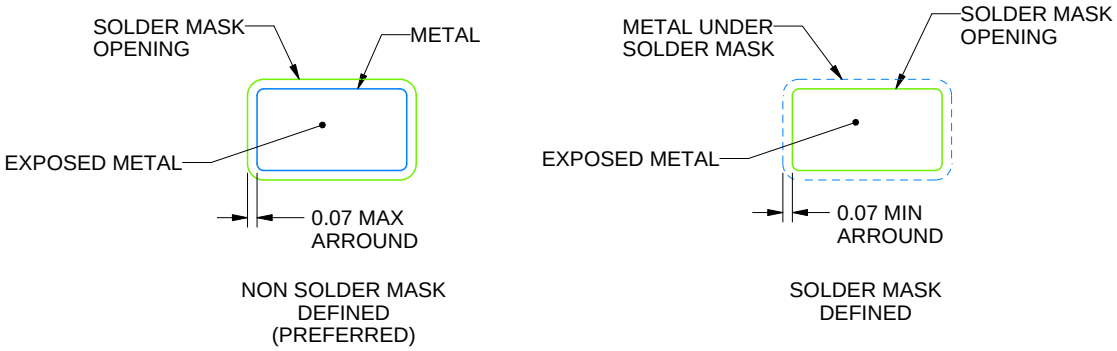
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

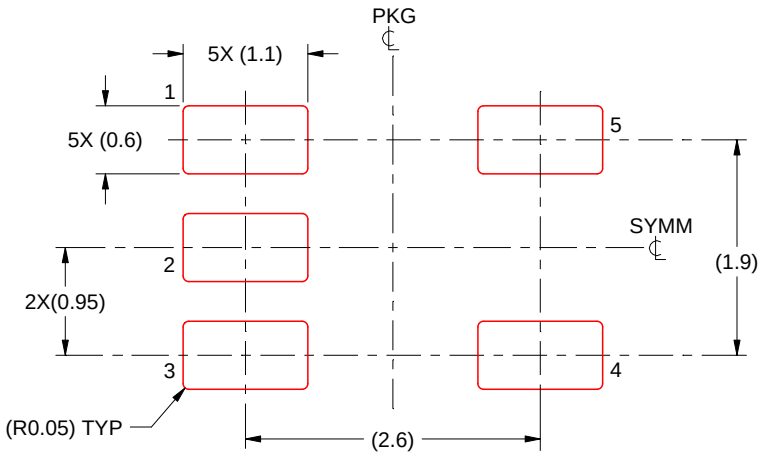


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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