Commercial and Industrial Consumer DDR 512Mb SDRAM

Features

- **JEDEC DDR Compliant**
  - Differential clock inputs (CK and $\overline{CK}$)
  - DLL aligns DQ and DQS transition with CK transitions
  - 2n Prefetch Architecture
  - DQS is edge-aligned with data for reads and center-aligned with data for WRITEs
  - DQ and DM referenced to both edges of DQS
  - tRAS lockout (tRAP = tRCD)
- **Signal Integrity**
  - Configurable DS for system compatibility
- **Data Integrity**
  - Auto Refresh Mode
  - Self Refresh Mode
- **Power Saving Mode**
  - Power Down Mode
- **Interface and Power Supply**
  - SSTL_2 compatible (All inputs)
  - SSTL_2, Class II compatible (All outputs)
  - VDD/VDDQ=2.5V±0.2V (DDR-333)
  - VDD/VDDQ=2.6V±0.1V (DDR-400)

Options

- **Speed Grade (CL-TRCD-TRP) [1,2]**
  - 400 Mbps / 3-3-3
- **Temperature Range (T_A)**
  - Commercial Grade = 0℃~70℃
  - Industrial Grade = -40℃~85℃

Programmable Functions

- **CAS Latency (2.5, 3)**
- **Burst Length (2, 4, 8)**
- **Burst Type (Sequential, Interleaved)**
- **Driver Strength (Normal, Weak)**

Packages / Density Information

Lead-free RoHS compliance and Halogen-free

512Mb (Org. / Package)		Length x Width[5] (mm)	Pin pitch (mm)
64M x 8	66 pin TSOPII	22.22 x 10.16	0.65
32M x 16			

Density and Addressing

Item	512Mb	
Organization	64M x 8	32M x 16
Number of banks	4	4
Bank Address	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP
tRFC(ns) [3]	72	72
tREFI (μs) [4]	7.8	7.8
Row Address	A[12:0]	A[12:0]
Column Address	A11, A[9:0]	A[9:0]

NOTE 1 The timing specification of high speed bin is backward compatible with low speed bin.
NOTE 2 The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.
NOTE 3 Violating tRFC specification will induce malfunction. tRFC spec is 70ns under DDR-400 operation and 72ns under DDR-333 operation.
NOTE 4 tREFI values for all bank refresh is within temperature specification.
NOTE 5 It excludes the pin.

Descriptions

Nanya 512Mb SDRAMs is a high-speed CMOS Double Data Rate SDRAM containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

It uses a double-data-rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access effectively consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

It operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going high and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4, or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving Power Down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

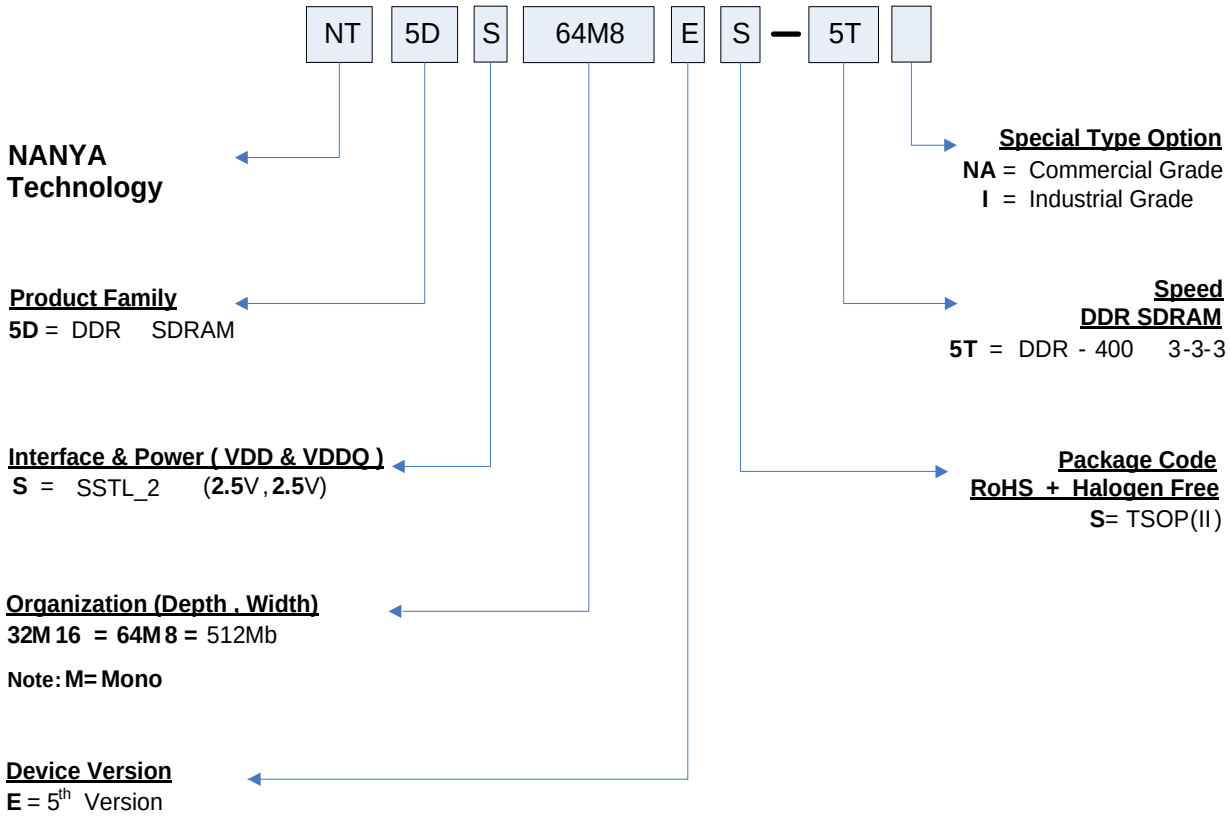
Ordering Information

Commercial Grade				
Organization	**Part Number**	**Package**	**Speed [1]**	
			Date Rate (Mbps)	**CL-TRCD-TRP**
64M x 8	NT5DS64M8ES-5T	66 pin TSOP-II	DDR-400	3-3-3
32M x 16	NT5DS32M16ES-5T		DDR-400	3-3-3

Industrial Grade				
Organization	**Part Number**	**Package**	**Speed [1]**	
			Date Rate (Mbps)	**CL-TRCD-TRP**
64M x 8	NT5DS64M8ES-5TI	66 pin TSOP-II	DDR-400	3-3-3
32M x 16	NT5DS32M16ES-5TI		DDR-400	3-3-3

NOTE 1: The timing specification of high speed bin is backward compatible with low speed bin.

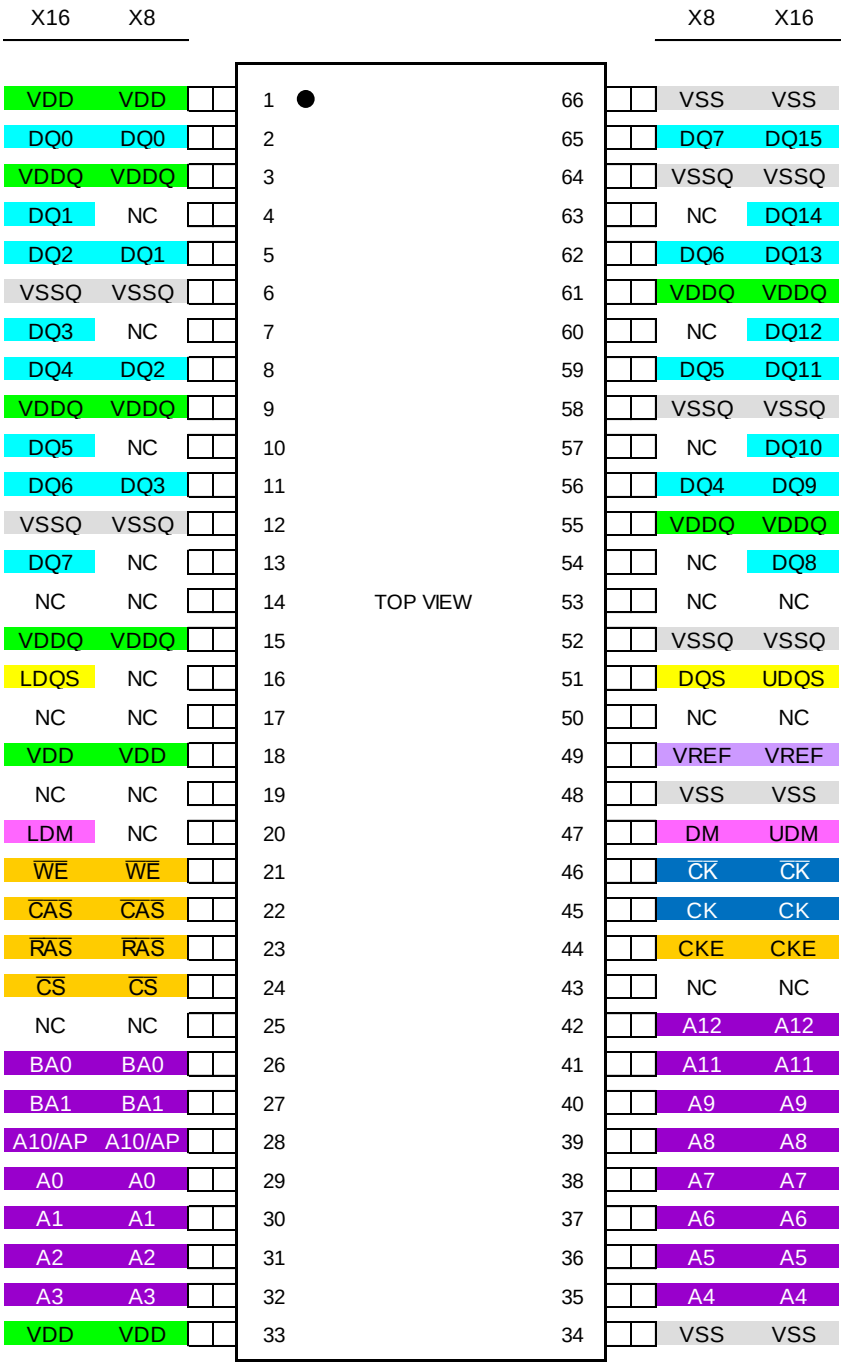
NANYA Component Part Numbering Guide



Pin Configuration (X8 / X16)

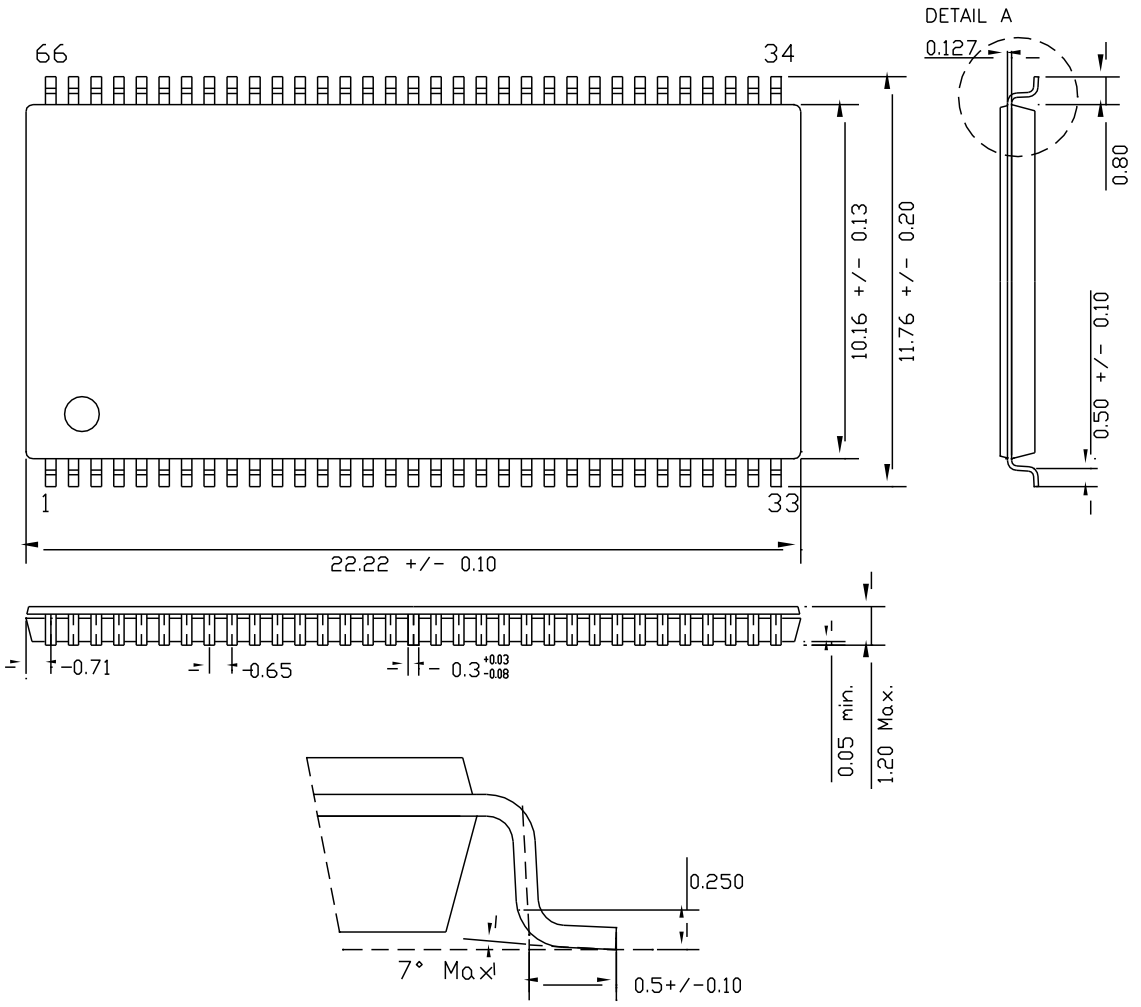
< TOP View>

See the balls through the package



Package Outline Drawing for 400 mil TSOP II (X8 / X16)

Unit: mm



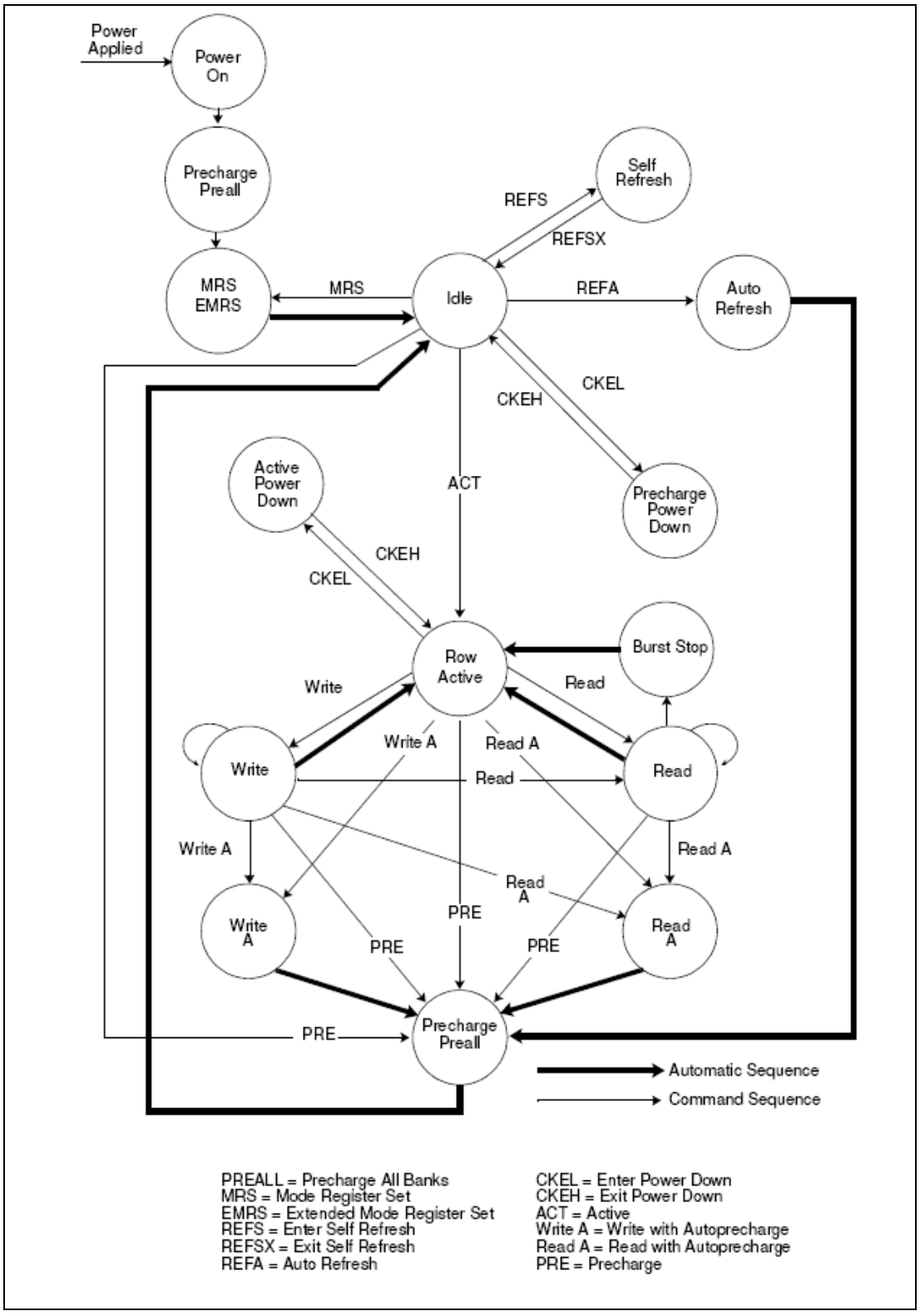
Pin Descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF-REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, CK and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied upon 1st power up. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. The standard pinout includes one CKE pin.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (LDM, UDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the X16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15. DM may be driven high, low, or floating during READs.
BA0 – BA1	Input	**Bank Address Inputs:** Defines to which bank an Active, Read, Write or Pre-charge command is being applied. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
A0 – A12	Input	**Address Inputs:** Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command.
DQ	Input/output	**Data Bus:** Inputs/Output
DQS (LDQS, UDQS)	Input/output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15.
NC	-	**No Connect:** No internal electrical connection is present.

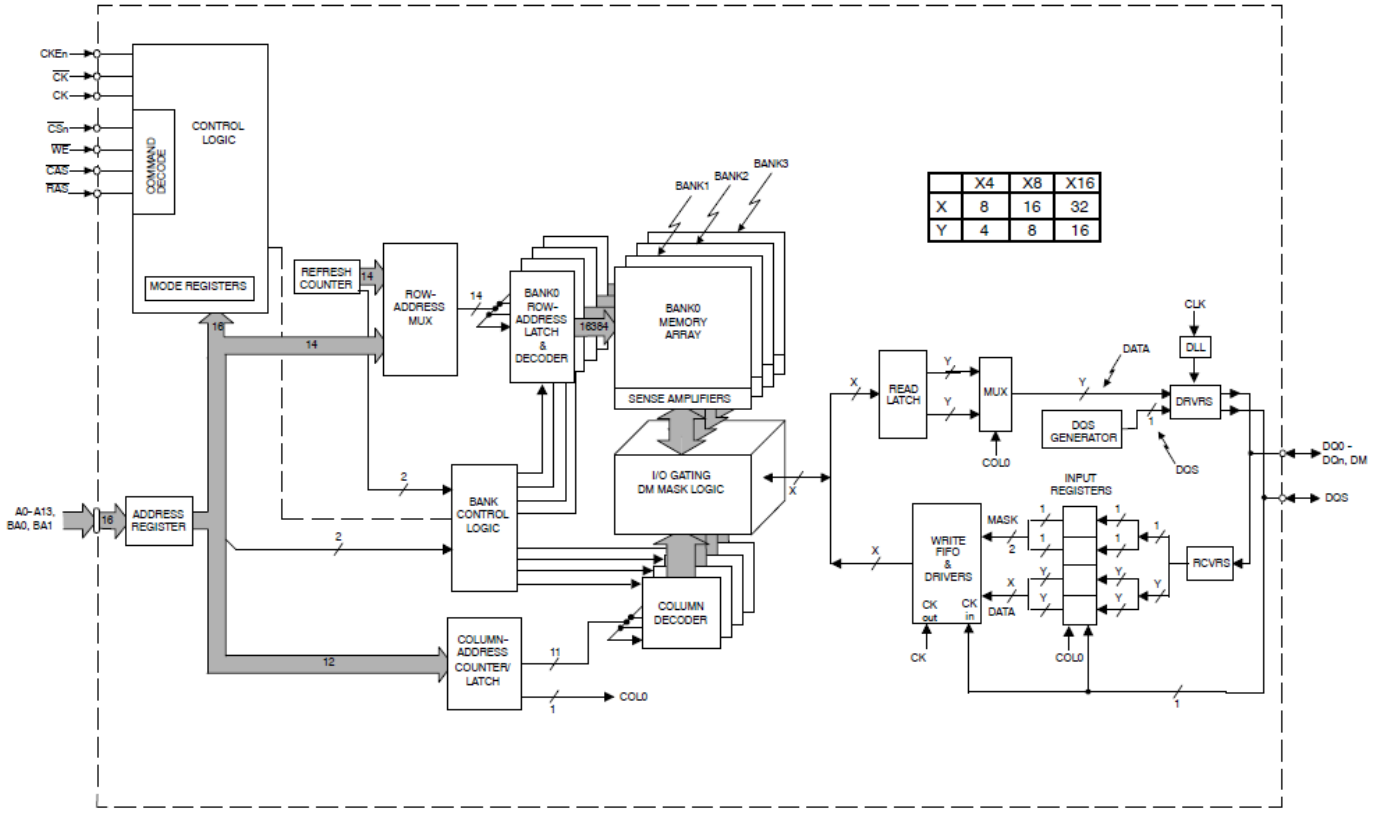
V_{DDQ}	Supply	**DQ Power Supply:** 2.5V ± 0.2V (DDR-333); VDD=VDDQ=2.6V±0.1V (DDR-400)
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.2V (DDR-333); VDD=VDDQ=2.6V±0.1V (DDR-400)
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage**

NOTE: The signal may show up in a different symbol but it indicates the same thing. e.g., /CK = CK# = $\overline{CK}$ = CKb, /CS = CS# = $\overline{CS}$ = CSb.

Simplified State Diagram



Function Block Diagram



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Note 3: Not all address inputs are used on all densities.

Functional Descriptions

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

It uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

Only one of the following two conditions must be met.

• No power sequencing is specified during power up or power down given the following criteria:

VDD and VDDQ are driven from a single power converter output, and

VTT is limited to 1.35V, and

VREF tracks VDDQ /2

OR

• The following relationships must be followed:

VDDQ is driven after or with VDD such that VDDQ < VDD + 0.3V

VTT is driven after or with VDDQ such that VTT < VDDQ + 0.3V

VREF is driven after or with VDDQ such that VREF < VDDQ + 0.3V

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200μs delay prior to applying an executable command.

Once the 200μs delay has been satisfied, a Deselect or NOP command should be applied, and CKE must be brought HIGH. Following the NOP command, a Precharge ALL command must be applied. Next a Mode Register Set command must be issued for the Extended Mode Register, to enable the DLL, and then a Mode Register Set command must be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A Precharge ALL command should be applied, placing the device in the “all banks idle” state

Once in the idle state, two auto refresh cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

DDR SDRAM's may be reinitialized at any time during normal operation by asserting a valid MRS command to either the base or extended mode registers without affecting the contents of the memory array. The contents of either the mode register or extended mode register can be modified at any valid time during device operation without affecting the state of the internal address refresh counters used for device refresh.

Register Definition

Mode Register

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode. The Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements results in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition.

Burst Length, Burst Type and Starting Column Address

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type=Sequential	Type=Interleaved
2	-	-	0	0-1	0-1
	-	-	1	1-0	1-0
4	-	0	0	0-1-2-3	0-1-2-3
	-	0	1	1-2-3-0	1-0-3-2
	-	1	0	2-3-0-1	2-3-0-1
	-	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-A i selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A i selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A i selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

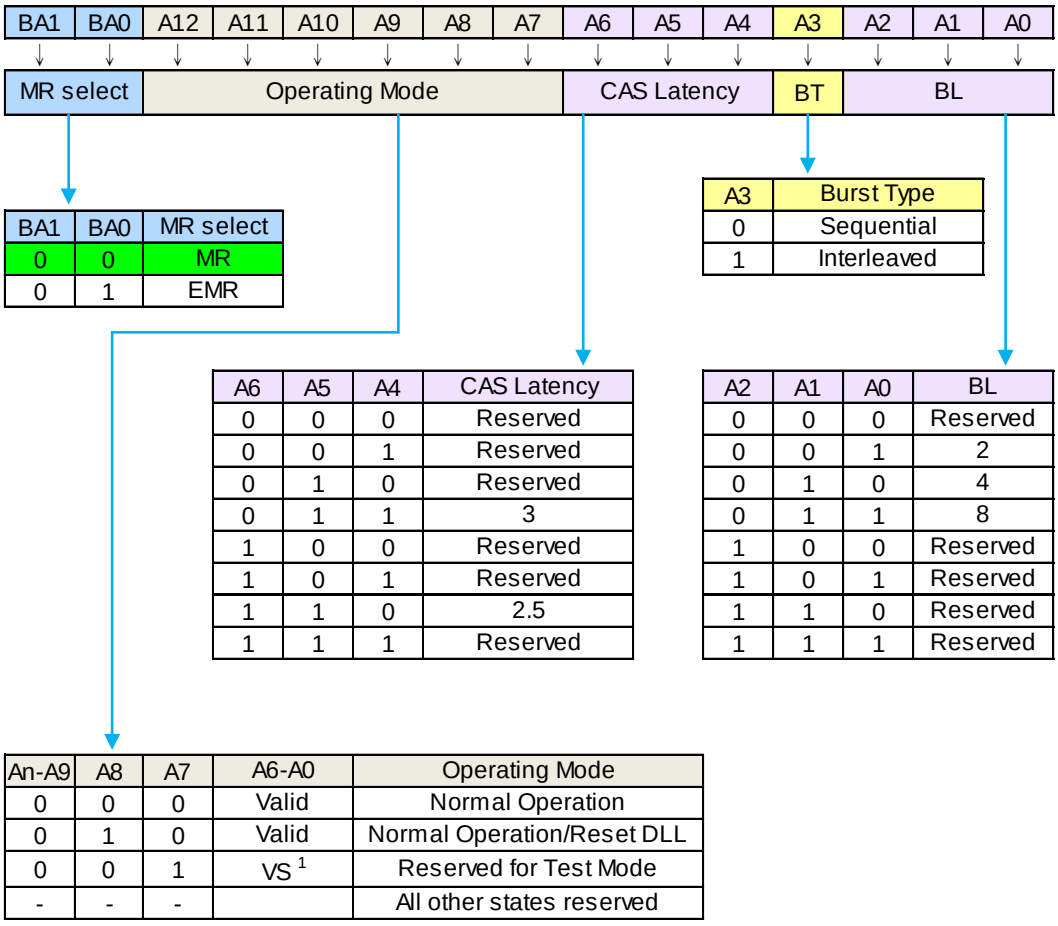
Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data.

If a Read command is registered at clock edge *n*, and the latency is *m* clocks, the data is available nominally coincident with clock edge *n* + *m*.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Mode Register Operation



BA1	BA0	MR select
0	0	MR
0	1	EMR

A3	Burst Type
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A2	A1	A0	BL
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

An-A9	A8	A7	A6-A0	Operating Mode
0	0	0	Valid	Normal Operation
0	1	0	Valid	Normal Operation/Reset DLL
0	0	1	VS [1]	Reserved for Test Mode
-	-	-		All other states reserved

Notes:

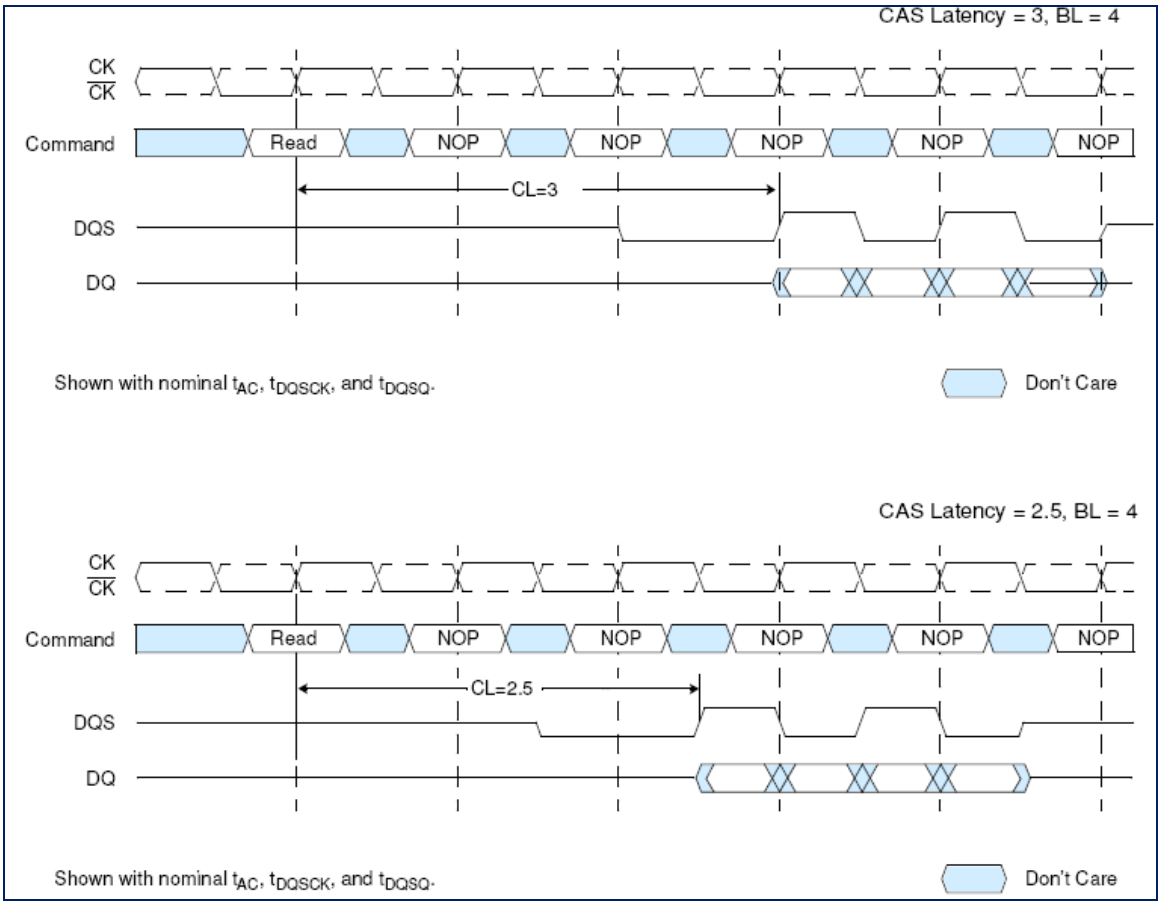
1. VS = Vendor Specific. Please contact with NTC for specific demands.
2. An = most significant address bit for this device.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latencies



Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, bit A0; output drive strength selection, bit A1. These functions are controlled via the bit settings shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

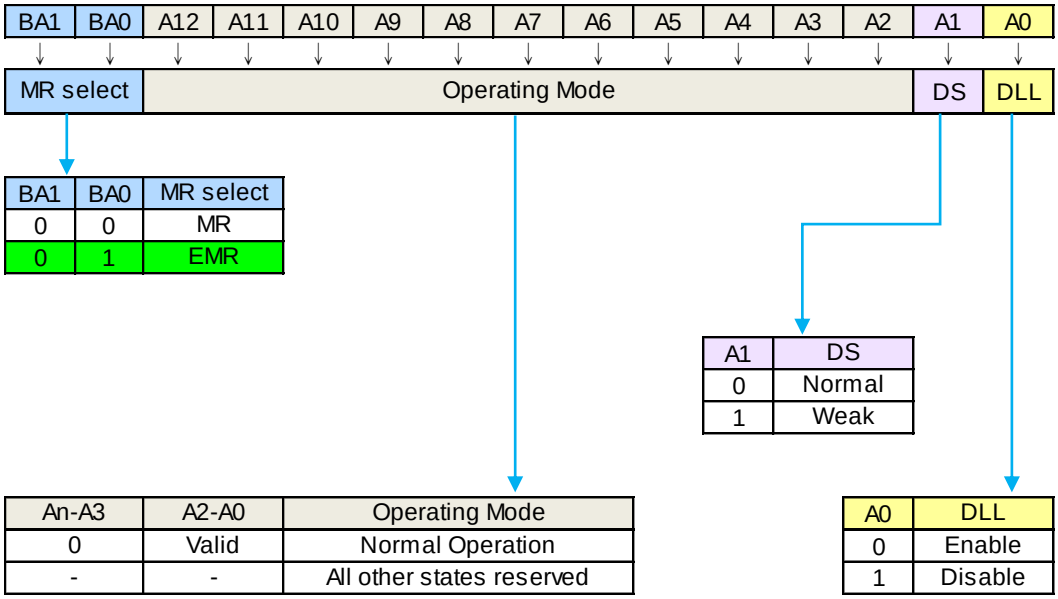
DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before a Read command can be issued. This is the reason for introducing timing parameter tXSRD for DDR SDRAM's (Exit Self Refresh to Read Command). Non- Read commands can be issued 2 clocks after the DLL is enabled via the EMRS command (tMRD) or 10 clocks after the DLL is enabled via self refresh exit command (tXSNR, Exit Self Refresh to Non-Read Command).

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II.

Extended Mode Register Definition



BA1	BA0	MR select
0	0	MR
0	1	EMR

A1	DS
0	Normal
1	Weak

An-A3	A2-A0	Operating Mode
0	Valid	Normal Operation
-	-	All other states reserved

A0	DLL
0	Enable
1	Disable

Commands

Truth Tables 1a and 1b provide a reference of the commands supported by DDR SDRAM devices. A verbal description of each command follows.

Truth Table 1a Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Notes
Deselect (NOP)	H	X	X	X	X	9
No Operation (NOP)	L	H	H	H	X	9
Active (Select Bank and Activate Row)	L	L	H	H	Bank / Row	3
Read (Select Bank, Column and Start Read Burst)	L	H	L	H	Bank / Col	4
Write (Select Bank, Column and Start Write Burst)	L	H	L	L	Bank / Col	4
Burst Terminate	L	H	H	L	X	8
Pre-Charge (Deactivate Row In Bank or Banks)	L	L	H	L	Code	5
Auto Refresh or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	6,7
Mode Register Set	L	L	L	L	Op-Code	2

Notes:

1. CKE is high for all commands shown except Self Refresh.
2. BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.)
3. BA0-BA1 provides bank address and A0-A12 provides row address.
4. BA0, BA1 provide bank address; A0-A*i* provide column address; A10 high enables the Auto Precharge feature (non-persistent), A10 low disables the Auto Precharge feature.
5. A10 LOW: BA0, BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care.”
6. This command is auto refresh if CKE is high; Self Refresh if CKE is low.
7. Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts.
9. Deselect and NOP are functionally interchangeable.

Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Notes:

1. Used to mask write data; provided coincident with the corresponding data.

Deselect

The Deselect function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The No Operation (NOP) command is used to perform a NOP to a DDR SDRAM. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Mode Register Set

The mode registers are loaded via inputs A0-A12, BA0 and BA1 while issuing the Mode Register Set Command. See mode register descriptions in the Register Definition section. The Mode Register Set command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until tMRD is met.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

Write

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Precharge

The Precharge command is used to deactivate (close) the open row in a particular bank or the open row(s) in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A precharge command is treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

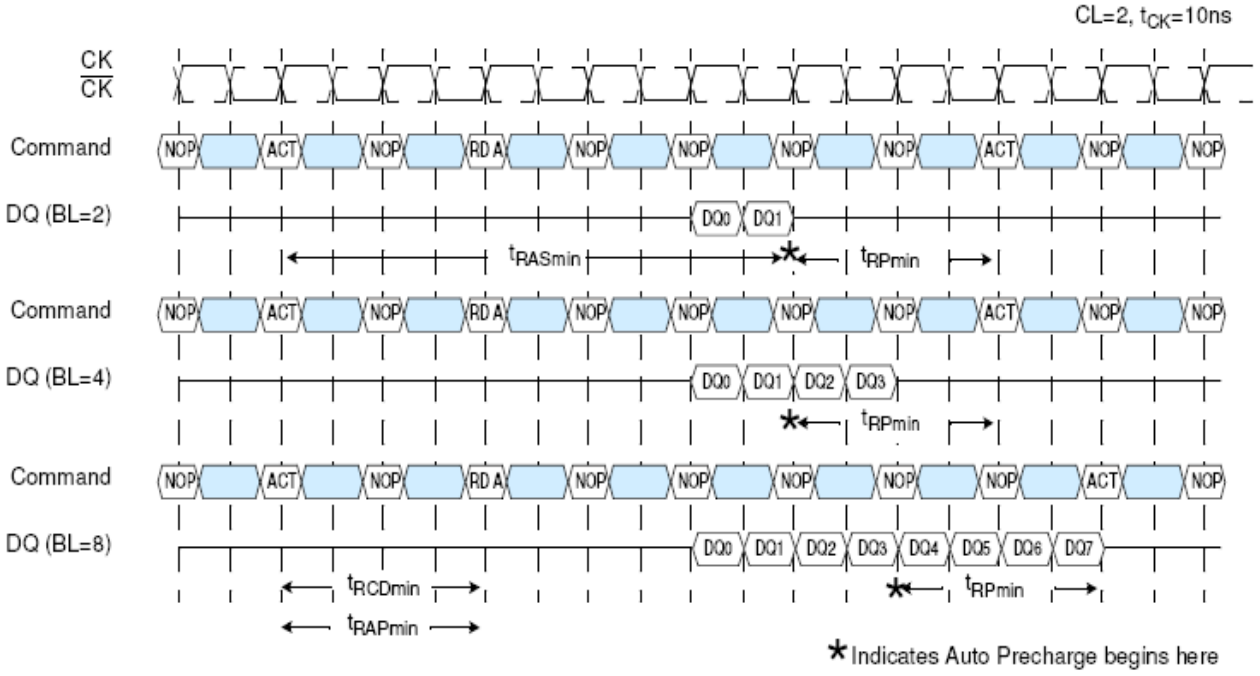
Auto Precharge

Auto Precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst. Auto Precharge is non-persistent in that it is either enabled or disabled for each individual Read or Write command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This is determined as if an explicit Precharge command was issued at the earliest possible time without violating tRAS (min). The user must not issue another command to the same bank until the precharge (tRP) is completed.

NTC DDR SDRAM device supports the optional tRAS lockout feature. This feature allows a Read command with Auto Precharge to be issued to a bank that has been activated (opened) but has not yet satisfied the tRAS (min) specification. The tRAS lockout feature essentially delays the onset of the auto precharge operation until two conditions occur. One, the entire burst length of data has been successfully prefetched from the memory array; and two, tRAS (min) has been satisfied.

As a means to specify whether a DDR SDRAM device supports the tRAS lockout feature, a new parameter has been defined; tRAP (RAS Command to Read Command with Auto Precharge or better stated Bank Activate to Read Command with Auto Precharge). For devices that support the tRAS lockout feature, tRAP = tRCD (min). This allows any Read Command (with or without Auto Precharge) to be issued to an open bank once tRCD (min) is satisfied.

tRAP Definition



The above timing diagrams show the effects of t_{RAP} for devices that support t_{RAS} lockout. In these cases, the Read with Auto Precharge command (RDA) is issued with t_{RCD}(min) and dataout is available with the shortest latency from the Bank Activate command (ACT). The internal precharge operation, however, does not begin until after t_{RAS}(min) is satisfied.

Burst Terminate

The Burst Terminate command is used to truncate read bursts (with Auto Precharge disabled). The most recently registered Read command prior to the Burst Terminate command is truncated, as shown in the Operation section of this data sheet. Write burst cycles are not to be terminated with the Burst Terminate command.

Auto Refresh

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to CAS before RAS (CBR) Refresh in previous DRAM types. This command is non-persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The 512Mb DDR SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8μs (maximum).

Self Refresh

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are "Don't Care" during Self Refresh operation.

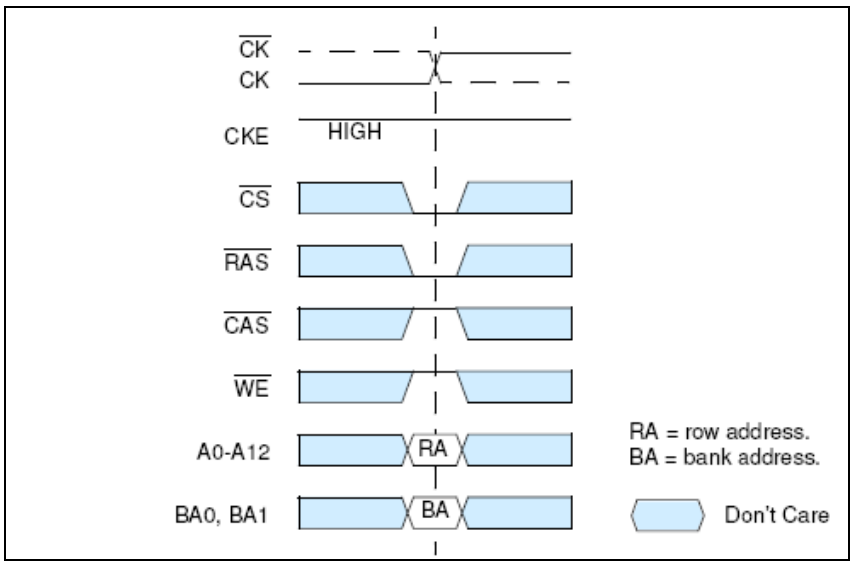
The procedure for exiting self refresh requires a sequence of commands. CK (and $\overline{CK}$) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Operations

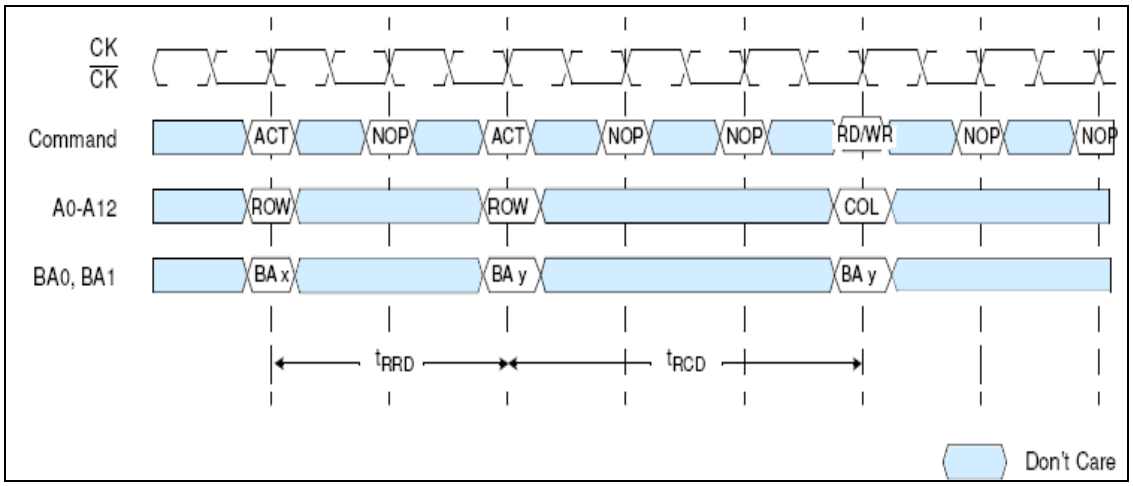
Bank/Row Activation

Before any Read or Write commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened" (activated). This is accomplished via the Active command and addresses A0-A12, BA0 and BA1 (see Activating a Specific Row in a Specific Bank), which decode and select both the bank and the row to be activated. After opening a row (issuing an Active command), a Read or Write command may be issued to that row, subject to the t_{RCD} specification. A subsequent Active command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive Active commands to the same bank is defined by t_{RC}. A subsequent Active command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.

Activating a Specific Row in a Specific Bank



tRCD and tRRD Definition



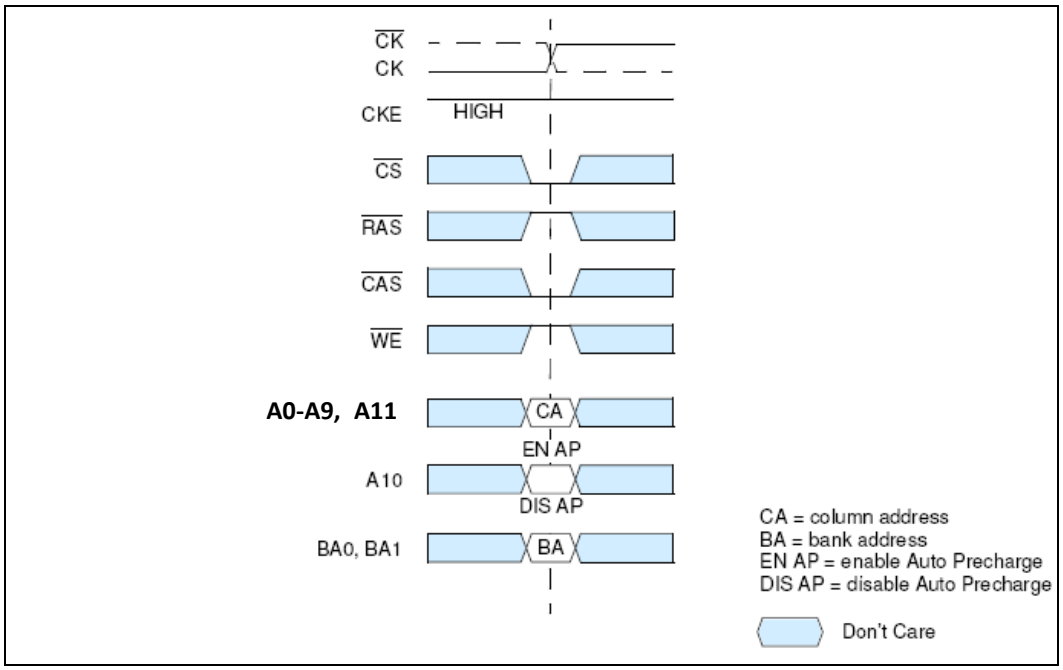
Reads

Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command.

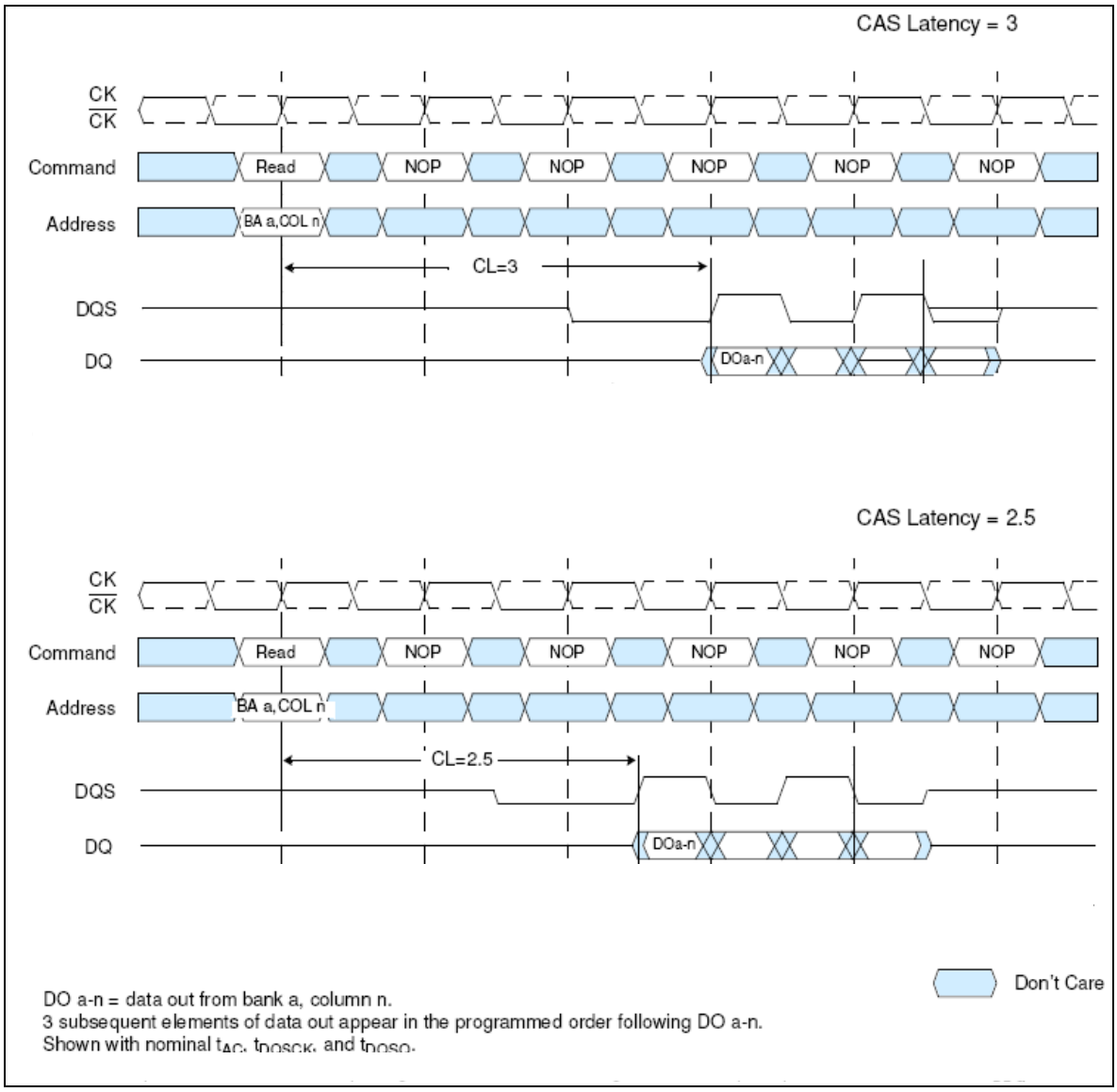
The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and CK). The following timing figure entitled “Read Burst: CAS Latencies (Burst Length=4)” illustrates the general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read post amble. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS go High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure entitled “Consecutive Read Bursts: CAS Latencies (Burst Length =4 or 8)”. A Read command can be initiated on any positive clock cycle following a previous Read command. Nonconsecutive Read data is shown in timing figure entitled “Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)”. Full-speed Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8) within a page (or pages) can be performed.

Read Command

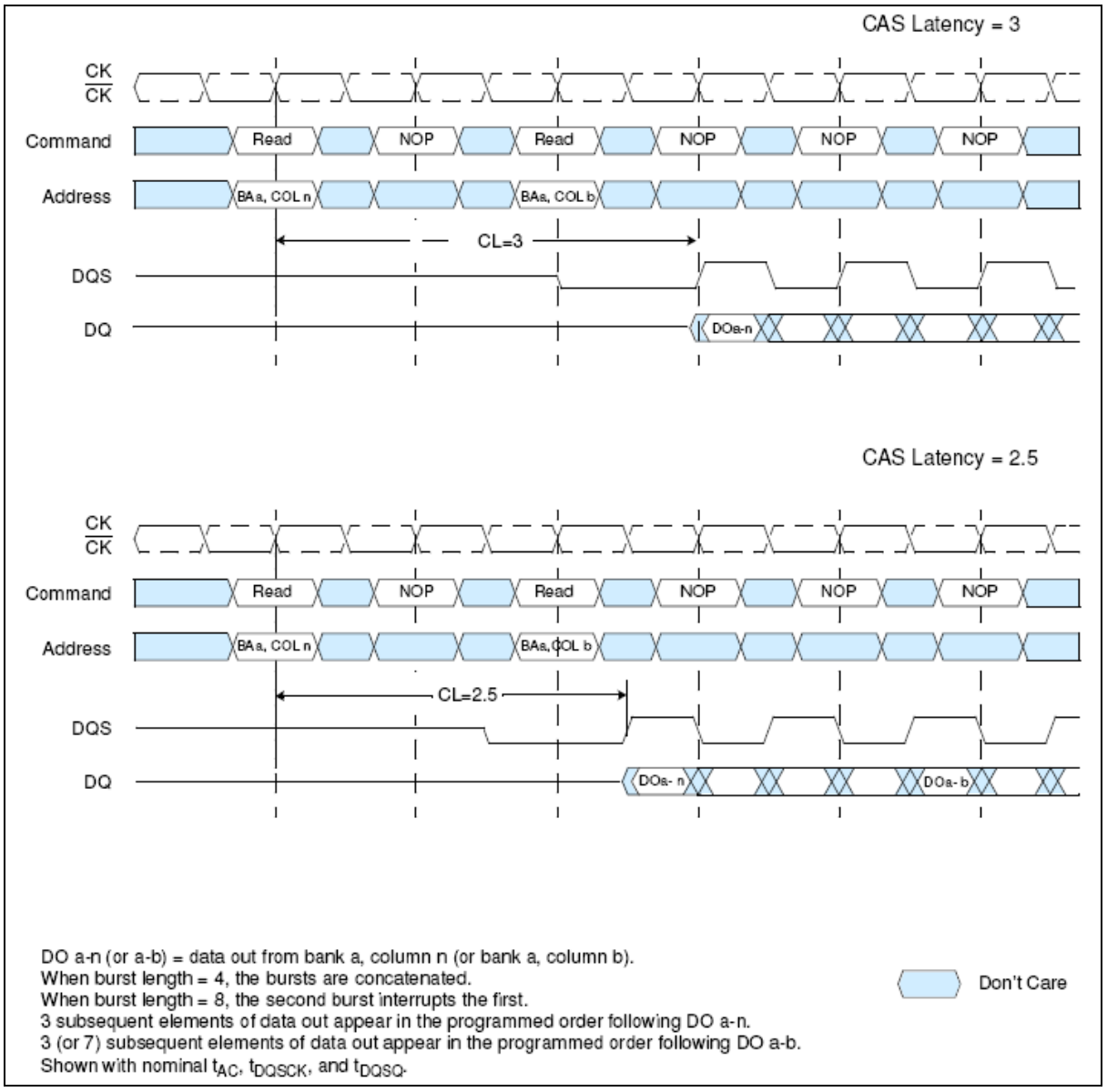


Read Burst: CAS Latencies (Burst Length = 4)



DO a-n = data out from bank a, column n.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

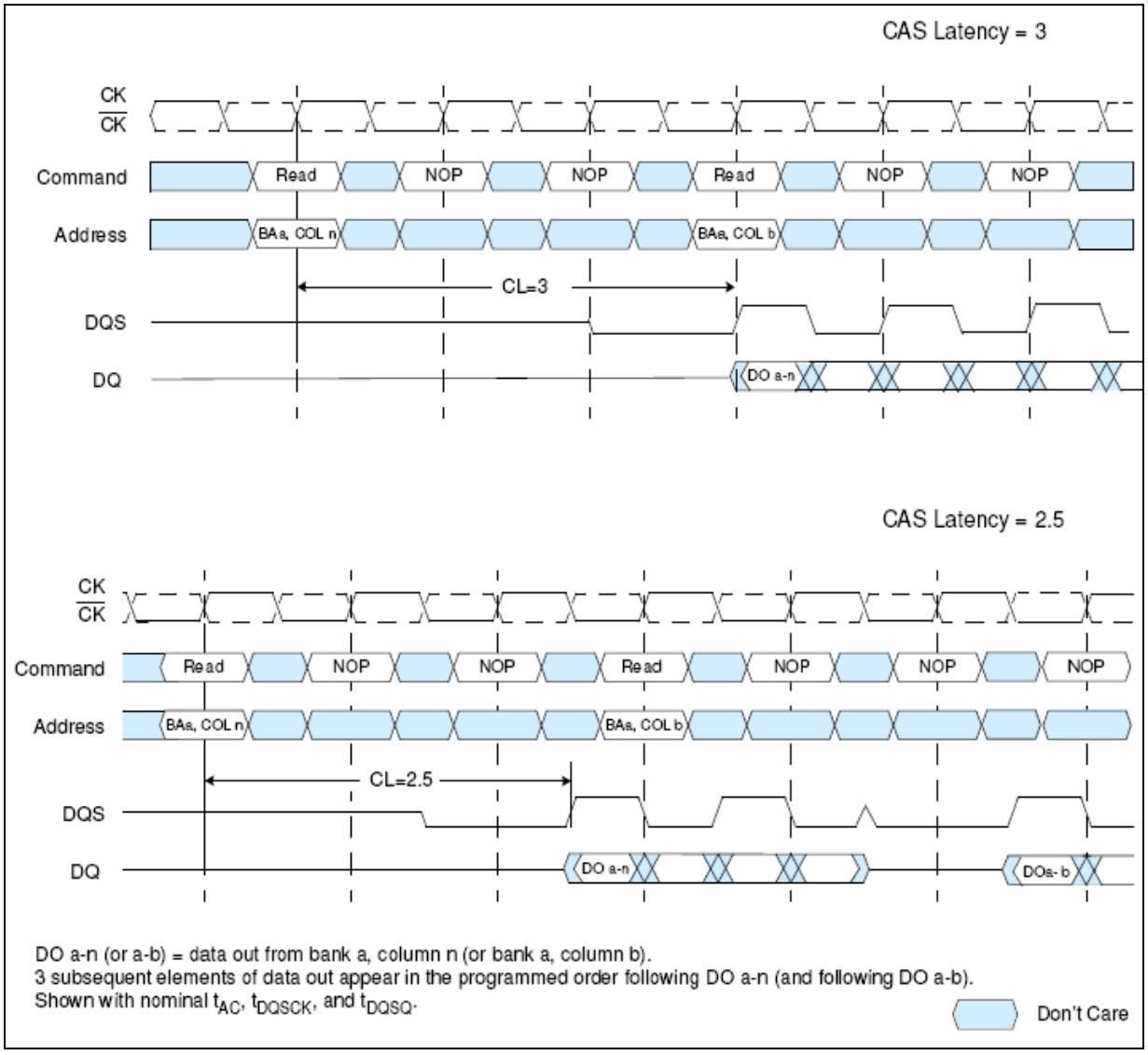
Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)



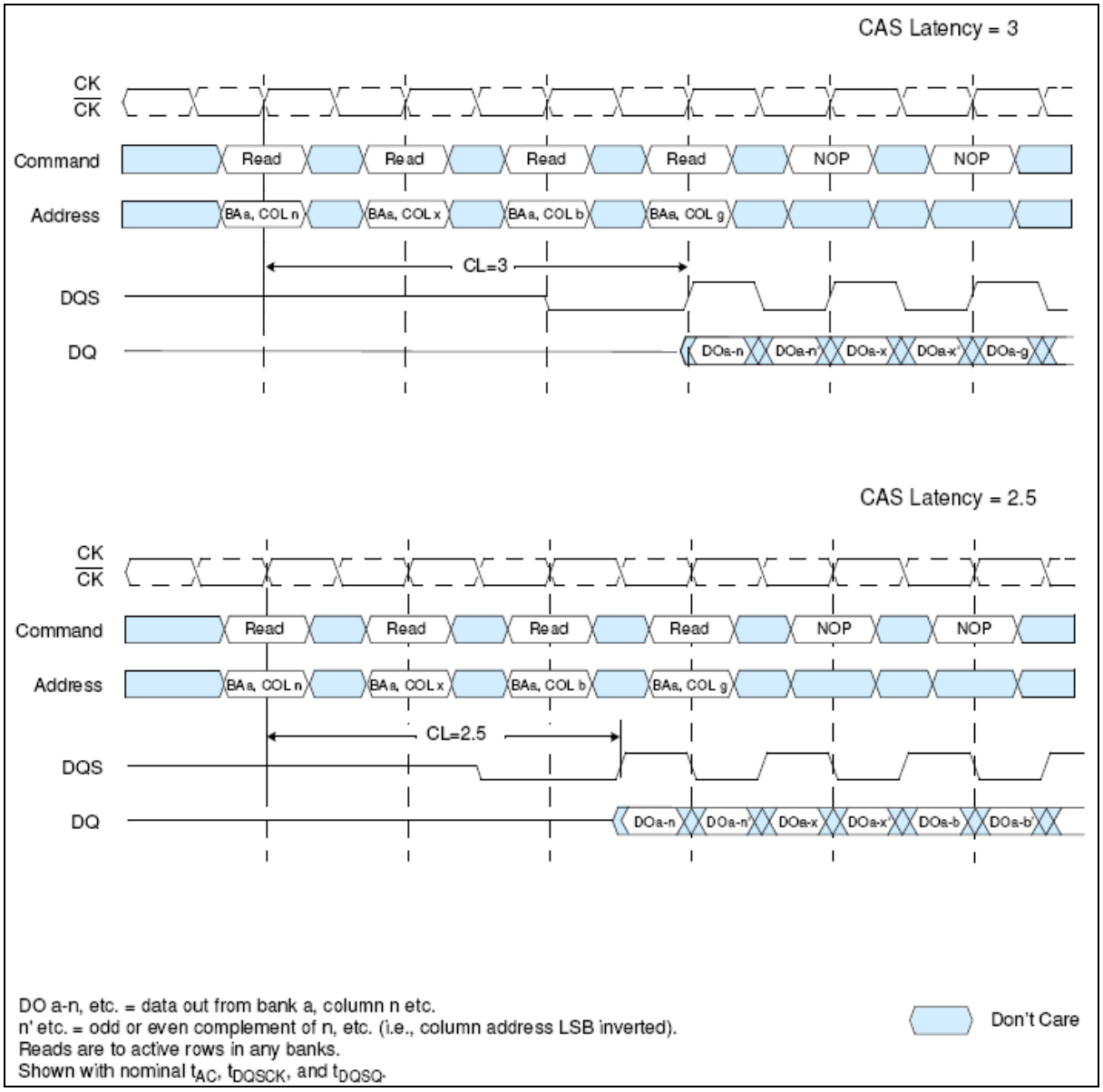
DO a-n (or a-b) = data out from bank a, column n (or bank a, column b).
When burst length = 4, the bursts are concatenated.
When burst length = 8, the second burst interrupts the first.
3 subsequent elements of data out appear in the programmed order following DO a-n.
3 (or 7) subsequent elements of data out appear in the programmed order following DO a-b.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)



Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)



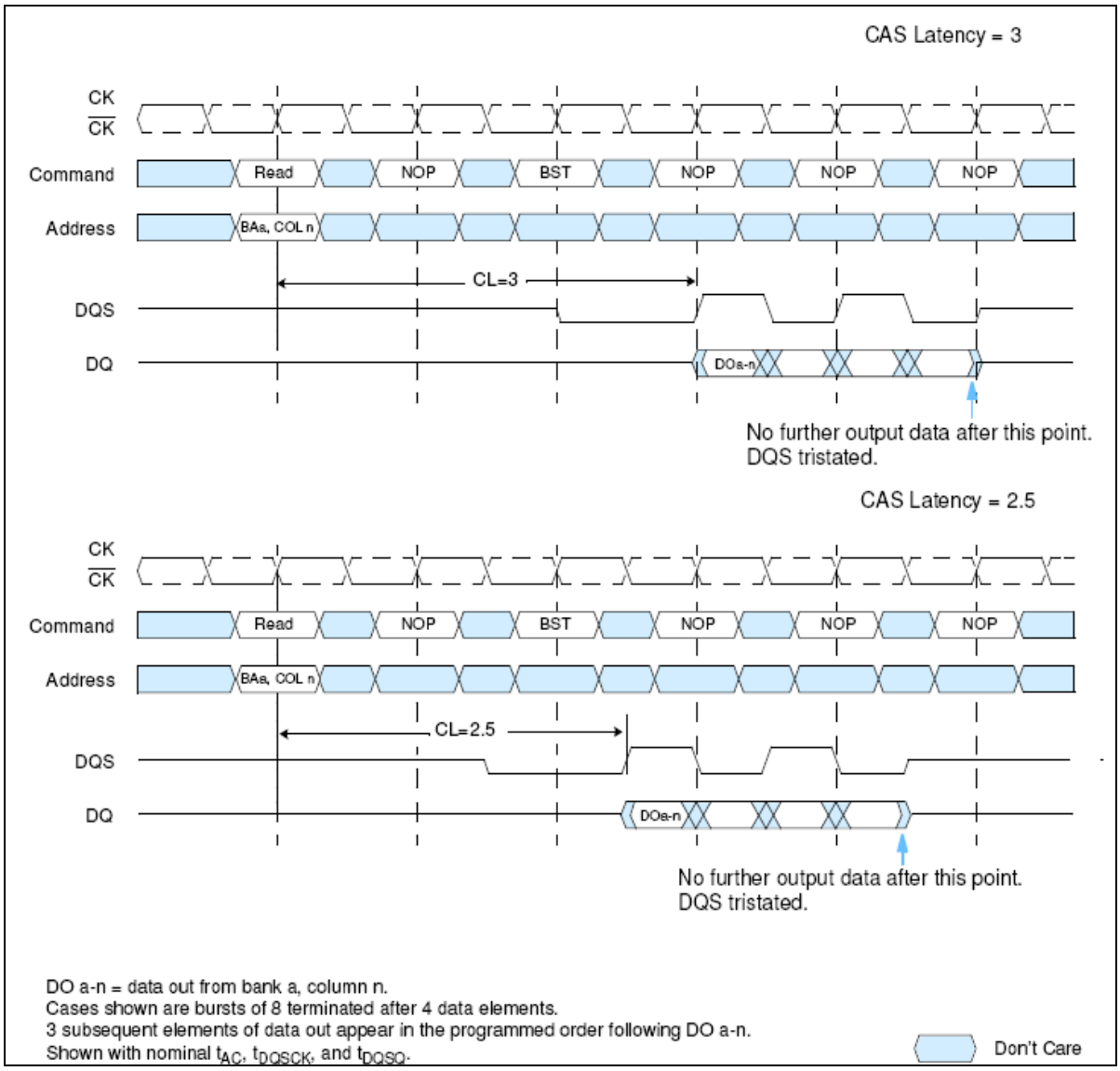
Data from any Read burst may be truncated with a Burst Terminate command, as shown in timing figure entitled *Terminating a Read Burst: CAS Latencies (Burst Length = 8)*. The Burst Terminate latency is equal to the read (CAS) latency, i.e. the Burst Terminate command should be issued x cycles after the Read command, where x equals the number of desired data element pairs.

Data from any Read burst must be completed or truncated before a subsequent Write command can be issued. If truncation is necessary, the Burst Terminate command must be used, as shown in timing figure entitled *Read to Write: CAS Latencies (Burst Length = 4 or 8).* The example is shown for tDQSS (min). The tDQSS (max) case, not shown here, has a longer bus idle time. tDQSS (min) and tDQSS (max) are defined in the section on Writes.

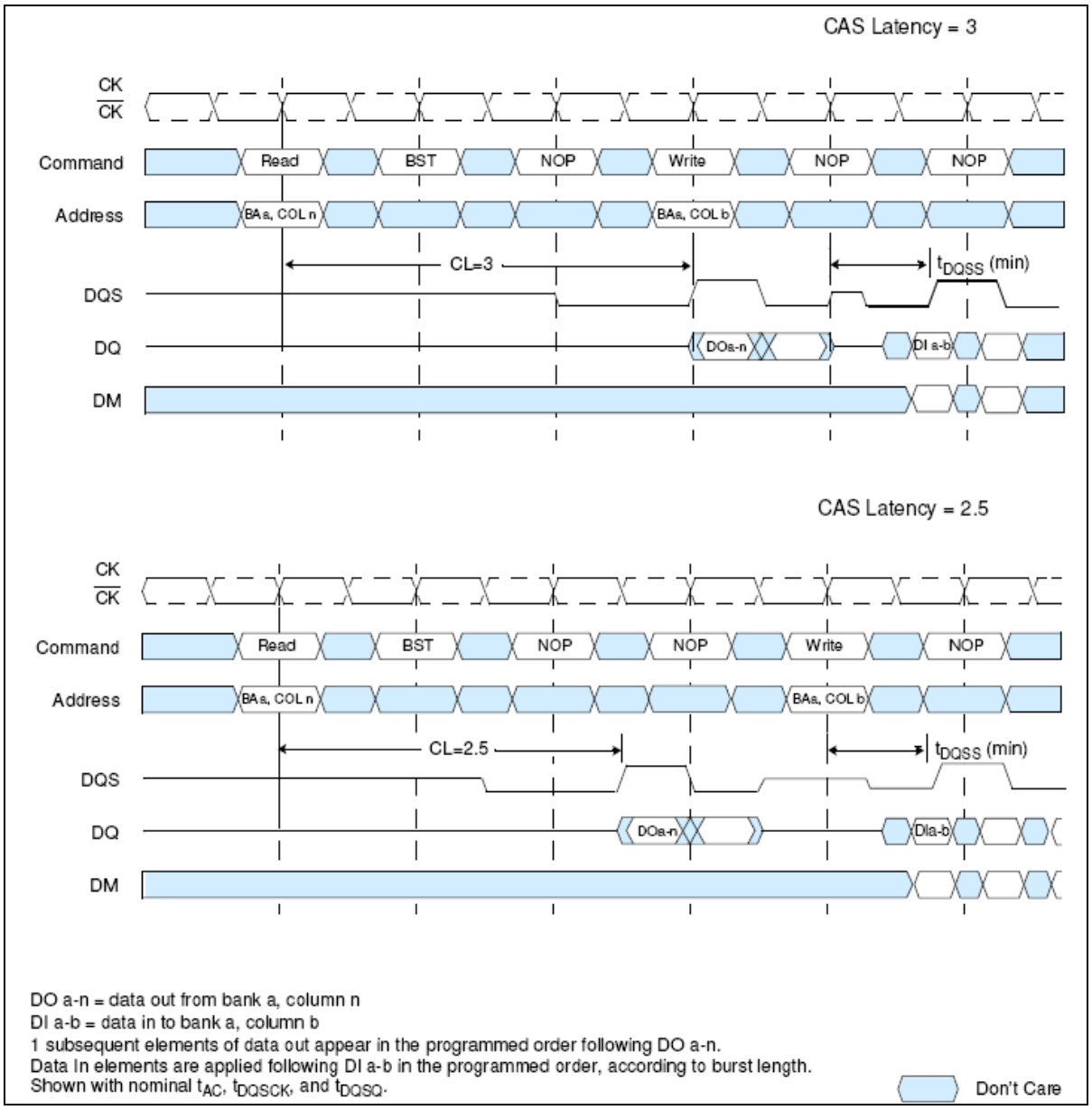
A Read burst may be followed by, or truncated with, a Precharge command to the same bank (provided that Auto Precharge was not activated). The Precharge command should be issued x cycles after the Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure for Read latencies of 3. Following the Precharge command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a Read being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same Read burst with Auto Precharge enabled. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

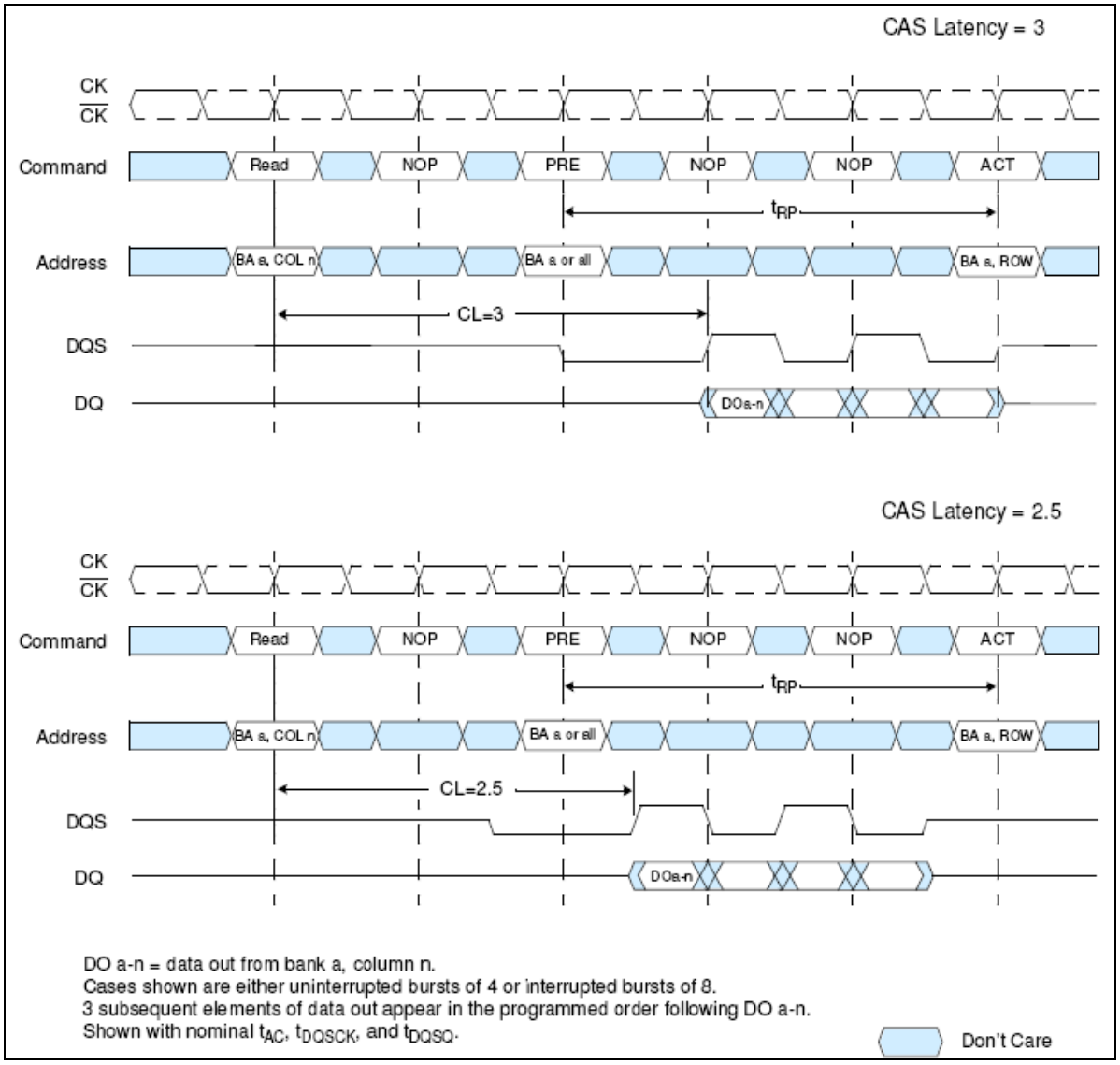
Terminating a Read Burst: CAS Latencies (Burst Length = 8)



Read to Write: CAS Latencies (Burst Length = 4 or 8)



Read to Precharge: CAS Latencies (Burst Length = 4 or 8)



Writes

Write bursts are initiated with a Write command, as shown in timing figure *Write Command*.

The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble. The time between the Write command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. tDQSS(min) and tDQSS(max)). Timing figure *Write Burst (Burst Length = 4)* shows the two extremes of tDQSS for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enter High-Z and any additional input data is ignored.

Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Timing figure *Write to Write (Burst Length = 4)* shows concatenated bursts of 4. An example of nonconsecutive Writes is shown in timing figure *Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)*. Full speed random write accesses within a page or pages can be performed as shown in timing figure *Random Write Cycles (Burst Length = 2, 4 or 8)*. Data for any Write burst may be followed by a subsequent Read command. To follow a Write without truncating the write burst, tWTR (Write to Read) should be met as shown in timing figure *Write to Read: Non-Interrupting (CAS Latency = 3; Burst Length = 4)*.

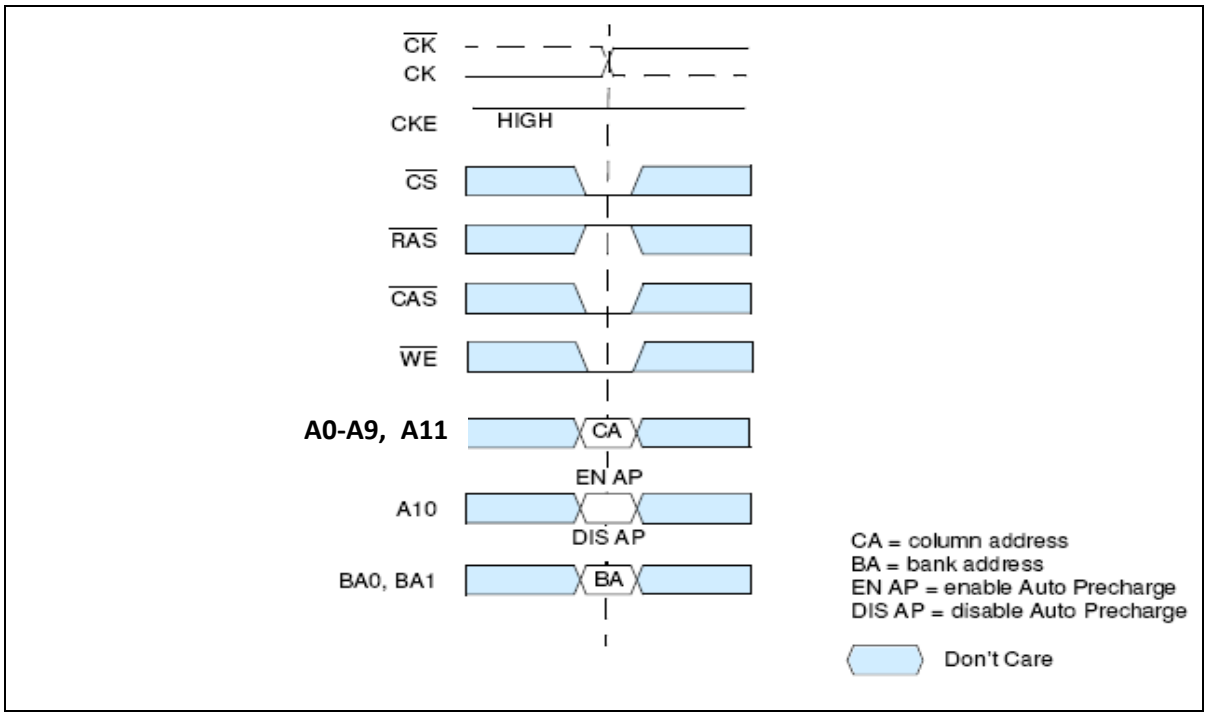
Note that only the data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in the diagrams noted previously.

Data for any Write burst may be followed by a subsequent Precharge command. To follow a Write without truncating the write burst, tWR should be met as shown in timing figure *Write to Precharge: Non-Interrupting (Burst Length = 4).*

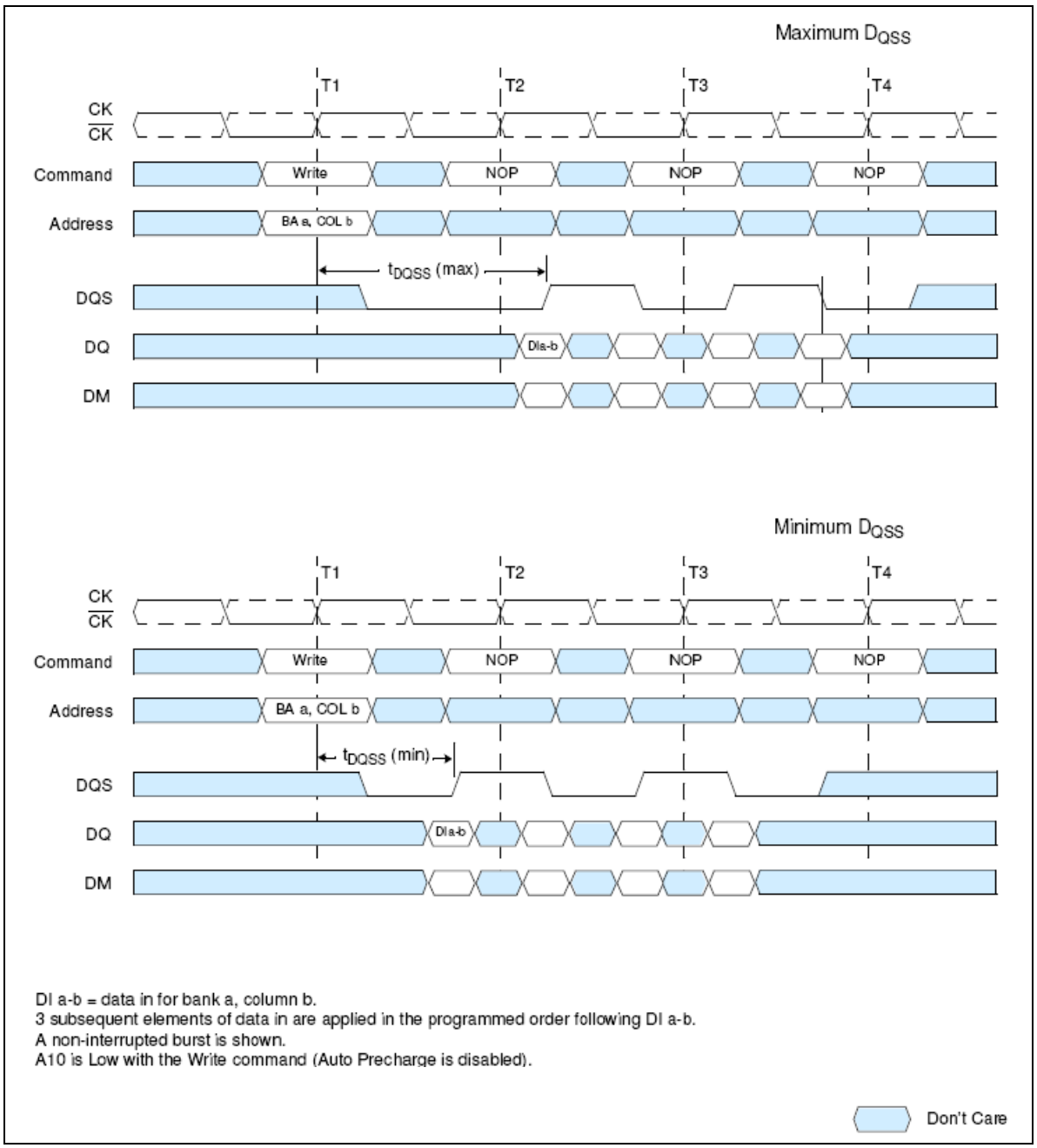
Data for any Write burst may be truncated by a subsequent Precharge command, as shown in timing figures *Write to Precharge: Interrupting (Burst Length = 4 or 8)* to *Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)*. Note that only the data-in pairs that are registered prior to the tWR period are written to the internal array and any subsequent data in should be masked with DM, Following the Precharge command, a subsequent command to the same bank cannot be issued until tRP is met.

In the case of a Write burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same burst with Auto Precharge. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

Write Command



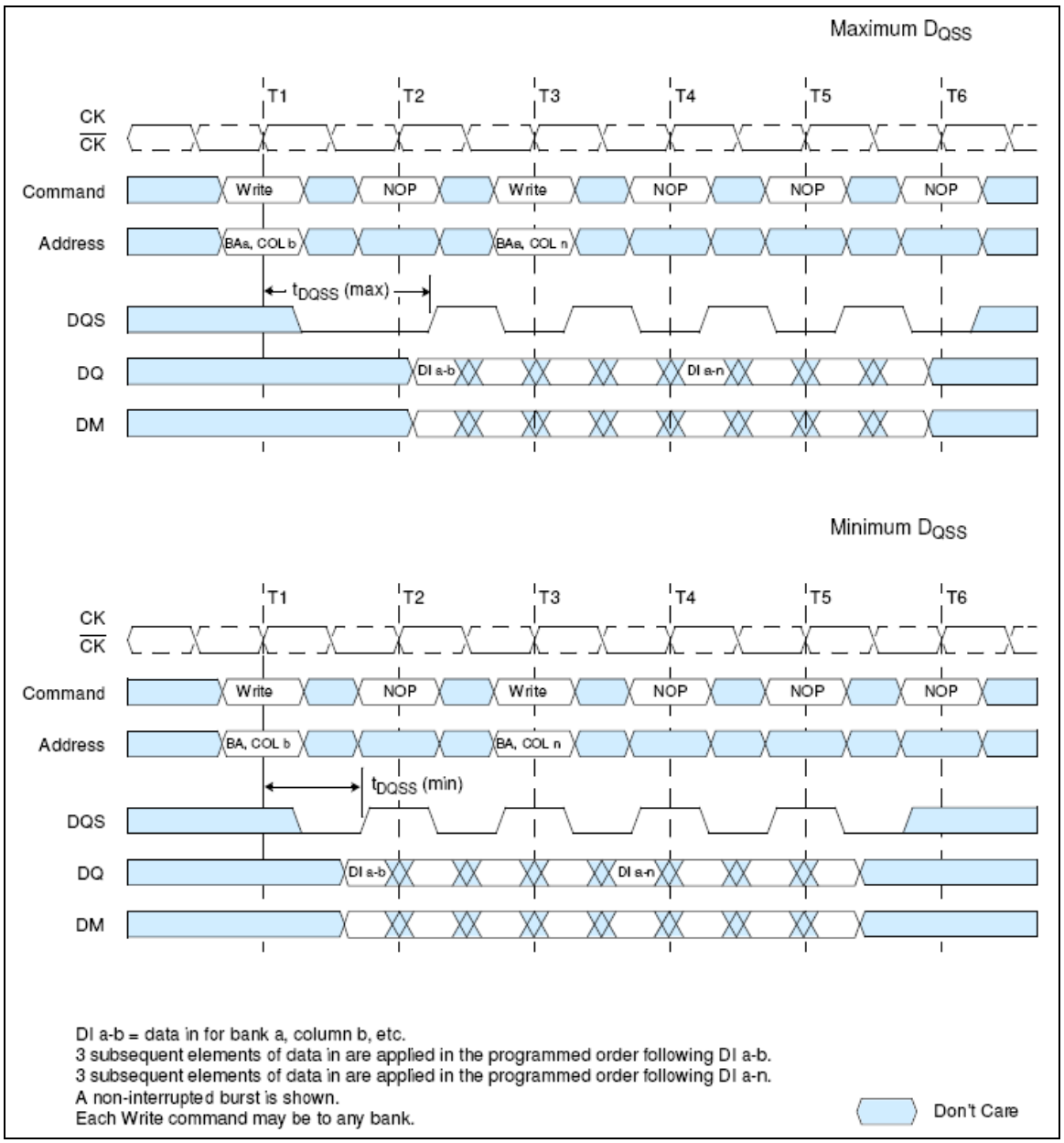
Write Burst (Burst Length = 4)



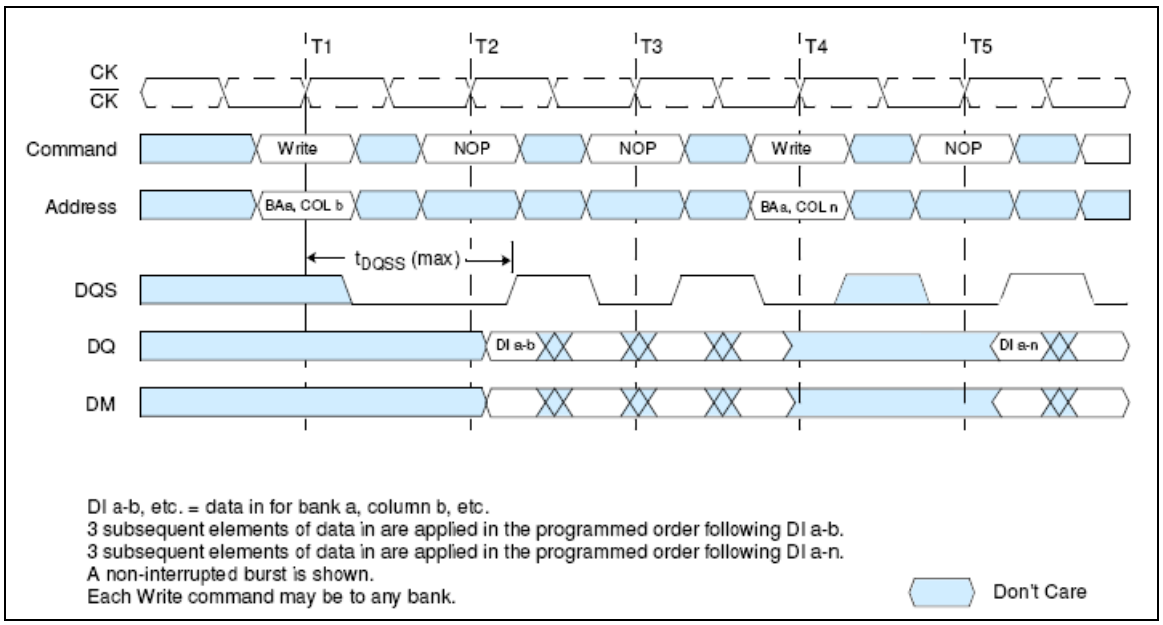
DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
A10 is Low with the Write command (Auto Precharge is disabled).

Don't Care

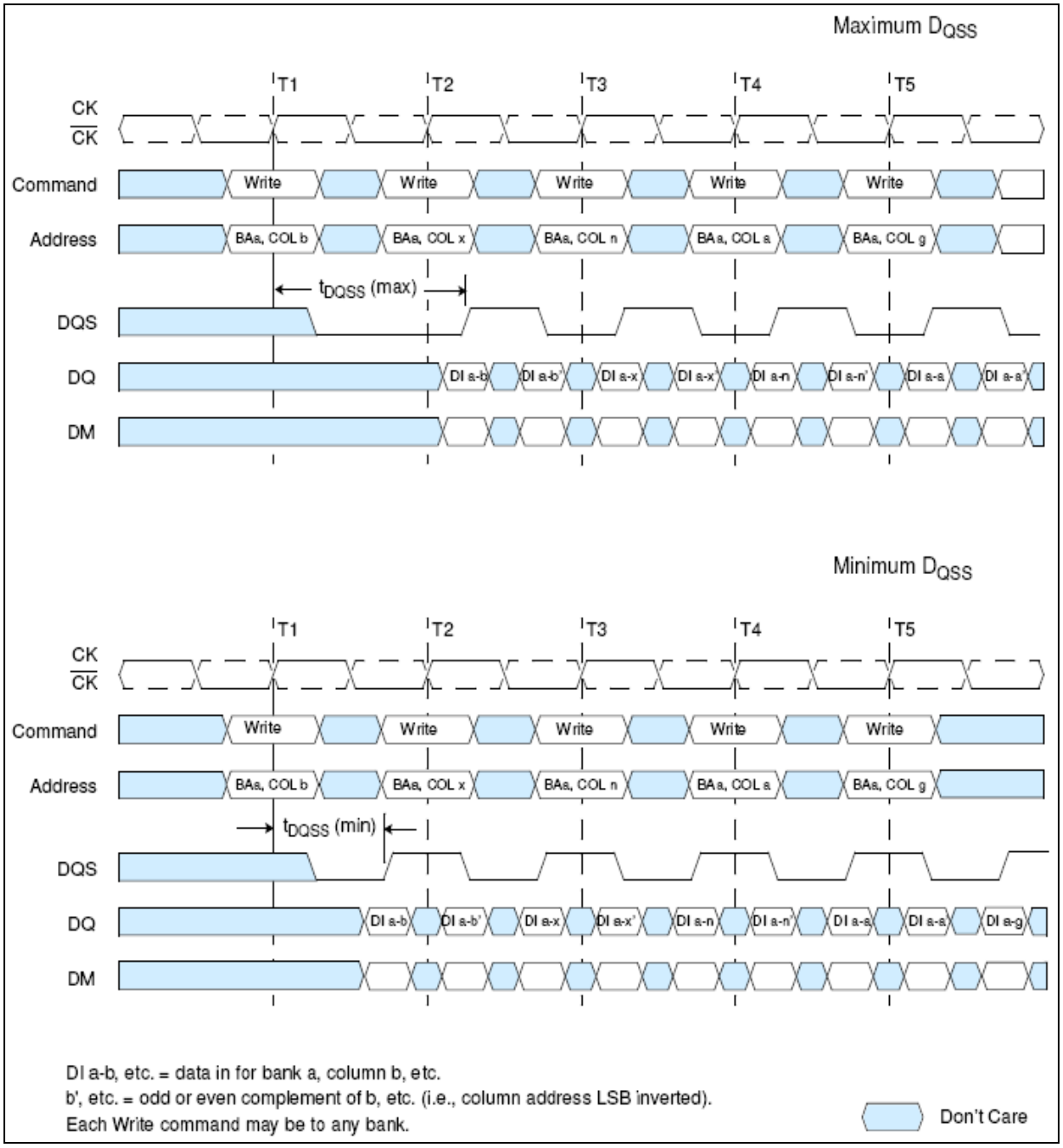
Write to Write (Burst Length = 4)



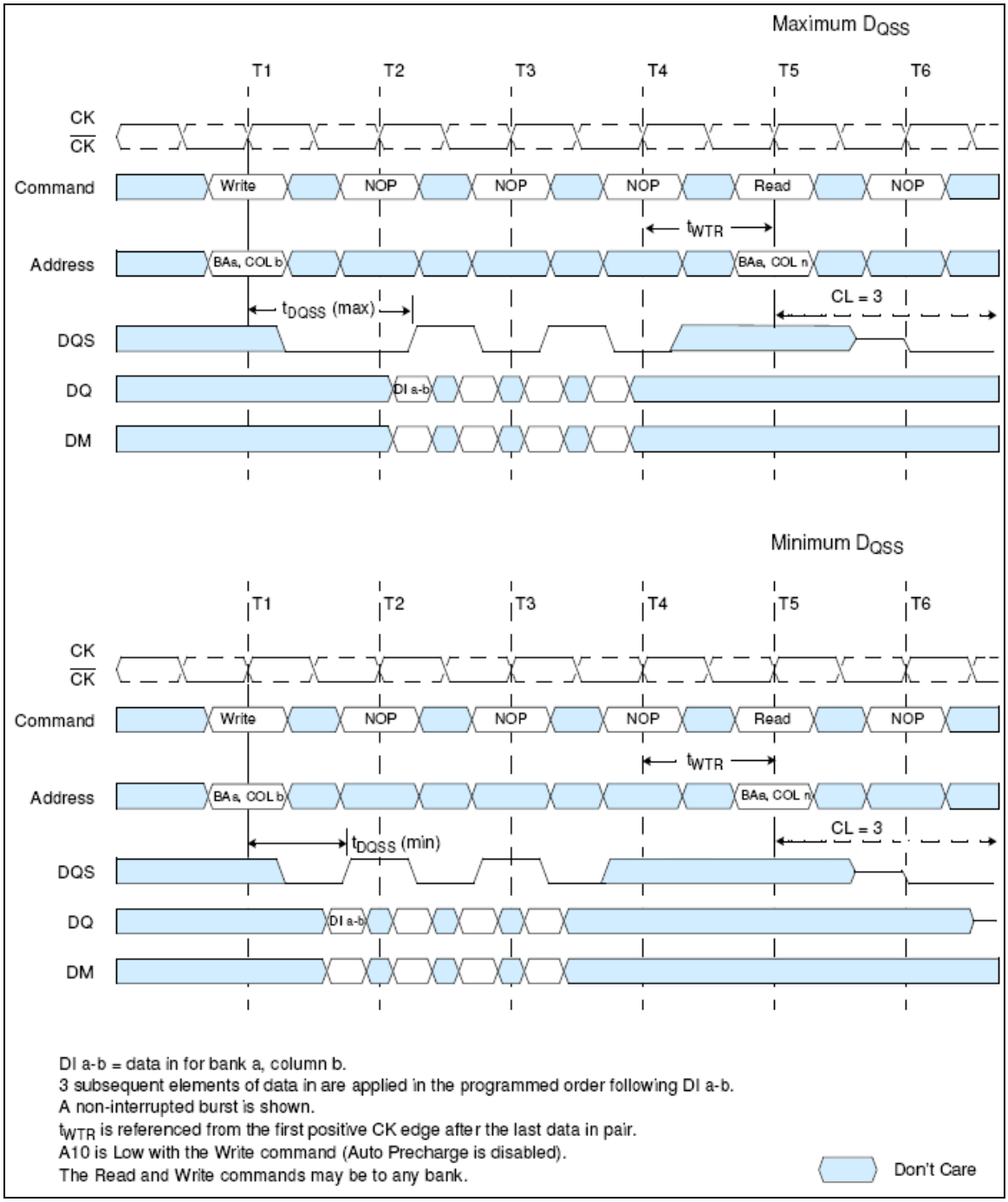
Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)



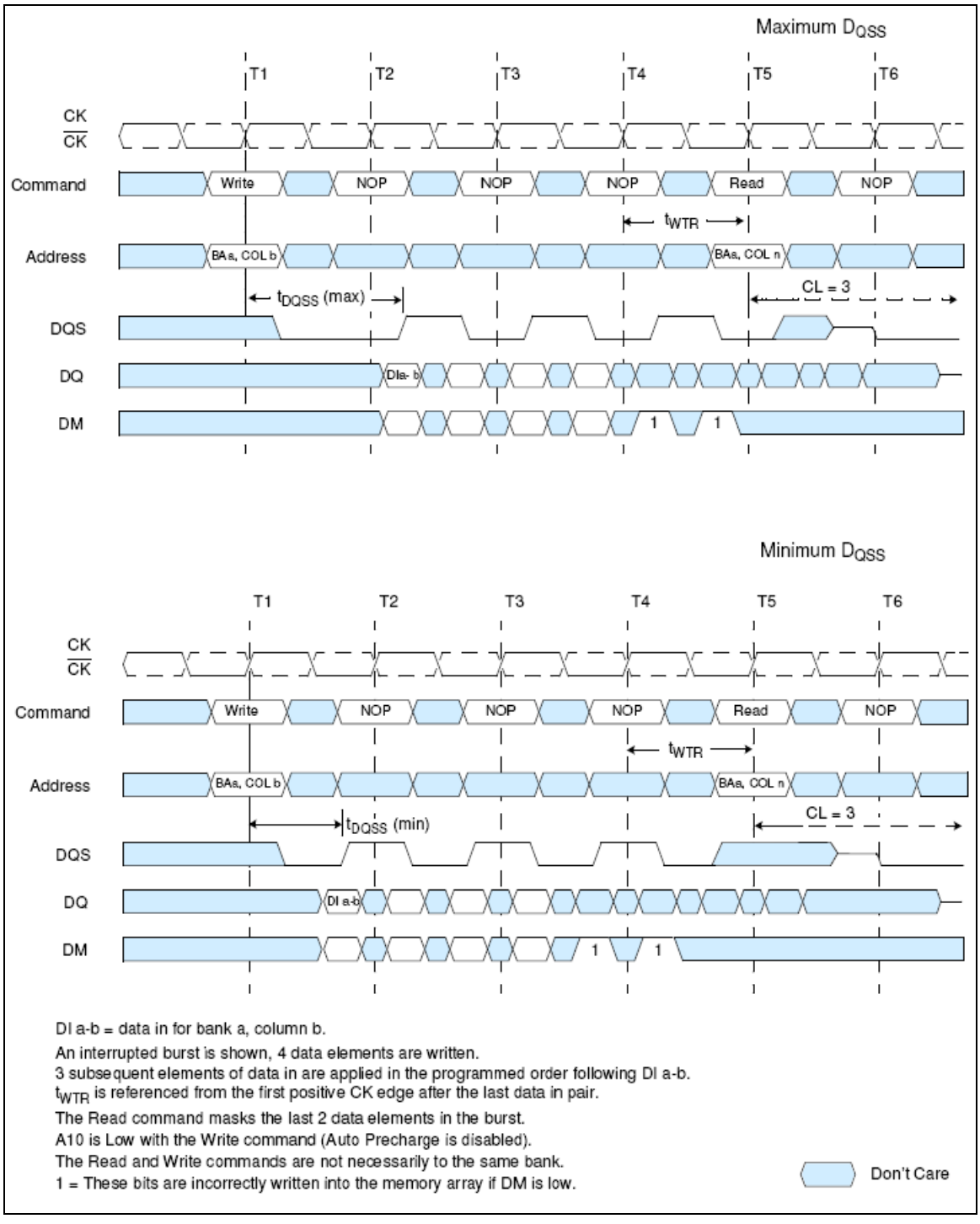
Random Write Cycles (Burst Length = 2, 4 or 8)



Write to Read: Non-Interrupting (CAS Latency = 3; Burst Length = 4)

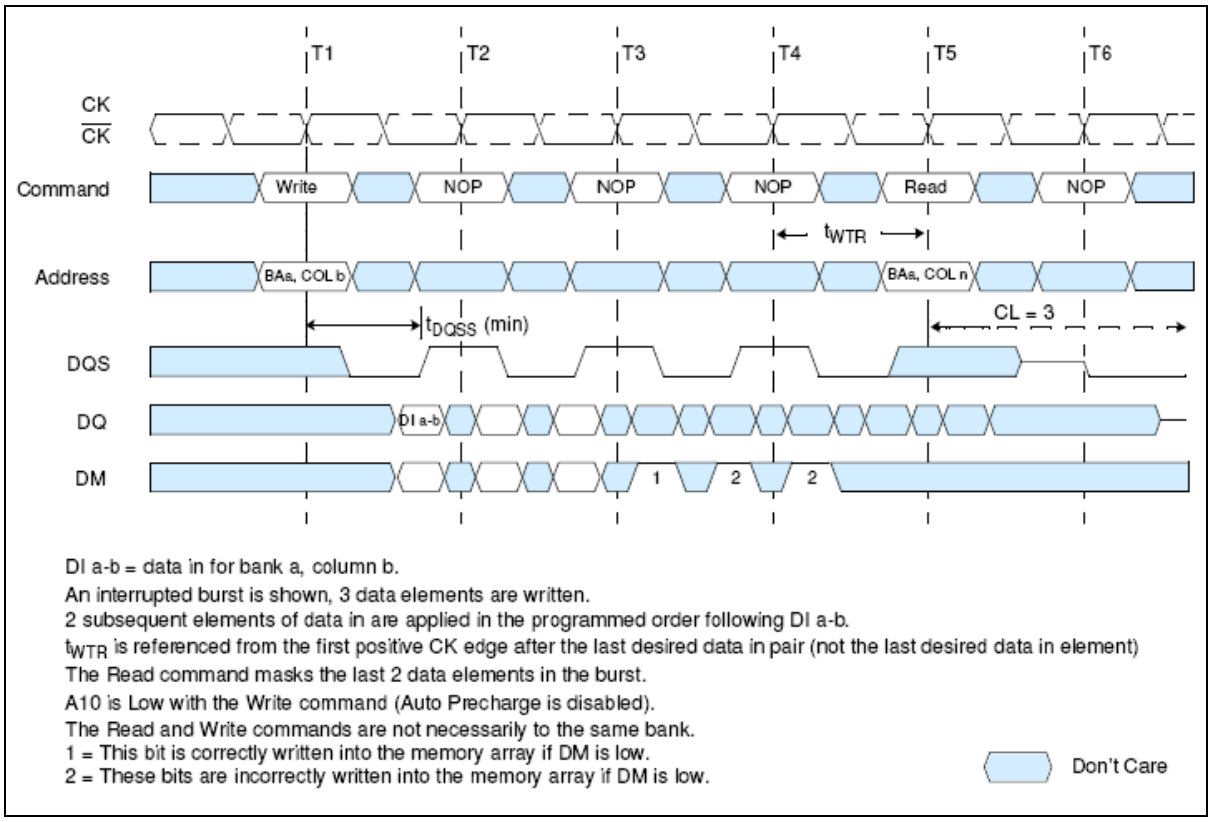


Write to Read: Interrupting (CAS Latency = 3; Burst Length = 8)

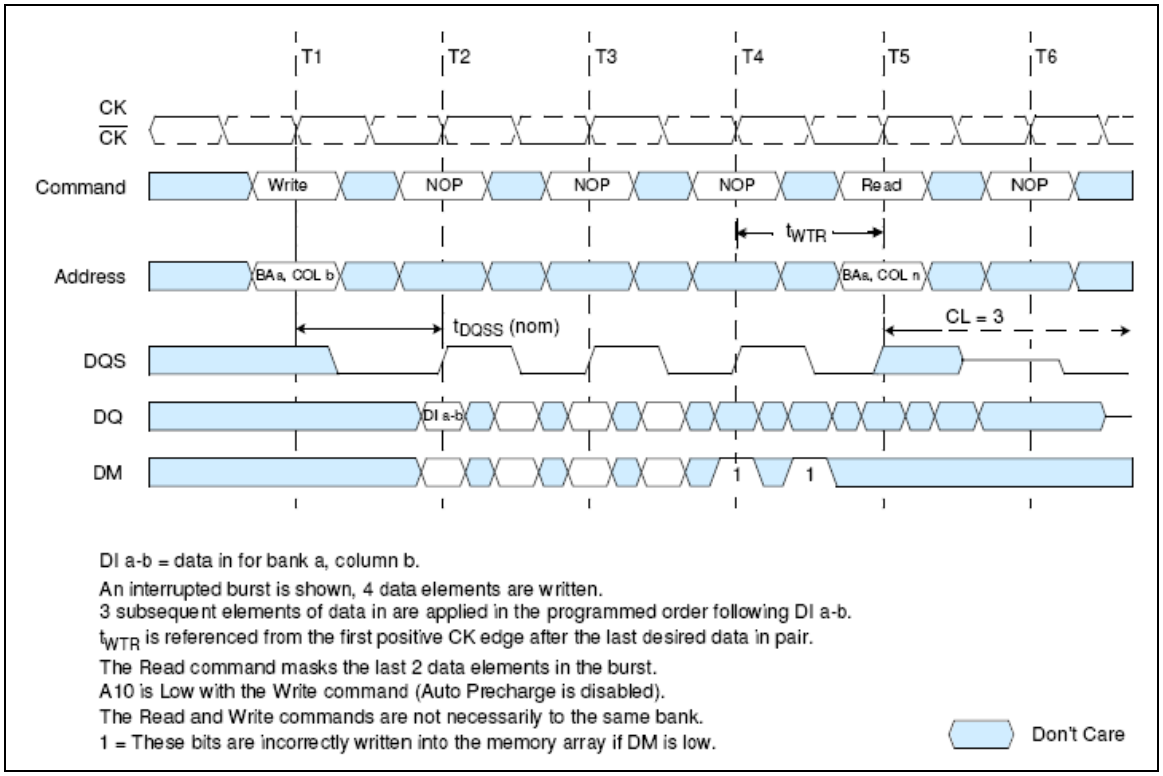


Write to Read: Minimum DQSS, Odd Number of Data (3 bit Write), and Interrupting

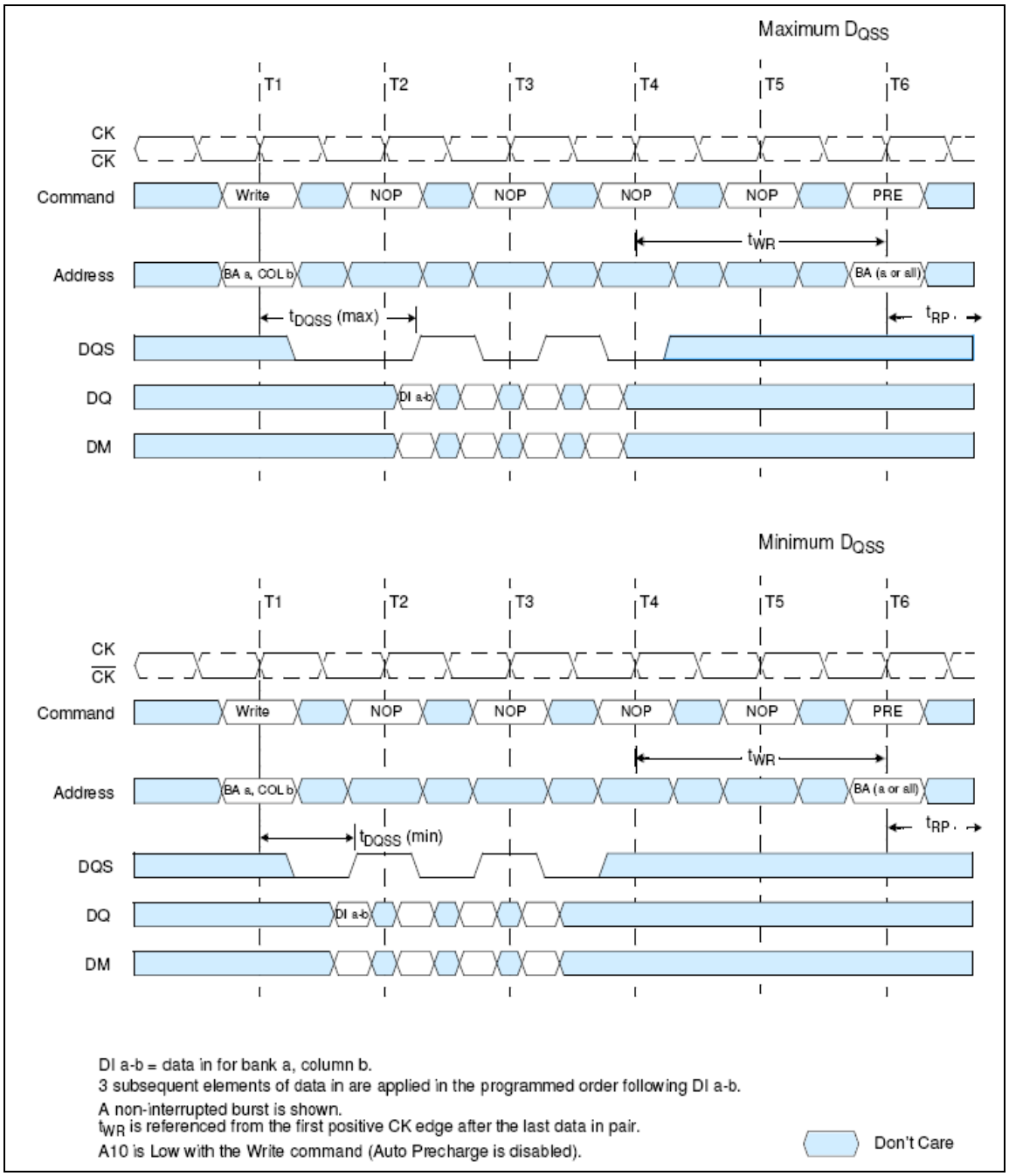
(CAS Latency = 3; Burst Length = 8)



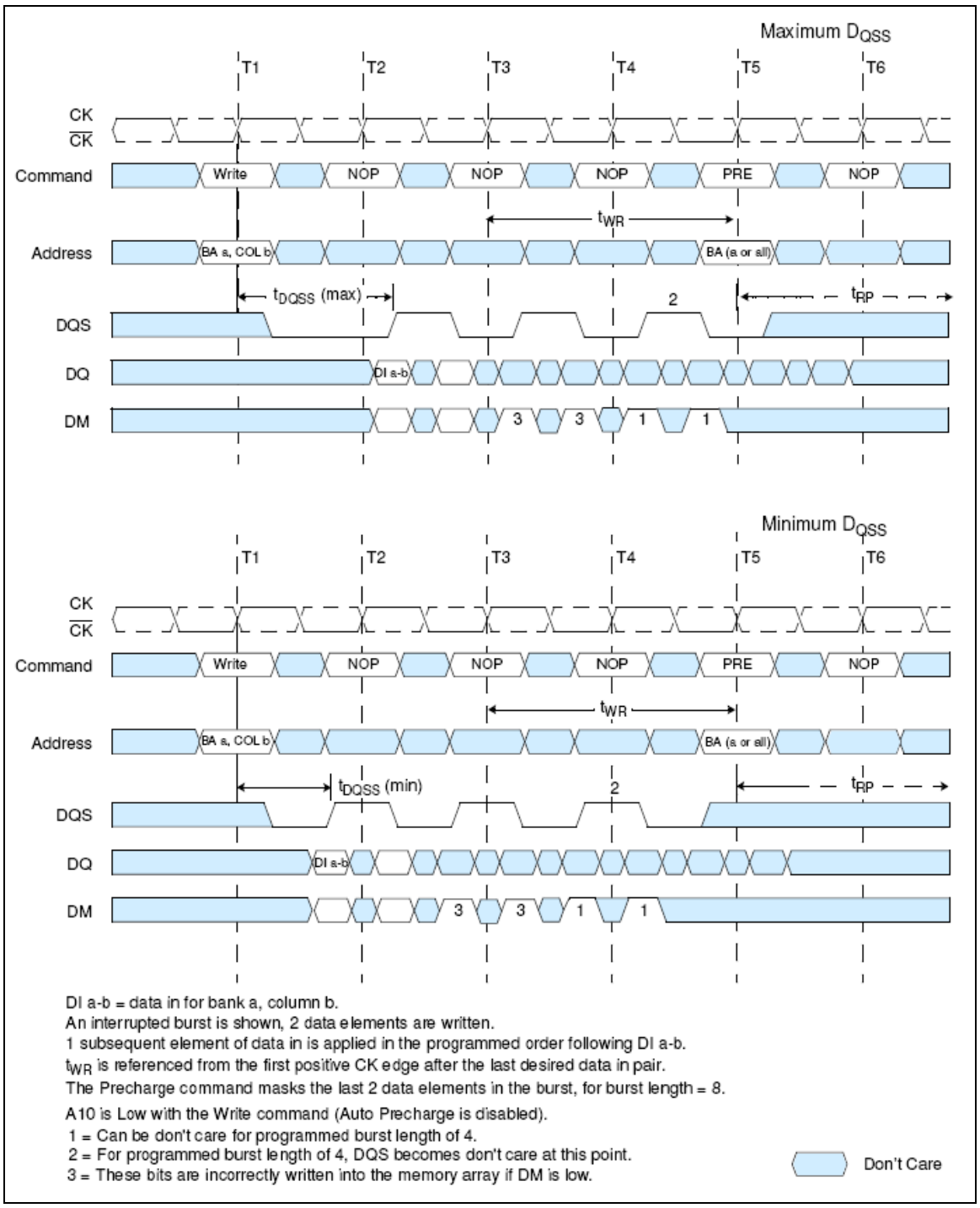
Write to Read: Nominal DQSS, Interrupting (CAS Latency = 3; Burst Length = 8)



Write to Precharge: Non-Interrupting (Burst Length = 4)



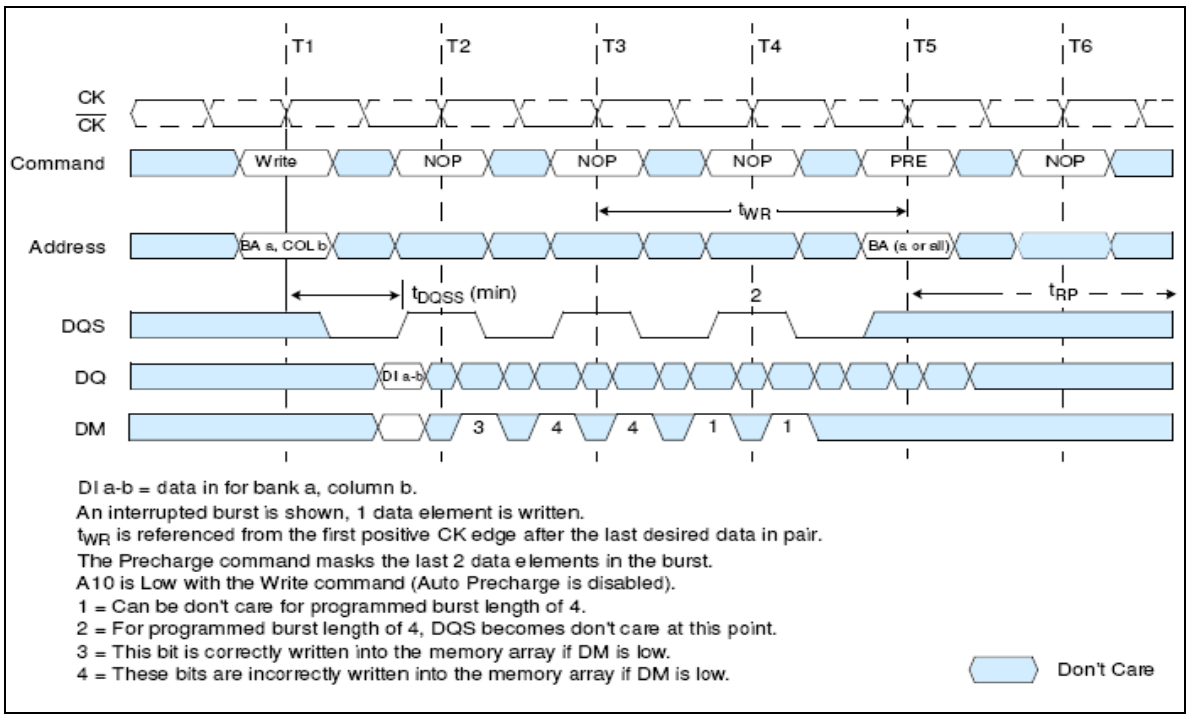
Write to Precharge: Interrupting (Burst Length = 4 or 8)



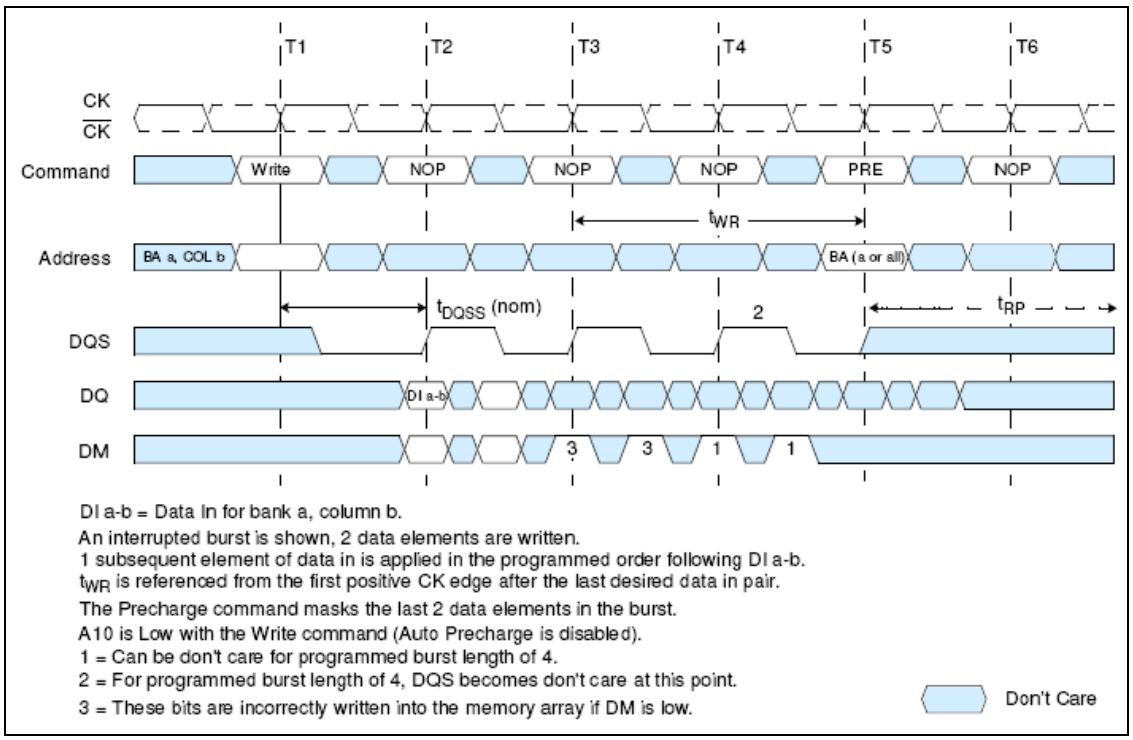
DI a-b = data in for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst, for burst length = 8.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

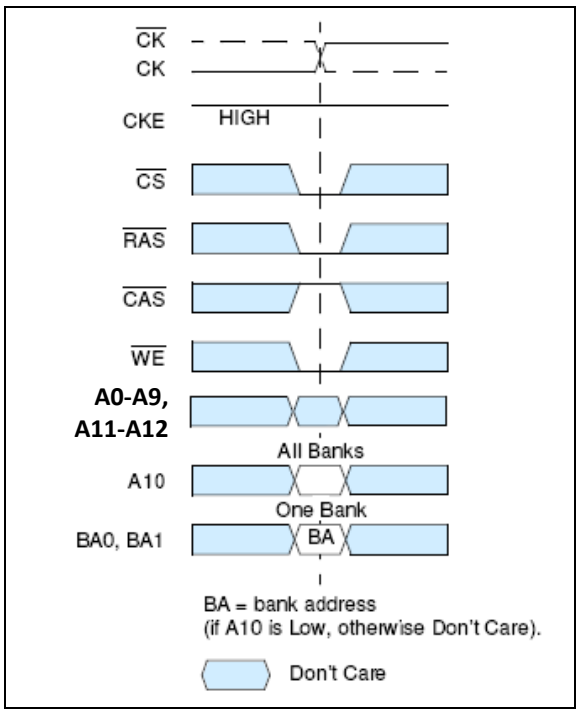
Write to Precharge: Minimum DQSS, Odd Number of Data (1 bit Write), Interrupting (Burst Length = 4 or 8)



Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)



Precharge Command



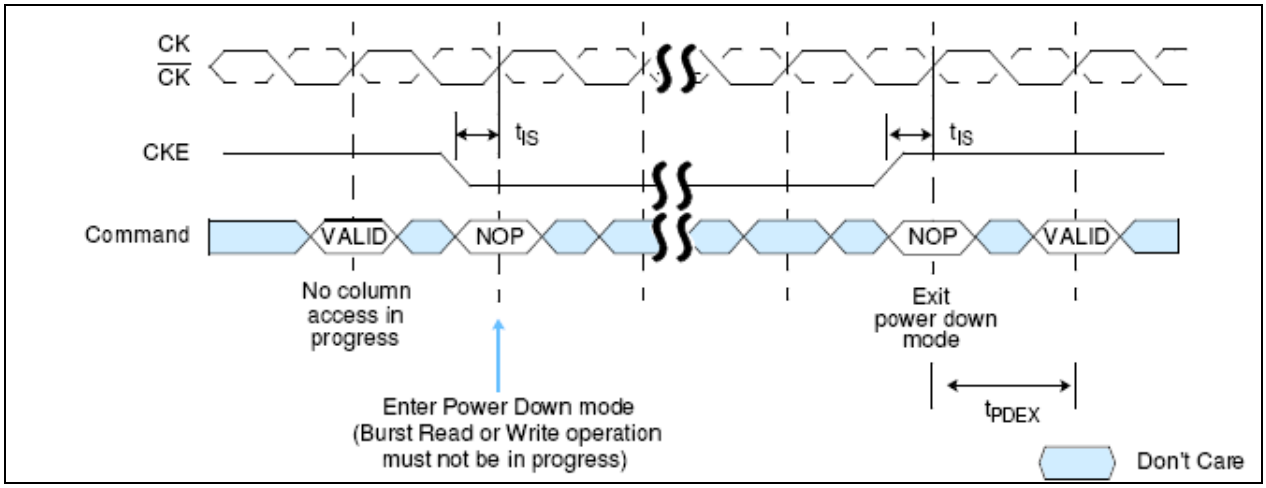
Precharge

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) is available for a subsequent row access some specified time (tRP) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.

Power Down

Power Down is entered when CKE is registered low (no accesses can be in progress). If Power Down occurs when all banks are idle, this mode is referred to as Precharge Power Down; if Power Down occurs when there is a row active in any bank, this mode is referred to as Active Power Down. Entering Power Down deactivates the input and output buffers, excluding CK, CK and CKE. The DLL is still running in Power Down mode, so for maximum power savings, the user has the option of disabling the DLL prior to entering Power Down. In that case, the DLL must be enabled after exiting Power Down, and 200 clock cycles must occur before a Read command can be issued. In Power Down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are "Don't Care". However, Power Down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled Power Down mode.

The Power Down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). A valid, executable command may be applied one clock cycle later.



Truth Table 2: Clock Enable (CKE)

Apply Note 3-6 to whole table.

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	1
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	1,2
Power Down	L	L	X	Maintain Power Down	
Power Down	L	H	Deselect or NOP	Exit Power Down	
All Banks Idle	H	L	Deselect or NOP	Precharge Power Down Entry	
All Banks Idle	H	L	Auto Refresh	Self Refresh Entry	
Bank(s) Active	H	L	Deselect or NOP	Active Power Down Entry	
	H	H	See Truth Table 3		

Notes:

1. VREF must be maintained during Self Refresh operation.
2. Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (tXSNR) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.
3. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
4. CKE n is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
5. Command n is the command registered at clock edge n, and action n is a result of command n.
6. All states and sequences not shown are illegal or reserved.
7. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Truth Table 3: Current State Banks n – Command to Bank n (Same Bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	
	L	H	H	H	No Operation	NOP. Continue previous operation	
Idle	L	L	H	H	Active	Select and activate row	
	L	L	L	H	Auto Refresh	Auto Refresh	7
	L	L	L	L	Mode Register Set	Mode Register Set	7
Row Active	L	H	L	H	Read	Select column and start Read burst	10
	L	H	L	L	Write	Select column and start Write burst	10
	L	L	H	L	Precharge	Deactivates row in bank(s)	8
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	10
	L	H	L	L	Write	Select column and start new Write burst	10,12
	L	L	H	L	Precharge	Truncate Read burst, start precharge	8
	L	H	H	L	Burst Termination	Burst Terminate	9
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	10,11
	L	H	L	L	Write	Select column and start Write burst	10
	L	L	H	L	Precharge	truncate Write burst, start precharge)	8,11

Notes:

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after tXSNR / tXSRD has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.

   Precharging: Starts with registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank is in the idle state.

   Row Activating: Starts with registration of an Active command and ends when tRCD is met. Once tRCD is met, the bank is in the "row active" state.

   Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank is in the idle state.

   Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank is in the idle state.

5. The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an Auto Refresh command and ends when tRFC is met. Once tRFC is met, the DDR SDRAM is in the “all banks idle” state.

   Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when tMRD has been met. Once tMRD is met, the DDR SDRAM is in the “all banks idle” state.

   Precharging All: Starts with registration of a Precharge All command and ends when tRP is met. Once tRP is met, all banks is in the idle state.

6. All states and sequences not shown are illegal or reserved.

7. Not bank-specific; requires that all banks are idle.

8. May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.

9. Not bank-specific; Burst terminate affects the most recent Read burst, regardless of bank.

10. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.

11. Requires appropriate DM masking.

12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command,

13. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Truth Table 4: Current State Banks n – Command to Bank m (different Bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	
	L	H	H	H	No Operation	NOP. Continue previous operation	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m		
Row Activating, Active or Precharge	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	7
	L	H	L	L	Write	Select column and start Write burst	7
	L	L	H	L	Precharge		
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	
	L	H	L	H	Read	Select column and start new Read burst	7
	L	H	L	L	Write	Select column and start new Write burst	7,9
	L	L	H	L	Precharge		
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	7,8
	L	H	L	L	Write	Select column and start Write burst	7
	L	L	H	L	Precharge		
Read (with Auto Precharge)	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	3a,7
	L	H	L	L	Write	Select column and start Write burst	3a,7,9
	L	L	H	L	Precharge		
Write (with Auto Precharge)	L	L	H	H	Active	Select and active Row	
	L	H	L	H	Read	Select column and start Read burst	3a,7
	L	H	L	L	Write	Select column and start Write burst	3a,9
	L	L	H	L	Precharge		

Notes:

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after tXSNR / tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Read with Auto Precharge Enable: See following text, notes 3a, 3b, and 3c:

   Write with Auto Precharge Enable: See following text, notes 3a, 3b, and 3c:

From Command	To Command (Different bank)	Minimum Delay Without Concurrent Auto Precharge Support	Minimum Delay WithConcurrent Auto Precharge Support	Units
Write w/AP	Read or Read w/AP	1+(BL/2) + (tWR/tCK) (rounded up)	1+(BL/2) + tWTR	tCK
	Write or Write w/AP	1+(BL/2) + (tWR/tCK) (rounded up)	BL/2	
	Precharge or Activate	1		
Read w/AP	Read or Read w/AP	BL/2		
	Write or Write w/AP	CL (rounded up) + (BL/2)		
	Precharge or Activate	1		

3a. For devices which *do not support* the optional "concurrent auto precharge" feature, the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).

3b. For devices which *do support* the optional "concurrent auto precharge" feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided.)

3c. The minimum delay from a read or write command with auto precharge enable, to a command to a different bank, is summarized below, for both cases of "concurrent auto precharge," supported or not:

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output, otherwise a Burst Terminate must be used to the READ prior to asserting a WRITE command.
10. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VIN, VOUT	Voltage on I/O pins relative to VSS	-0.5 to VDDQ+ 0.5	V
VIN	Voltage on Inputs relative to VSS	-1.0 to +3.6	V
VDD	Voltage on VDD supply relative to VSS	-1.0 to +3.6	V
VDDQ	Voltage on VDDQ supply relative to VSS	-1.0 to +3.6	V
TSTG	Storage Temperature (Plastic)	-55 to +150	℃
PD	Power Dissipation	1.0	W
IOUT	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Ambient operating temperatures

Symbol	Parameter	Grade	Range
TA	Ambient operating temperatures	Commercial	0℃ to 70℃
		Industrial	-40℃ to 85℃

Capacitance

Parameter	Symbol	Max.	Units	Notes
Input Capacitance: CK, $\overline{CK}$	CI1	3.0	pF	1
Delta Input Capacitance: CK, $\overline{CK}$	delta CI1	0.25	pF	1
Input Capacitance: All other input-only pins (except DM)	CI2	3.0	pF	1
Delta Input Capacitance: All other input-only pins (except DM)	delta CI2	0.5	pF	1
Input/Output Capacitance: DQ, DQS, DM	CIO	5.0	pF	1,2
Delta Input/Output Capacitance: DQ, DQS, DM	delta CIO	0.5	pF	1

1. VDDQ = VDD = 2.5V ± 0.2V (DDR333); 2.6V ± 0.1V (DDR400) (minimum range to maximum range), f = 100MHz, TA = 25°C, VODC = VDDQ/2, VOPeak -Peak = 0.2V.
2. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match input propagation times of DQ, DQS and DM in the system.

DC Electrical Characteristics and Operating Conditions

(For DDR333, V_{DDQ} = V_{DD} = +2.5V±0.2V; For DDR400, V_{DDQ} = V_{DD} = + 2.6V ± 0.1V)

Symbol	Parameter	Min		Max	Units	Notes
		DDR333	DDR400			
VDD	Supply Voltage	2.3	2.5	2.7	V	1
VDDQ	I/O Supply Voltage	2.3	2.5	2.7	V	1
VREF	I/O Reference Voltage	0.49 x VDDQ		0.51 x VDDQ	V	1,2
VTT	I/O Termination Voltage (System)	VREF - 0.04		VREF + 0.04	V	1,3
VIH(DC)	Input High (Logic1) Voltage	VREF + 0.15		VDD + 0.3	V	1
VIL(DC)	Input Low (Logic0) Voltage	- 0.3		VREF - 0.15	V	1
VIN(DC)	Input Voltage Level, CK and $\overline{CK}$ Inputs	- 0.3		VDDQ + 0.3	V	1
VID(DC)	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.36		VDDQ + 0.6	V	1,4
II	Input Leakage Current Any input 0V ≦ VIN ≦ VDD; (All other pins not under test = 0V)	-2		2	µA	
IOZ	Output Leakage Current (DQs are disabled; 0V ≦ Vout ≦ VDDQ	-5		5	µA	1

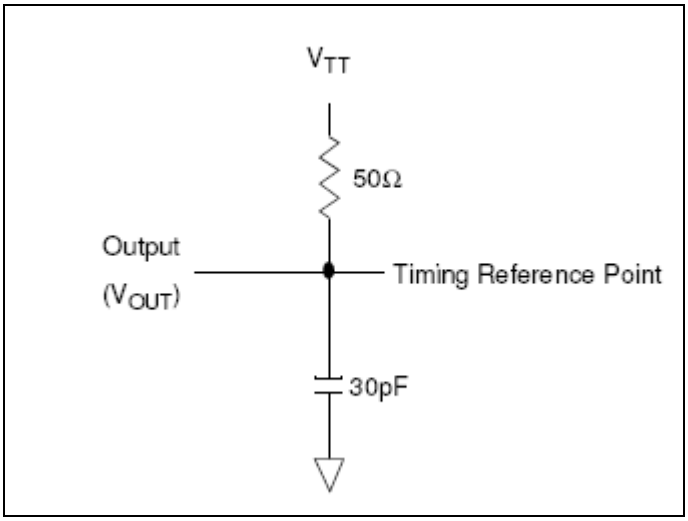
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK.
5. The ratio of the pull-up current to the pull down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pull-up and pull down drivers due to process variation.

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between V_{IL} (AC) and V_{IH} (AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.

AC Output Load Circuit Diagrams



AC Input Operating Conditions

(V_{DDQ} = V_{DD} = + 2.5V ± 0.2V (DDR333); + 2.6V ± 0.1V (DDR400);

Symbol	Parameter / Condition	Min	Max	Unit	Note
$V_{IH(AC)}$	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	V_{REF} + 0.31	-	V	1,2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals	-	V_{REF} – 0.31	V	1,2
$V_{ID(AC)}$	Input Differential Voltage, CK and CK Inputs	0.7	V_{DDQ} + 0.6	V	1,2,3
$V_{IX(AC)}$	Input Crossing Point Voltage, CK and CK Inputs	0.5*V_{DDQ} – 0.2	0.5*V_{DDQ} + 0.2	V	1,2,4

1. Input slew rate = 1V/ns.

2. Inputs are not recognized as valid until V_{REF} stabilizes.

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK.

4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

IDD TEST CONDITIONS

Symbol	Conditions

IDD0	**Operating current for one bank active-precharge;**
	tRC = tRC(min);
	tCK = 6 ns for DDR333, 5 ns for DDR400;
	DQ, DM and DQS inputs changing once per clock cycle;
	address and control inputs changing once every two clock cycles;
	$\overline{CS}$ = high between valid commands.

IDD1	**Operating current for one bank operation;** one bank open, BL = 4, reads (Refer to the following page for detailed test conditions) $\overline{CS}$ = high between valid commands.
IDD2P	**Precharge power-down standby current;** all banks idle; power-down mode; CKE ≤ VIL(max); tCK = 6 ns for DDR333, 5 ns for DDR400; VIN = VREF for DQ, DQS and DM
IDD2F	**Precharge floating standby current;** $\overline{CS}$ ≥ VIH(min); all banks idle; CKE ≥ VIH(min); tCK = 6 ns for DDR333, 5 ns for DDR400; address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS and DM
IDD2Q	**Precharge quiet standby current;** $\overline{CS}$ ≥ VIH(min); all banks idle; CKE ≥ VIH(min); tCK = 6 ns for DDR333, 5 ns for DDR400; address and other control inputs stable at >= VIH(min) or <= VIL (max); VIN = VREF for DQ, DQS and DM
IDD3P	**Active power-down standby current ;** one bank active; power-down mode; CKE ≤ VIL(max); tCK = 6 ns for DDR333, 5 ns for DDR400; VIN = VREF for DQ, DQS and DM

IDD3N	**Active standby current;**
	$\overline{CS}$ ≥ VIH(min);
	CKE ≥ VIH(min);
	one bank active; tRC = tRAS(max);
	tCK = 6 ns for DDR333, 5 ns for DDR400;
	DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle

IDD4R	**Operating current for burst read;** burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; CL = 2.5 at tCK = 6 ns for DDR333, 5 ns for DDR400; 50% of data changing on every transfer; lOUT = 0mA

IDD4W	**Operating current for burst write;** burst length = 2; writes; continuous burst; one bank active; address and control inputs changing once per clock cycle; CL = 2.5 at tCK = 6 ns for DDR333, 5 ns for DDR400; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer
IDD5	**Auto refresh current;** tRC = tRFC(min) which is 12 * tCK for DDR333 at tCK = 6ns; 14 * tCK for DDR400 at tCK = 5ns; IDD5: tRC = tRFC = # of clocks is for 512 Mb devices and smaller.
IDD6	**Self refresh current;** CKE ≤ 0.2 V; external clock on; tCK = 6ns for DDR333, 5 ns for DDR400
IDD7	**Operating current for four bank operation;** four bank interleaving with BL = 4 (Refer to the following page for detailed test condition)

1. Typical case : For DDR200, 266, and 333: VDD = 2.5 V, T = 25℃; For DDR400: VDD = 2.6 V, T = 25 ℃
2. Worst case : VDD = 2.7 V, T = 10 ℃
3. Self refresh: normal/low power respectively
4. Measured values for all items will be averaged from repeated cycles with the above description

DETAILED test conditons for IDD1 and IDD7

Typical Case:

- For DDR333: VDD = 2.5 V, T = 25℃;

- For DDR400: VDD = 2.6 V, T = 25℃

Worst Case:

- VDD = 2.7 V, T = 10℃

Legend: A = Active, R = Read, RA = Read with Autoprecharge, P = Precharge, N = DESELECT

IDD1 : Operating current: One bank operation

Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs change logic state once per Deselect cycle.

IOUT = 0mA

Timing patterns

- DDR333 (167 MHz, CL = 2.5): tCK = 6 ns, BL = 4, tRCD = 3 * tCK, tRC = 10 * tCK, tRAS = 7 * tCK

  Setup:A0 N N R0 N N N P0 N N

  Read: A0 N N R0 N N N P0 N N -repeat the same timing with random address changing 50% of data changing at every transfer

- DDR400 (200 MHz, CL = 3): tCK = 5 ns, BL = 4, tRCD = 3 * tCK, tRC = 11 * tCK, tRAS = 8 * tCK

  Setup:A0 N N R0 N N N N P0 N N

  Read: A0 N N R0 N N N N P0 N N -repeat the same timing with random address changing 50% of data changing at every transfer

IDD7 : Operating current: Four bank operation

Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on Deselect edge are not changing. lOUT = 0mA

Timing patterns

- DDR333 (167 MHz, CL = 2.5): tCK = 6 ns, BL = 4, tRRD = 2 * tCK, tRCD = 3 * tCK, tRAS = 7 * tCK

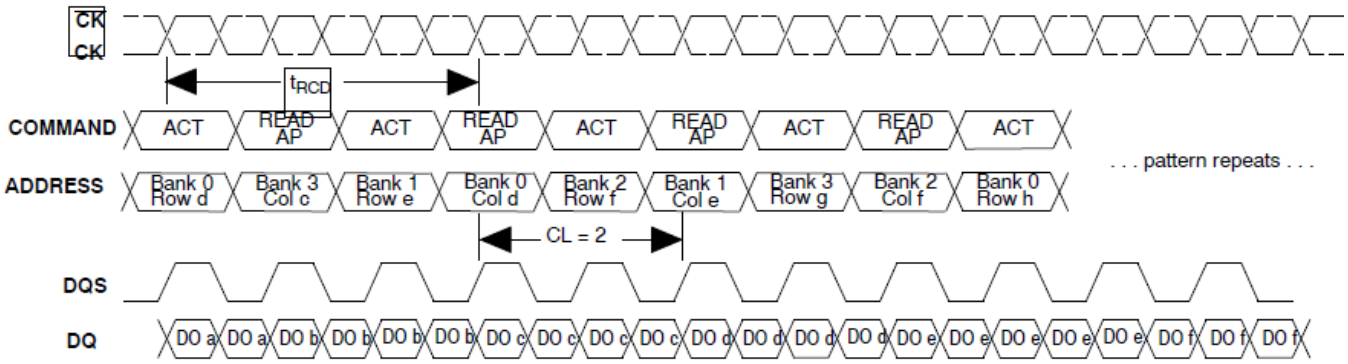
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3

  Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing 50% of data changing at every transfer

- DDR400 (200 MHz, CL = 3): tCK = 5 ns, BL = 4, tRRD = 2 * tCK, tRCD = 3 * tCK, tRAS = 8 * tCK

  Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N

  Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N - repeat the same timing with random address changing 50% of data changing at every transfer



Timing waveform for IDD7 measurement at 100 MHz Ck operation

IDD SPECIFICATION

Parameter	Conditions	DDR-400 X8		DDR-400 X16		Unit
		Typical	Max	Typical	Max	
IDD0	Operating current for one bank active-precharge	63	70	65	80	mA
IDD1	Operating current for one bank operation	65	80	70	90	mA
IDD2P	Precharge power-down standby current	8	10	8	10	mA
IDD2F	Precharge floating standby current	26	33	26	35	mA
IDD2Q	Precharge quiet standby current	26	33	26	35	mA
IDD3P	Active power-down standby current	18	25	18	25	mA
IDD3N	Active standby current	40	50	45	55	mA
IDD4R	Operating current for burst read	80	95	85	115	mA
IDD4W	Operating current for burst write	85	100	100	120	mA
IDD5	Auto refresh current	110	120	110	120	mA
IDD6	Self refresh current	8	10	8	10	mA
IDD7	Operating current for four bank operation	165	180	170	200	mA

Electrical Characteristics & AC Timing - Absolute Specifications

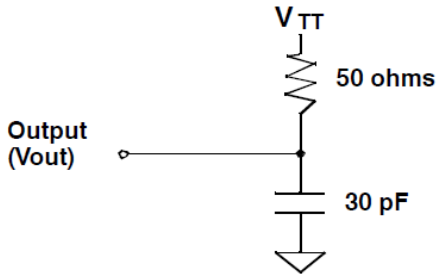
(V_{DDQ} = V_{DD} = + 2.5V ± 0.2V (DDR333); + 2.6V ± 0.1V (DDR400); See AC Characteristics)

Symbol	Parameter		DDR333		DDR400		Unit	Notes
			Min	Max	Min	Max		
tAC	DQ output access time from CK/$\overline{CK}$		− 0.70	+0.7	− 0.70	+ 0.7	ns	
tDQSCK	DQS output access time from CK/$\overline{CK}$		− 0.60	+ 0.60	− 0.60	+ 0.60	ns	
tCH	CK high-level width		0.45	0.55	0.45	0.55	tCK	
tCL	CK low-level width		0.45	0.55	0.45	0.55	tCK	
tHP	CK half period		min (tCL, tCH)	-	min (tCL, tCH)	-	ns	24,25
tCK	Clock cycle time	CL=2.5	6	12	6	12	ns	30
		CL=3	6	12	5	12	ns	
tDH	DQ and DM input hold time		0.45	-	0.4	-	ns	j,k,31
tDS	DQ and DM input setup time		0.45	-	0.4	-	ns	j,k,31
tIPW	Input pulse width		2.2	-	2.2	-	ns	22
tDIPW	DQ and DM input pulse width		1.75	-	1.75	-	ns	22
tHZ	Data-out high-impedance time from CK/$\overline{CK}$		-	0.7	-	0.7	ns	15
tLZ	Data-out low-impedance time from CK/$\overline{CK}$		− 0.7	0.7	− 0.7	0.7	ns	15
tDQSQ	DQS & associated DQ signals skew		-	0.45	-	0.4	ns	26
tQH	Data output hold time from DQS		tHP - tQHS	-	tHP - tQHS	-	ns	25
tQHS	Data hold Skew Factor		-	0.55	-	0.5	ns	25
tDQSS	write command to 1st DQS latching		0.75	1.25	0.72	1.25	tCK	
tDQSH	DQS input high pulse width		0.35	-	0.35	-	tCK	
tDQSL	DQS input low pulse width		0.35	-	0.35	-	tCK	
tDSS	DQS falling edge to CK setup time		0.2	-	0.2	-	tCK	
tDSH	DQS falling edge hold time from CK		0.2	-	0.2	-	tCK	
tMRD	Mode register set command cycle time		2	-	2	-	tCK	
tWPRES	write preamble setup time		0	-	0	-	ns	17
tWPST	write postamble		0.4	0.6	0.4	0.6	tCK	16
tWPRE	write preamble		0.25	-	max(0.25 * tCK,1.5ns)	-	tCK	8
tIH	Address and control input hold time(fast slew rate)		0.75	-	0.6	-	ns	i, 19, 21-23
tIS	Address and control input setup time(fast slew rate)		0.75	-	0.6	-	ns	i, 19, 21-23
tIH	Address and control input hold time(slow slew rate)		0.8	-	0.7	-	ns	i, 20-23
tIS	Address and control input setup time(slow slew rate)		0.8	-	0.7	-	ns	i, 20-23

Symbol	Parameter		DDR333		DDR400		Unit	Notes
			Min	Max	Min	Max		
tRPRE	Read preamble		0.9	1.1	0.9	1.1	tCK	28, 33
tRPRES	Read preamble setup time(Optional CL=1.5)		-	N/A	-	N/A	ns	28
tRPST	Read postamble		0.4	0.6	0.4	0.6	tCK	33
tRAS	Active to Precharge		42	70K	40	70K	ns	
tRC	Active to Active/Auto-refresh command period		60	-	55	-	ns	
tRFC	Auto-refresh to Active/Auto-refresh command period		72	-	70	-	ns	
tRCD	Active to Read or write delay		18	-	15	-	ns	
tRP	Precharge command period		18	-	15	-	ns	
tRAP	Active to Read Command with Auto Precharge		tRCD	-	tRCD	-	ns	
tRRD	Active bank A to Active bank B command		12	-	10	-	ns	
tWR	write recovery time		15	-	15	-	ns	
tDAL	Auto precharge write recovery + precharge time		-	-	-	-	tCK	27
tWTR	Internal write to read command delay	CL= 1.5	N/A	-	N/A	-	tCK	
		CL=2.5	1	-	2	-	tCK	
		CL=3	1	-	2	-	tCK	
tXSNR	Exit self-refresh to non-read command		75	-	75	-	ns	29
tXSRD	Exit self-refresh to read command		200	-	200	-	tCK	
tREFI	Average Periodic Refresh Interval		-	7.8	-	7.8	µs	18, 31

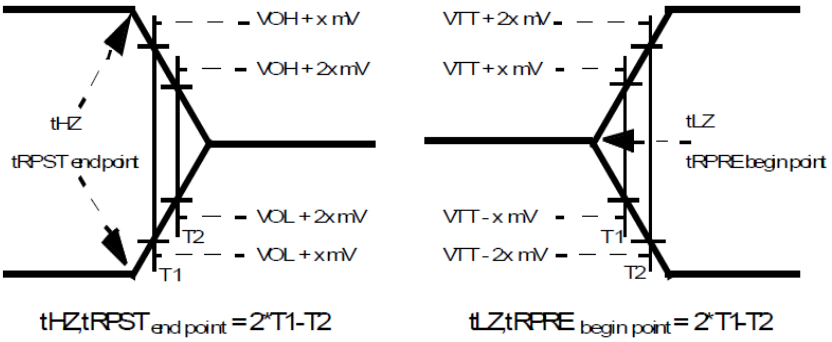
Notes

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. The timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).



4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK,$\overline{CK}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.2VDDQ is recognized as LOW.
7. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak-to-peak noise on VREF may not exceed +/-2% of the dc value.
8. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF.
9. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
10. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
11. Enables on-chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized.
13. The CK, $\overline{CK}$ input reference level (for timing referenced to CK, $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK, $\overline{CK}$, is VREF.
14. The output timing reference voltage level is VTT.

15. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). Calculate the point when the device is no longer driving (tHZ) or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
17. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
18. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
19. For command/address input slew rate ≥1.0 V/ns
20. For command/address input slew rate ≥0.5 V/ns and <1.0 V/ns
21. For CK & $\overline{CK}$ slew rate ≥1.0 V/ns (single-ended)
22. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
23. Slew Rate is measured between VOH(ac) and VOL(ac).
24. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
25. tQH = tHP - tQHS, where: tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQon the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
26. tDQSQ Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
27. tDAL = (tWR/tCK) + (tRP/tCK**)** For each of the terms above, if not already an integer, round to the next highest integer.
28. Optional CAS Latency, 1.5, is only defined for DDR200 speed grade
29. In all circumstances, tXSNR can be satisfied using tXSNR = tRFCmin + 1*tCK
30. The only time that the clock frequency is allowed to change is during self-refresh mode

31. If refresh timing or tDS/tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
32. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
33. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Calculate the point when the device is no longer driving (tRPST) or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

SYSTEM CHARACTERISTICS for DDR SDRAMS

These characteristics are for system simulation purposes and are guaranteed by design.

Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS	SYMBOL	DDR400		DDR333		UNITS	NOTES
PARAMETER		MIN	MAX	MIN	MAX		
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	0.4	0.5	0.4	V/ns	a, m

Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	△tIS	△tIH	UNITS	NOTES
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Input/Output Setup & Hold Time Derating for Slew Rate

I/O Input Slew Rate	△tDS	△tDH	UNITS	NOTES
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	△tDS	△tDH	UNITS	NOTES
±0.0 ns/V	0	0	ps	j
±0.25 ns/V	+50	+50	ps	j
±0.5 ns/V	+100	+100	ps	j

Output Slew Rate Characteristics (X4, X8 Devices only)

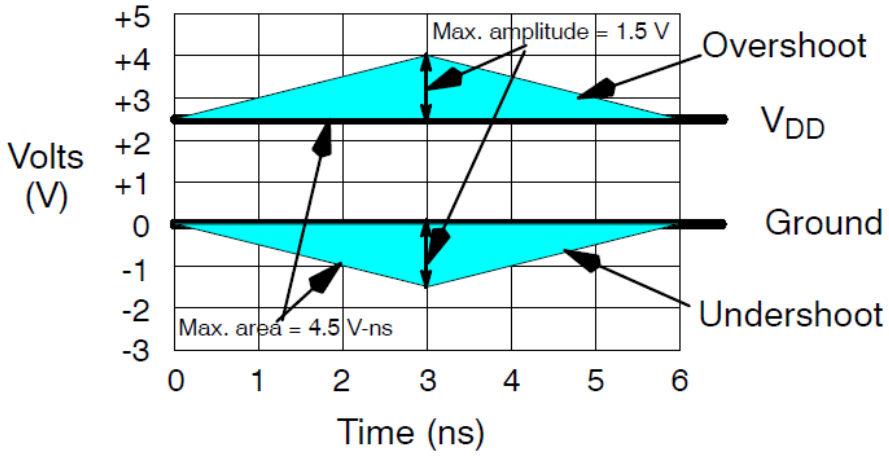
Slew Rate Characteristic	Typical Range(V/ns)	Minimum(V/ns)	Maximum(V/ns)	NOTES
Pullup Slew Rate	1.2 - 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown Slew Rate	1.2 - 2.5	1.0	4.5	b,c,d,f,g,h

Output Slew Rate Characteristics (X16 Devices only)

Slew Rate Characteristic	Typical Range(V/ns)	Minimum(V/ns)	Maximum(V/ns)	NOTES
Pullup Slew Rate	1.2 - 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown Slew Rate	1.2 - 2.5	0.7	5.0	b,c,d,f,g,h

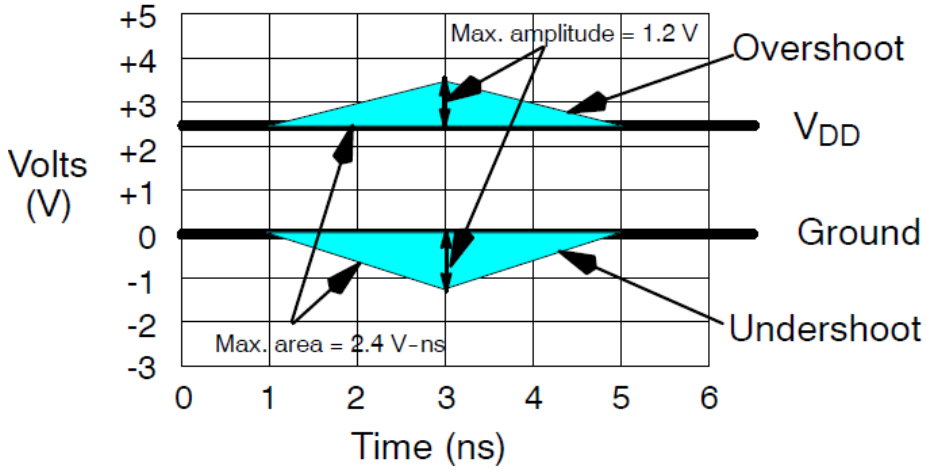
AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	Specification
	DDR333/400
Maximum peak amplitude allowed for overshoot	1.5 V
Maximum peak amplitude allowed for undershoot	1.5 V
The area between the overshoot signal and VDD must be less than or equal to	4.5 V-ns
The area between the undershoot signal and GND must be less than or equal to	4.5 V-ns



Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins

Parameter	Specification
	DDR333/400
Maximum peak amplitude allowed for overshoot	1.2 V
Maximum peak amplitude allowed for undershoot	1.2 V
The area between the overshoot signal and VDD must be less than or equal to	2.4 V-ns
The area between the undershoot signal and GND must be less than or equal to	2.4 V-ns



Clamp V-I Characteristics for Address, Control and Data Pins

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0.1
0.8	0.1	0.6
0.9	1	1.8
1.0	2.5	3.4
1.1	4.7	5.6
1.2	6.8	7.6
1.3	9.1	10
1.4	11	13
1.5	13.5	15.4
1.6	16	18
1.7	18.2	21.6
1.8	21	25
1.9	23.3	28
2.0	26	31
2.1	28.2	34.4
2.2	31	38
2.3	33	42
2.4	35	46
2.5	37	50

System Notes:

a. Pullup slew rate is characterized under the test conditions as shown in Figure 39.

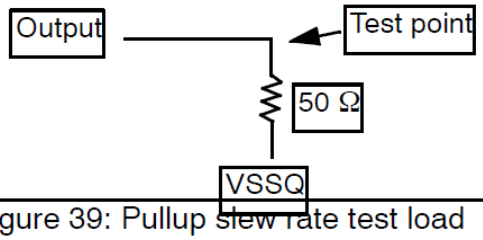


Figure 39: Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 40.

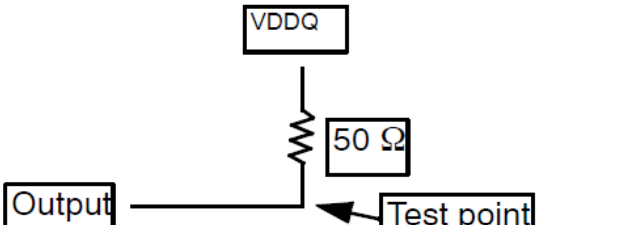


Figure 40: Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV±250 mV)

Pulldown slew rate is measured between (VDDQ/2 + 320 mV±250 mV)

Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew rate, DQ0 is switching

For minimum slew rate, all DQ bits are switching worst case pattern

For maximum slew rate, only one DQ is switching from either high to low, or low to high.

The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions

Typical: 25 °C (T Ambient), VDDQ = nominal, typical process

Minimum: 70 °C (T Ambient), VDDQ = minimum, slow-slow process

Maximum: 0 °C (T Ambient), VDDQ = maximum, fast-fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package devices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. A derating factor applies to speed bins DDR200, DDR266, and DDR333.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

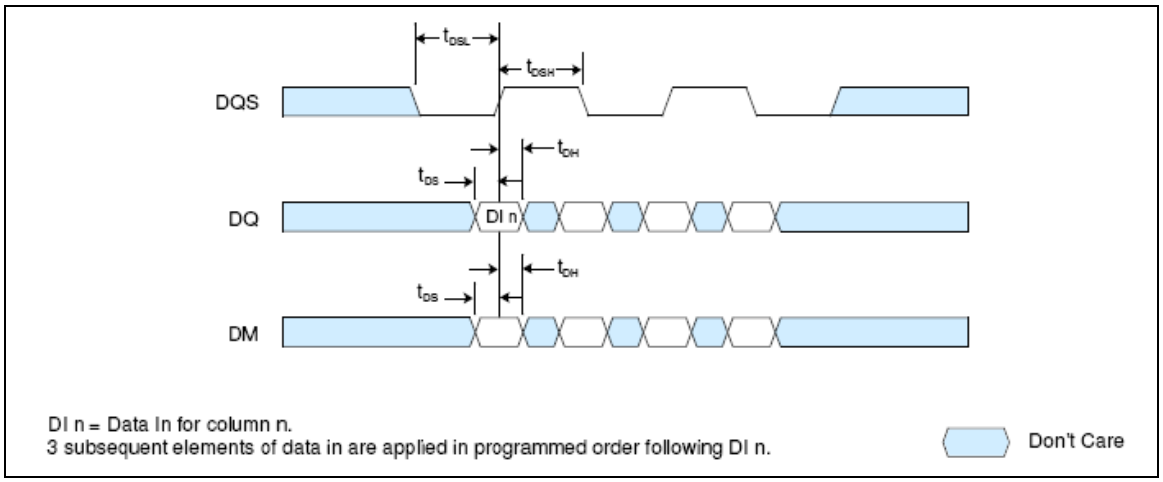
The delta rise/fall rate is calculated as:
{1/(Slew Rate1)}-{1/(slew Rate2)}

For example: If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise,fall rate is -0.5 ns/V. Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps. A derating factor applies to speed bins DDR200, DDR266, and DDR333.

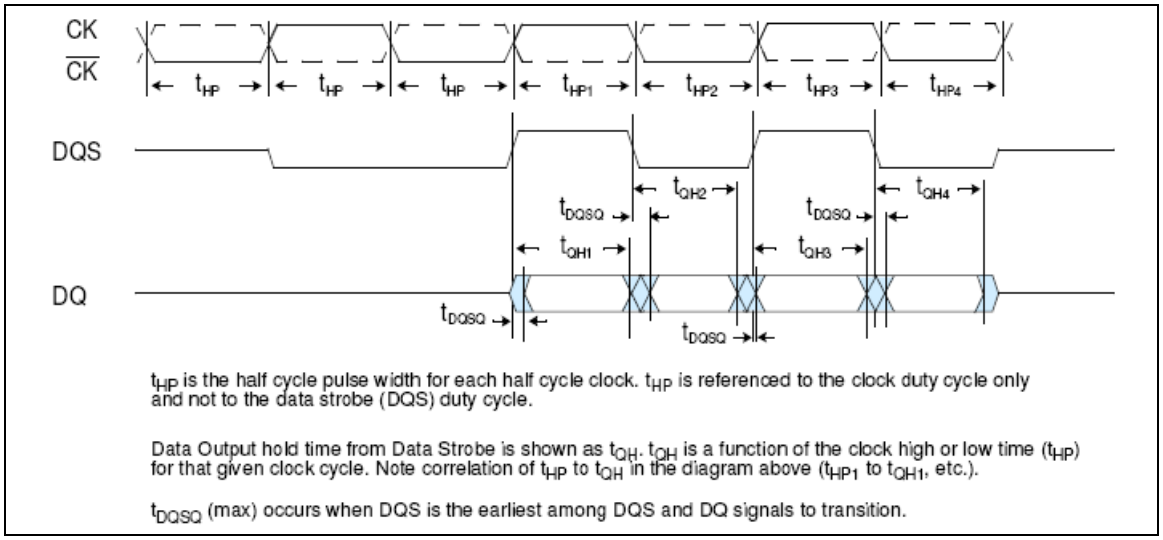
k. Table is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(AC) or VIH(DC) to VIL(DC), and similarly for rising transitions. A derating factor applies to speed bins DDR200, DDR266, and DDR333.

l. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

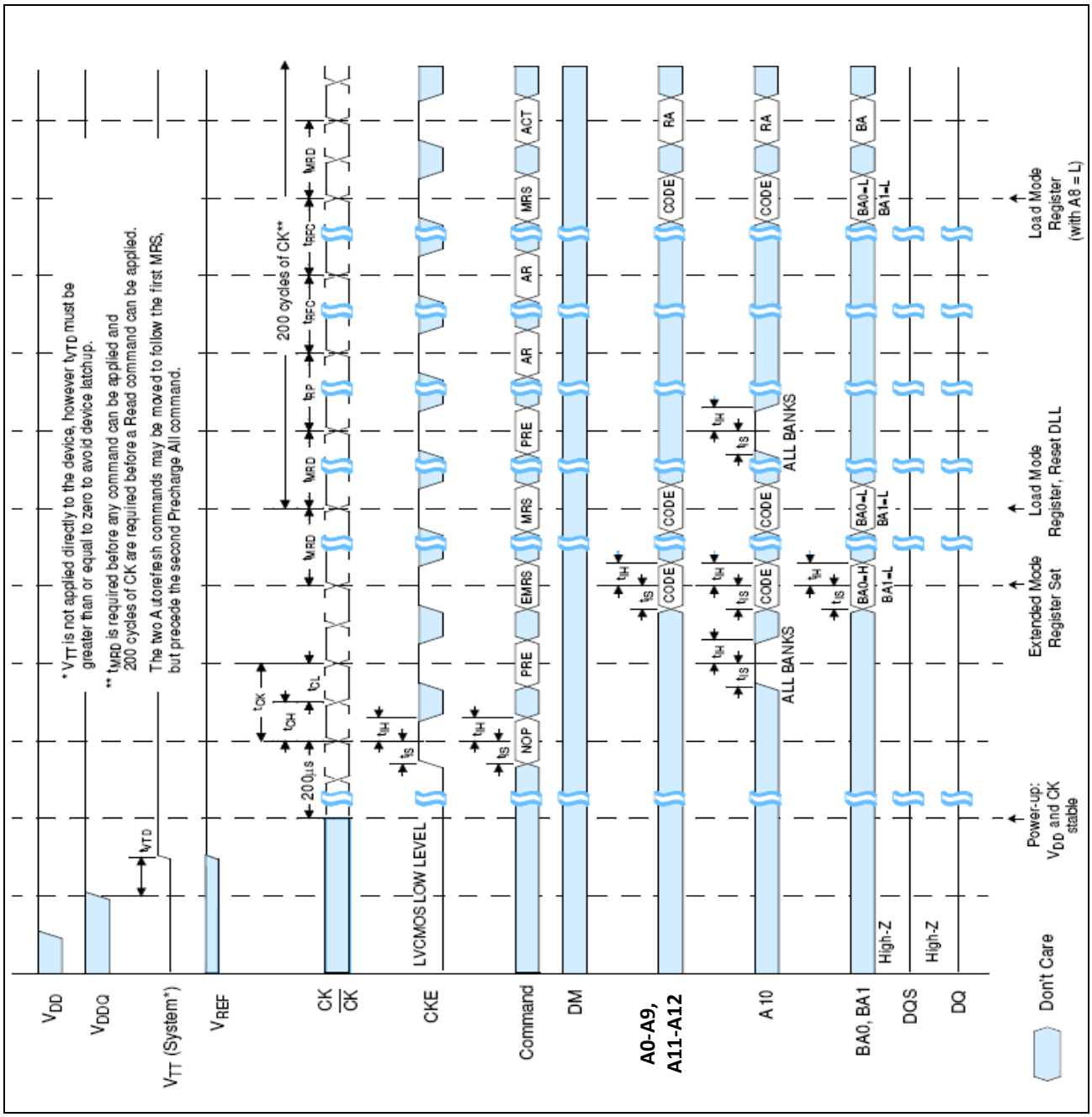
Data Input (Write) (Timing Burst Length =4)



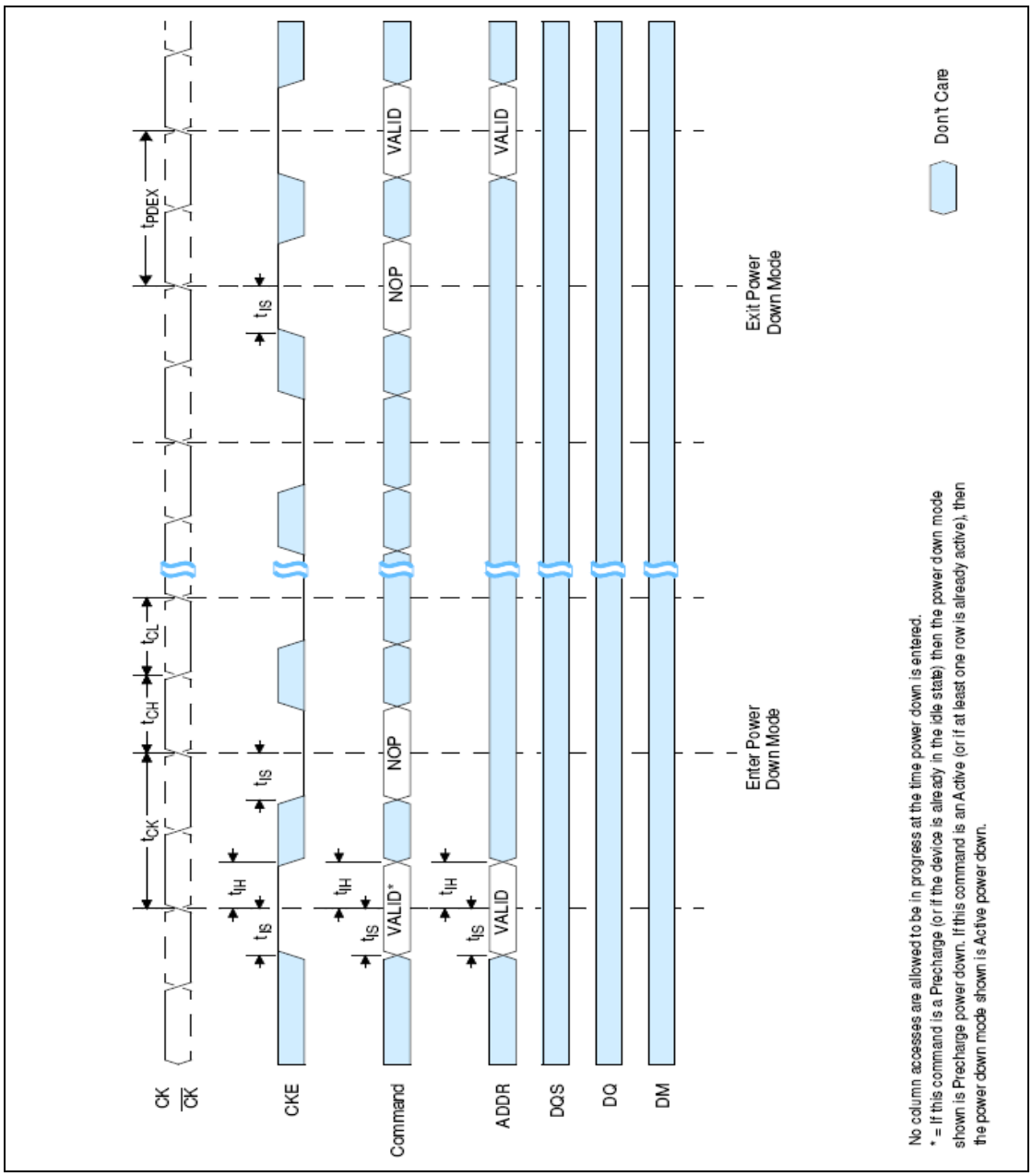
Data Output (Read) (Timing Burst Length =4)



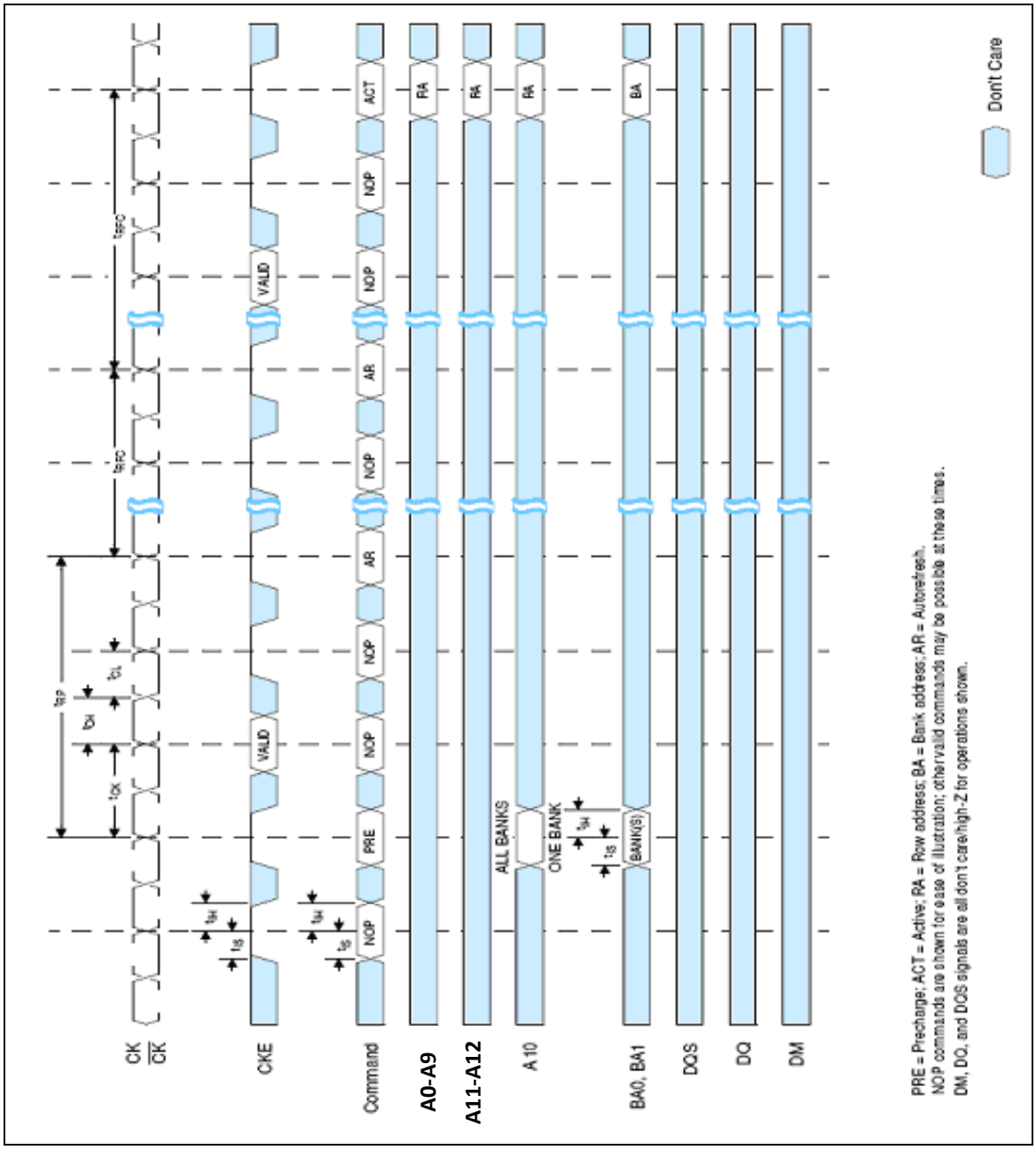
Initialize and Mode Register Set



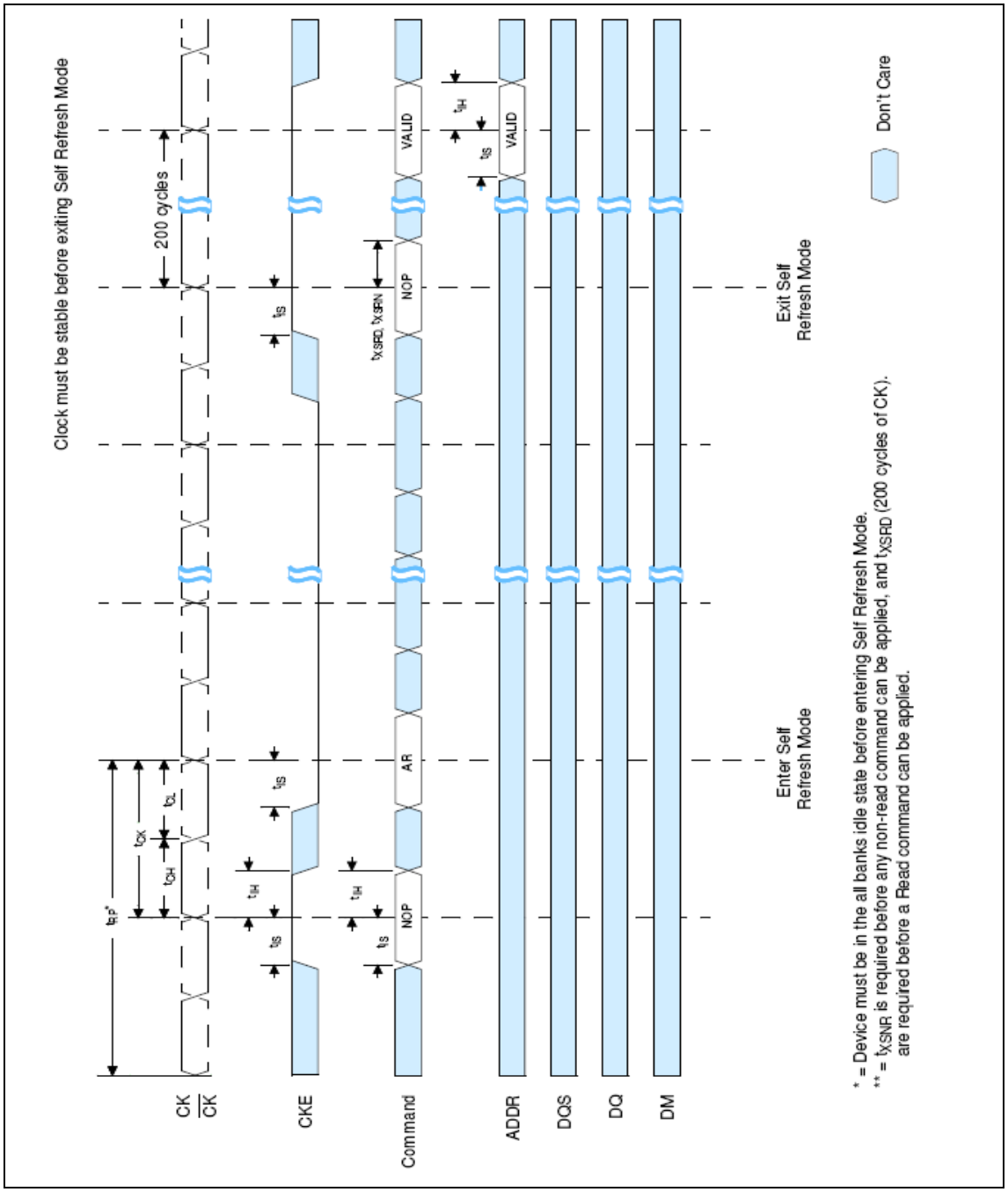
Power Down Mode



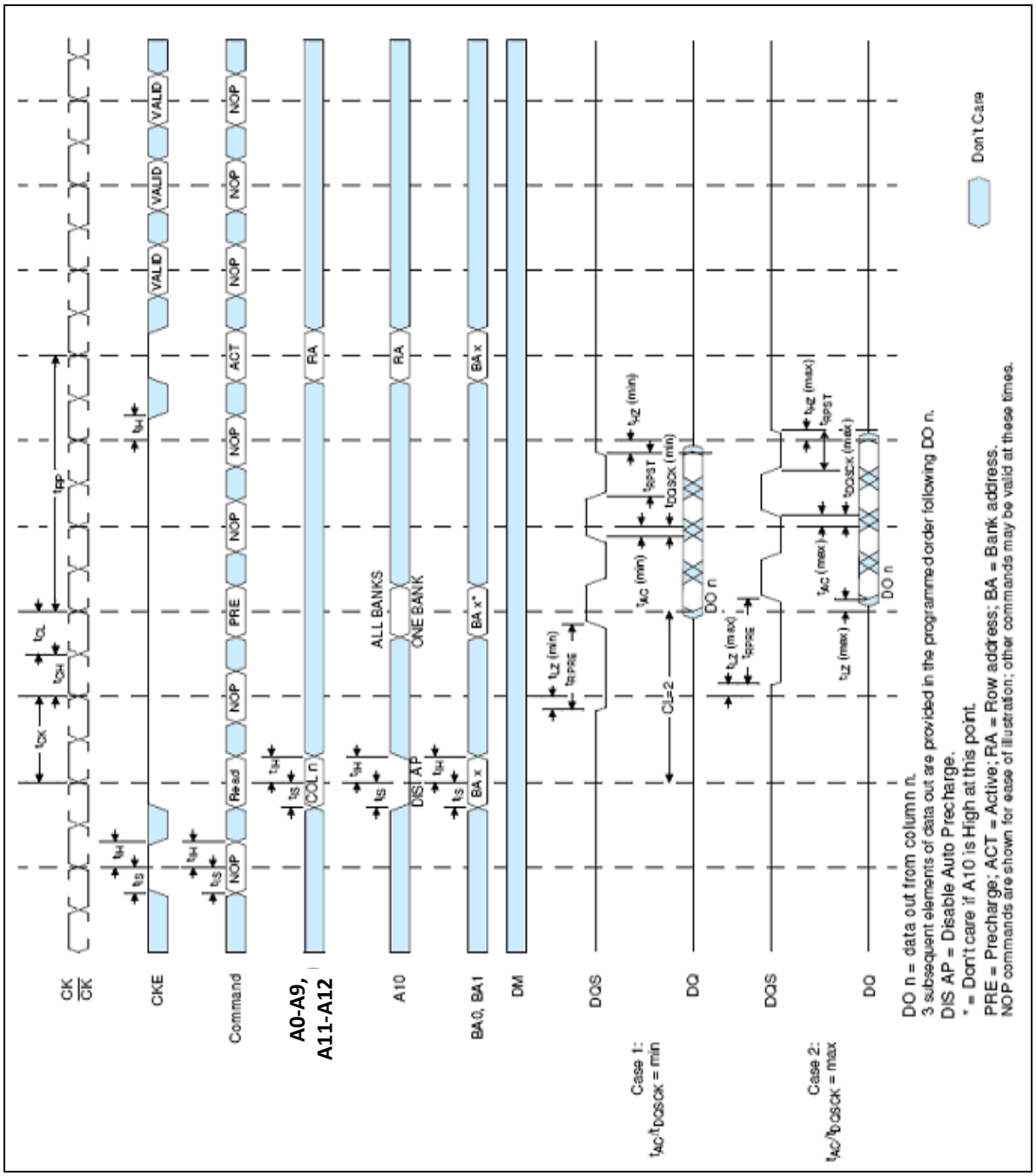
Auto Refresh



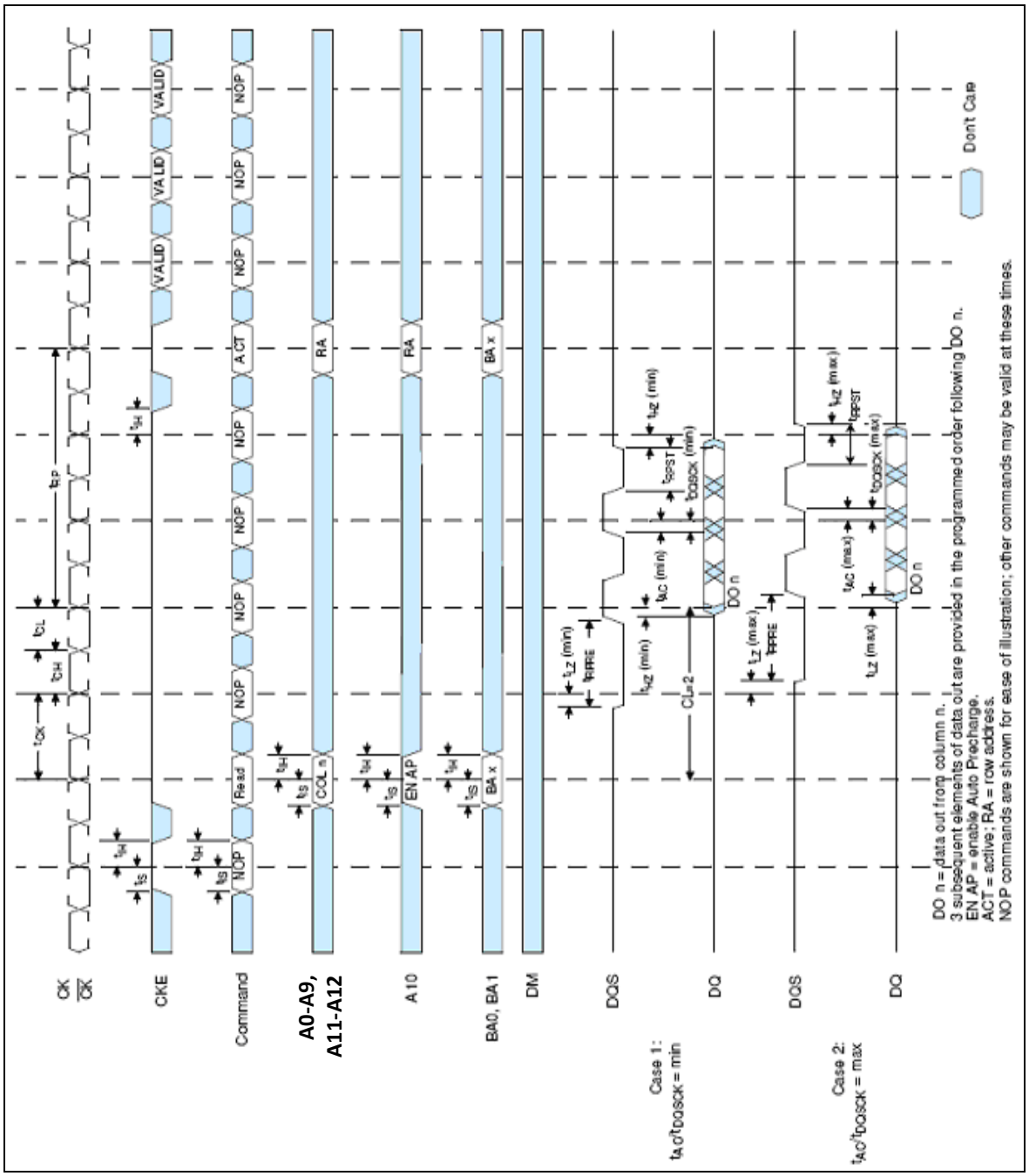
Self Refresh Mode



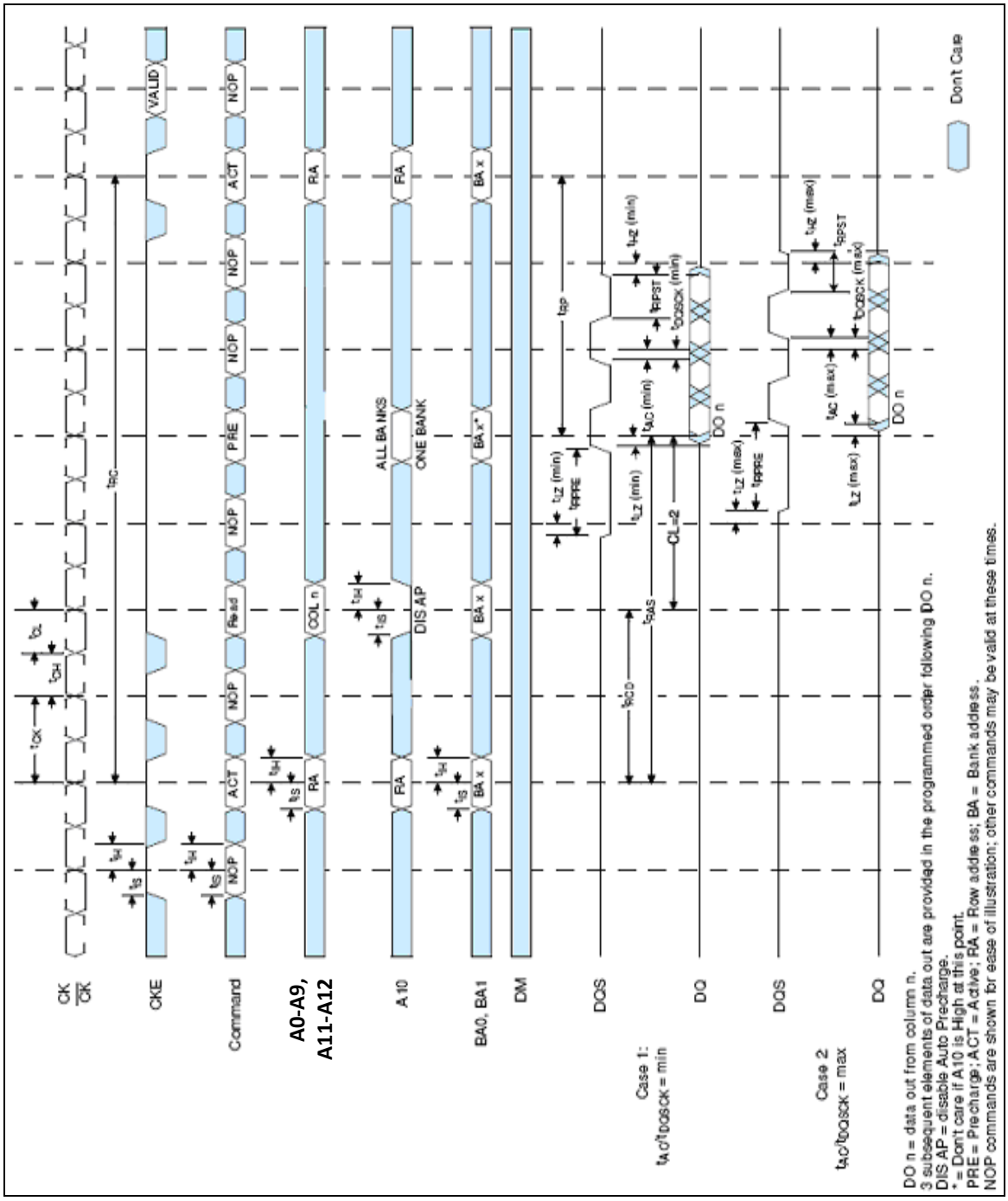
Read without Auto Precharge (Burst Length = 4)



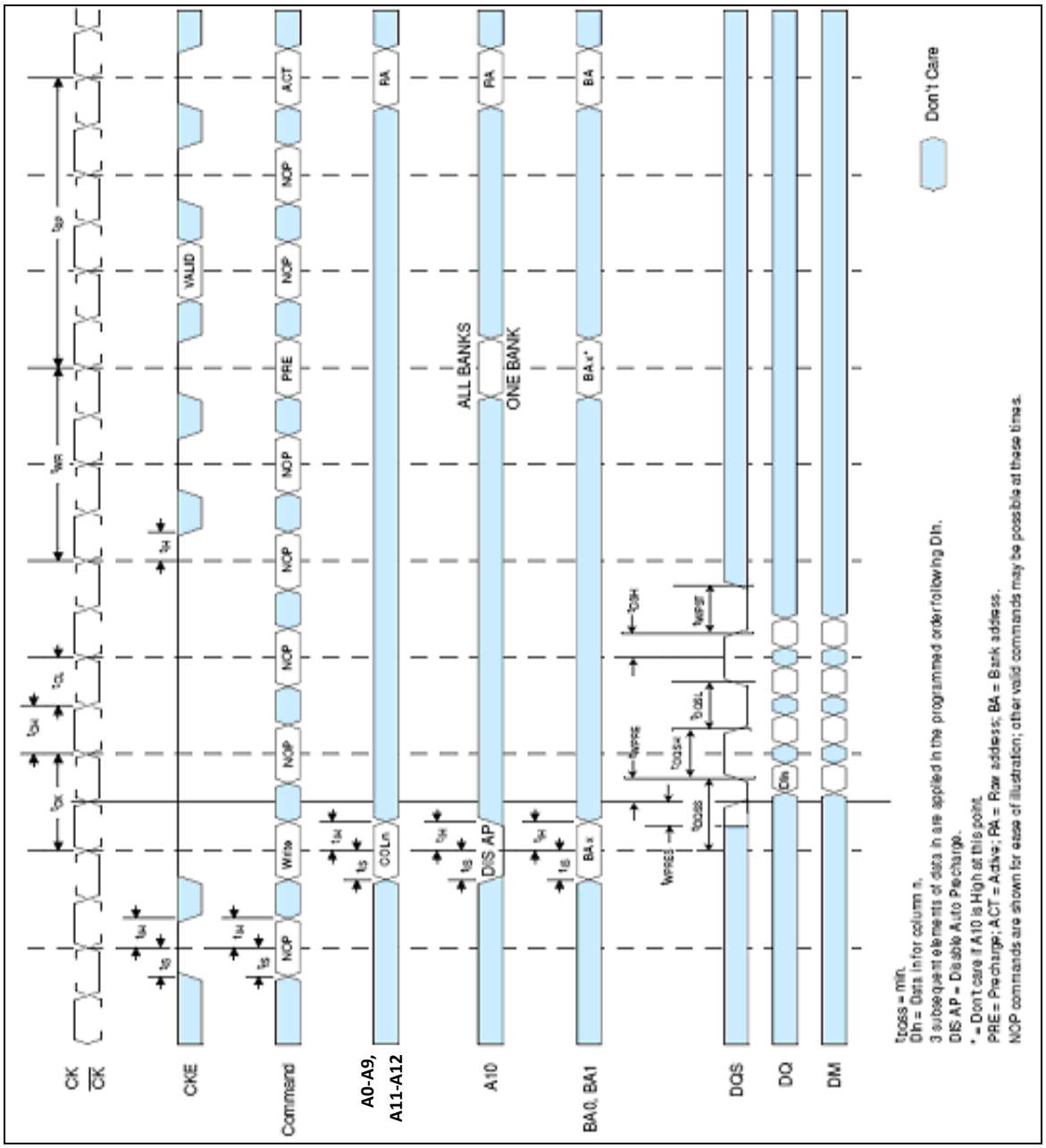
Read with Auto Precharge (Burst Length = 4)



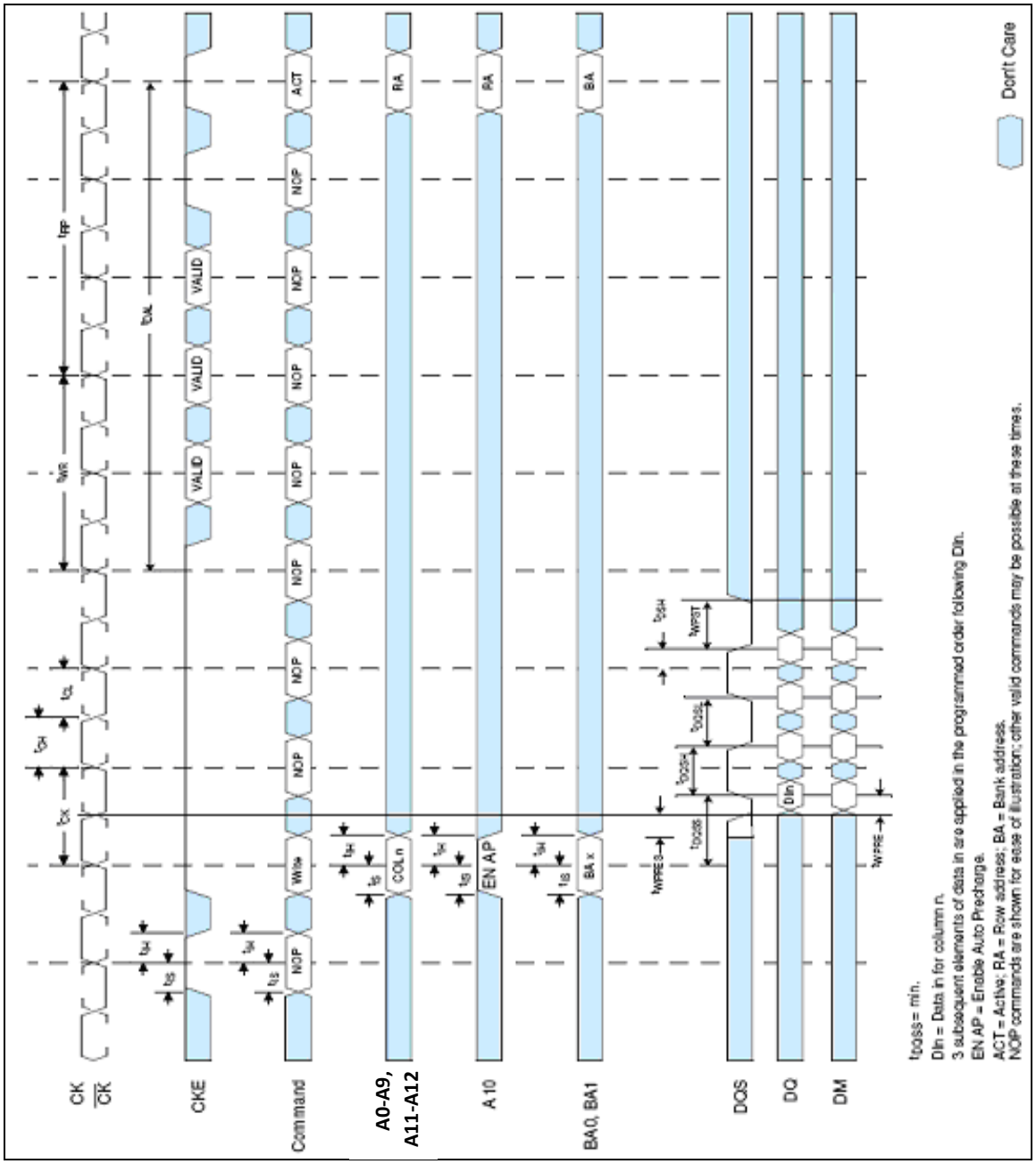
Bank Read Access (burst Length = 4)



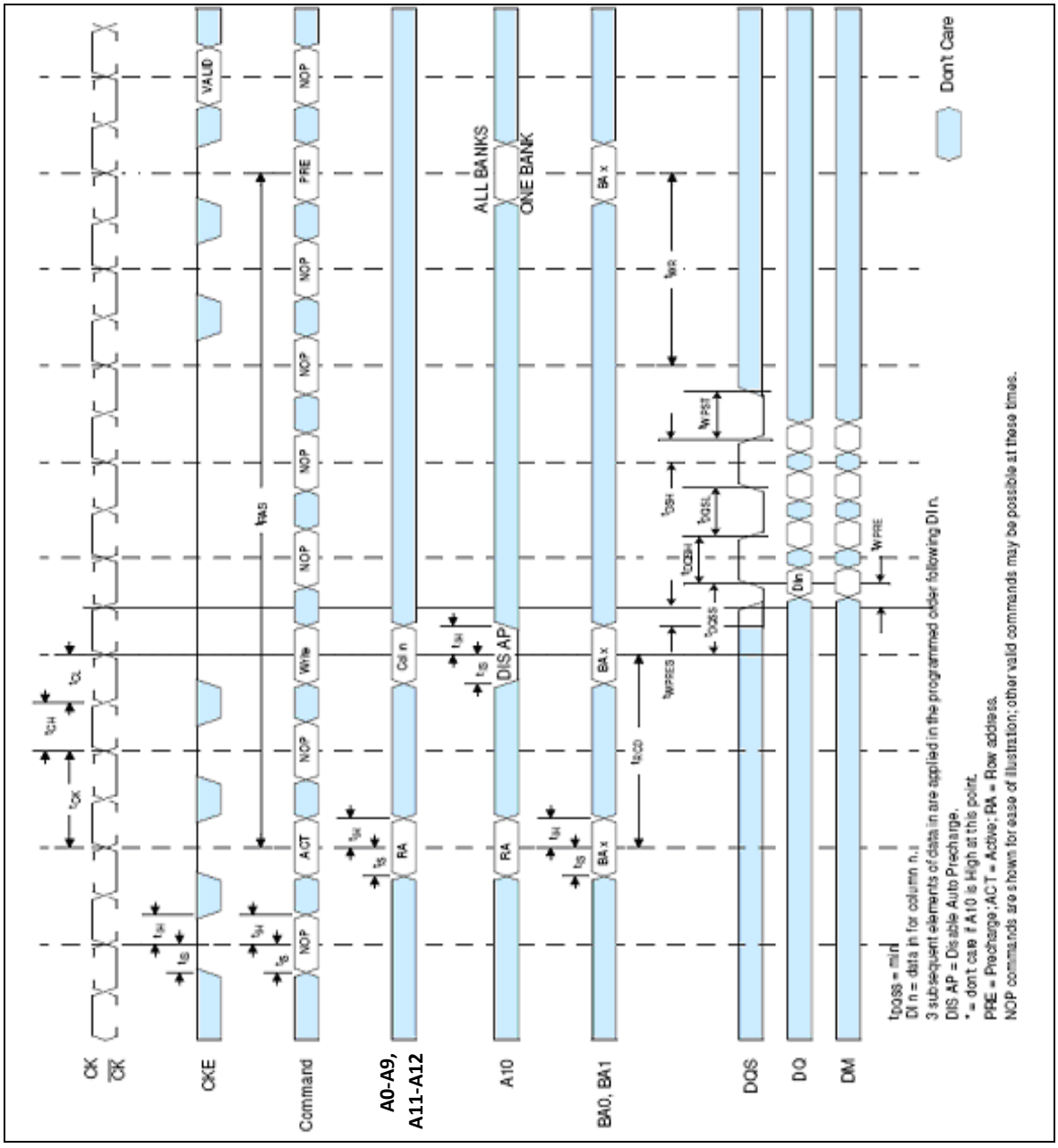
Write without Auto Precharge (Burst Length = 4)



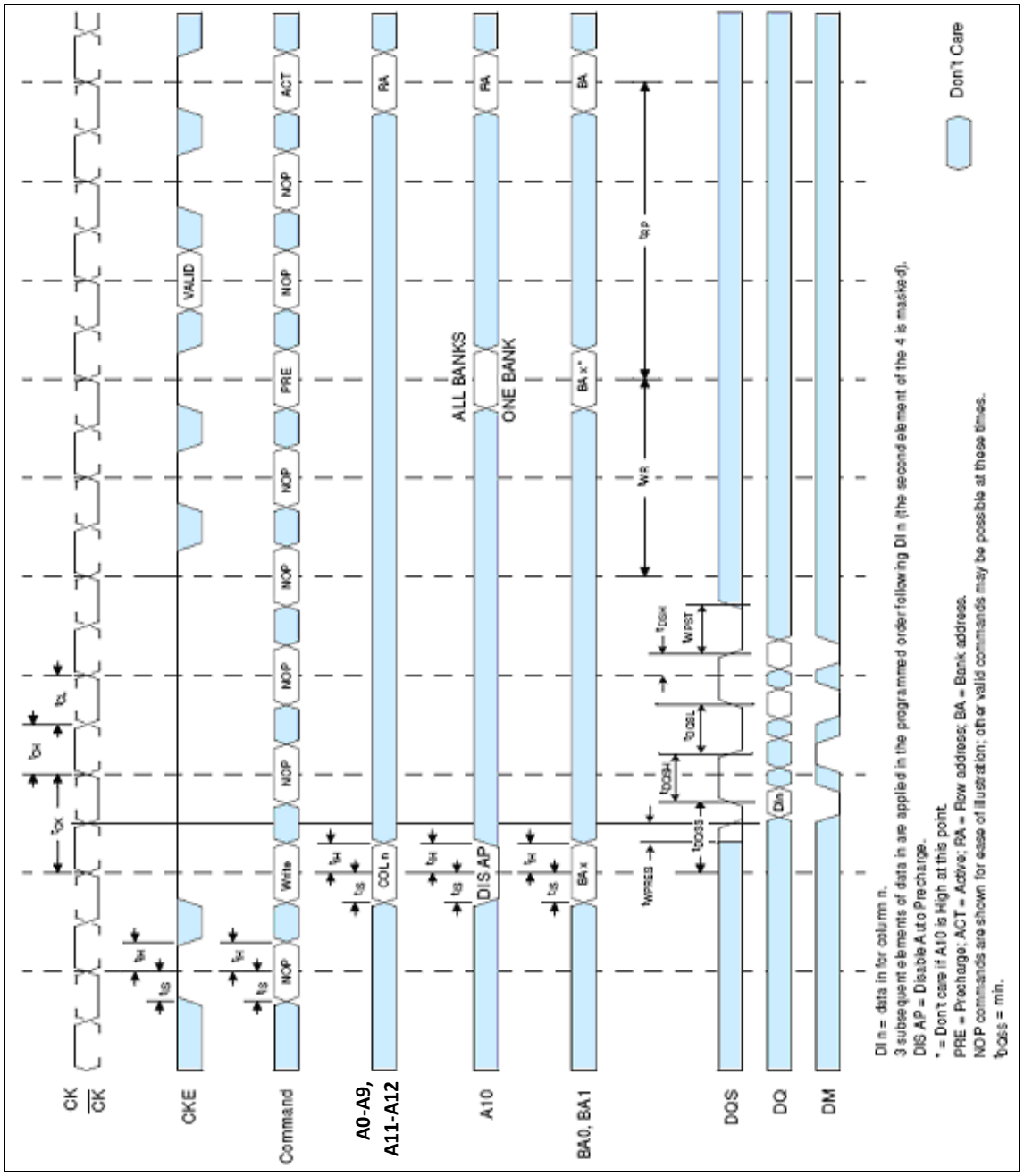
Write with Auto Precharge (Burst Length = 4)



Bank Write Access (Burst Length = 4)



Write DM Operation (Burst Length = 4)



Revision History

Version	Page	Modified	Description	Released
1.0	-	-	Preliminary Release.	03/2014
1.1	-	-	Official Release.	05/2014
1.2	P4	Part Number Guide	Simplify part number guide.	08/2014
	P65,66	-	Remove 6K/-6KI and 5T/5TI code from AC/DC timing table.	

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