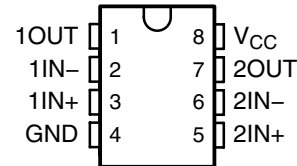


- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Low Supply-Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage:**
 - Non-V Devices . . . ± 26 V
 - V-Suffix Devices . . . ± 32 V
- **Low Input Bias and Offset Parameters:**
 - Input Offset Voltage . . . 3 mV Typ
 - Input Offset Current . . . 2 nA Typ
 - Input Bias Current . . . 20 nA Typ
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

**D OR PW PACKAGE
(TOP VIEW)**



description/ordering information

This device consists of two independent, high-gain, frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies is possible as long as the difference between the two supplies is 3 V to 26 V (3 V to 32 V for V-suffix devices), and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily provide the required interface electronics without additional ± 5 -V supplies.

The LM2904Q is manufactured to demanding automotive requirements.

ORDERING INFORMATION[†]

T _A	V _{IOmax} AT 25°C	MAX V _{CC}	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	7 mV	26 V	SOIC (D)	Tape and reel	LM2904QDRQ1	2904Q1
	7 mV	26 V	TSSOP (PW)	Tape and reel	LM2904QPWRQ1	2904Q1
	7 mV	32 V	SOIC (D)	Tape and reel	LM2904VQDRQ1	2904VQ1
	7 mV	32 V	TSSOP (PW)	Tape and reel	LM2904VQPWRQ1	2904VQ1
	2 mV	32 V	SOIC (D)	Tape and reel	LM2904AVQDRQ1	2904AVQ
	2 mV	32 V	TSSOP (PW)	Tape and reel	LM2904AVQPWRQ1	2904AVQ

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

[‡] Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

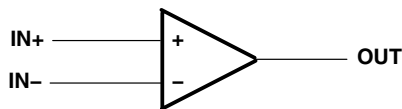


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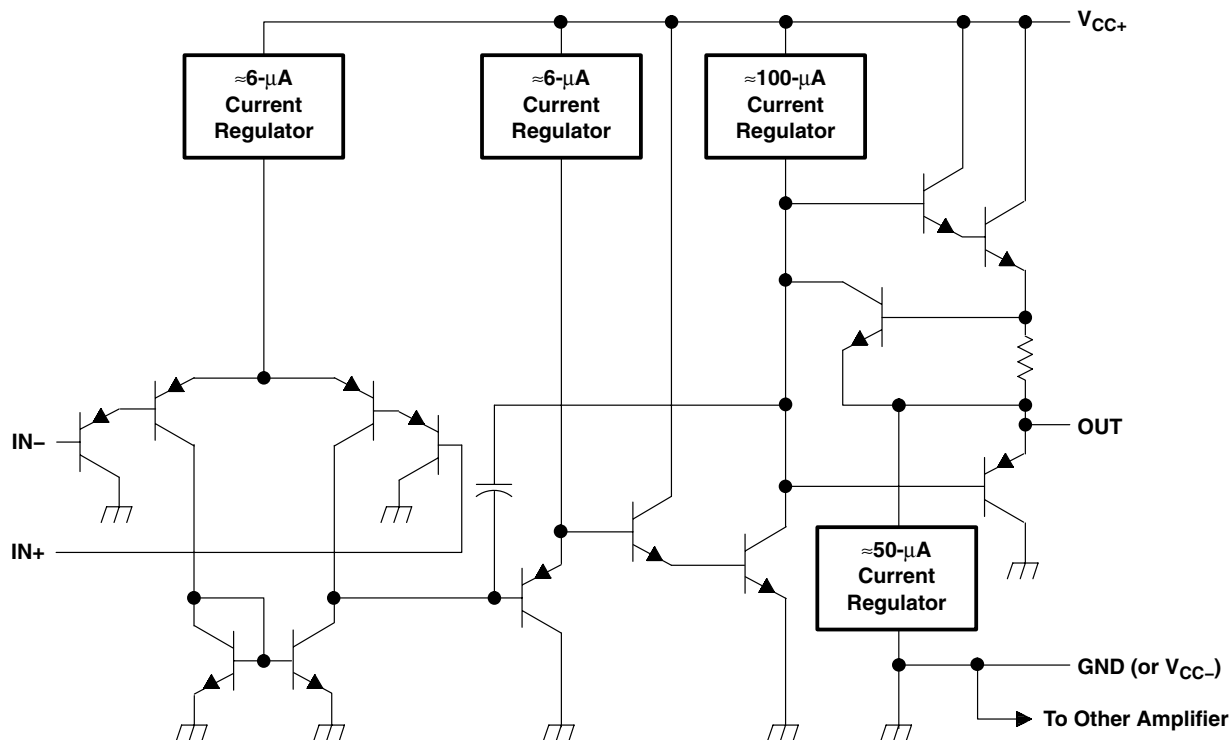
LM2904-Q1 DUAL OPERATIONAL AMPLIFIER

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symbol (each amplifier)



schematic (each amplifier)



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	7
Transistors	51
Capacitors	2

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1): Non-V devices	26 V
V-suffix devices	32 V
Differential input voltage, V_{ID} (see Note 2): Non-V devices	± 26 V
V-suffix devices	± 32 V
Input voltage range, V_I (either input): Non-V devices	–0.3 V to 26 V
V-suffix devices	–0.3 V to 32 V
Duration of output short circuit (one amplifier) to ground at (or below) 25°C	
free-air temperature ($V_{CC} \leq 15$ V) (see Note 3)	Unlimited
Operating virtual junction temperature, T_J	150°C
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package	97°C/W
PW package	149°C/W
Operating free-air temperature range, T_A	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages and V_{CC} specified for measurement of I_{OS} , are with respect to the network ground terminal.
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
 4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

LM2904-Q1

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electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A ‡	MIN	TYP§	MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC} = 5\text{ V to MAX,}$ $V_{IC} = V_{ICR(min)},$ $V_O = 1.4\text{ V}$	Non-A devices	25°C	3	7	mV	
				Full range		10		
			A-suffix devices	25°C	1	2		
				Full range		4		
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage		Full range		7		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current	$V_O = 1.4\text{ V}$	Non-V devices	25°C	2	50	nA	
				Full range		300		
			V-suffix devices	25°C	5	50		
				Full range		150		
$\alpha_{I_{IO}}$	Average temperature coefficient of input offset current		Full range		10		$\text{pA}/^\circ\text{C}$	
I_{IB}	Input bias current	$V_O = 1.4\text{ V}$		25°C	-20	-250	nA	
				Full range		-500		
I_B	Drift			Full range		50	$\text{pA}/^\circ\text{C}$	
V_{ICR}	Common-mode input voltage range	$V_{CC} = 5\text{ V to MAX}$		25°C	0 to $V_{CC}-1.5$		V	
				Full range		0 to $V_{CC}-2$		
V_{OH}	High-level output voltage	$R_L \geq 10\text{ k}\Omega$	Non-V devices	25°C	$V_{CC}-1.5$		V	
				Full range		22		
			V-suffix devices	$R_L = 2\text{ k}\Omega$		23		24
				$R_L \geq 10\text{ k}\Omega$		26		
Full range	$R_L = 2\text{ k}\Omega$		27	28				
	$R_L \geq 10\text{ k}\Omega$							
V_{OL}	Low-level output voltage	$R_L \leq 10\text{ k}\Omega$		Full range		5	20	mV
A_{VD}	Large-signal differential voltage amplification	$V_{CC} = 15\text{ V, } V_O = 1\text{ V to } 11\text{ V,}$ $R_L \geq 2\text{ k}\Omega$		25°C	25	100	V/mV	
				Full range		15		
CMRR	Common-mode rejection ratio	$V_{CC} = 5\text{ V to MAX,}$ $V_{IC} = V_{ICR(min)}$		25°C	65	80	dB	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{CC} = 5\text{ V to MAX}$		25°C	65	100	dB	
V_{O1}/V_{O2}	Crosstalk attenuation	$f = 1\text{ kHz to } 20\text{ kHz}$		25°C		120	dB	
I_O	Output current			25°C	-20	-30	mA	
				Full range		-10		
				25°C	10	20		
				Full range		5		
		$V_{ID} = -1\text{ V, } V_O = 200\text{ mV}$		25°C	12	40	μA	
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at -5 V, $V_O = 0$		25°C		± 40	± 60	mA
I_{CC}	Supply current (two amplifiers)	$V_O = 2.5\text{ V,}$ $V_{CC} = \text{MAX, } V_O = 0.5 V_{CC},$ No load		Full range		0.7	1.2	mA
							1	

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V_{CC} for testing purposes is 26 V for non-V devices and 32 V for V-suffix devices.

‡ Full range is -40°C to 125°C for LM2904Q.S

§ All typical values are at $T_A = 25^\circ\text{C}$.



operating conditions, $V_{CC} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 30\text{ pF}$, $V_I = \pm 10\text{ V}$ (see Figure 1)	0.3	$\text{V}/\mu\text{s}$
B_1	Unity-gain bandwidth	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$ (see Figure 1)	0.7	MHz
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, $V_I = 0\text{ V}$, $f = 1\text{ kHz}$ (see Figure 2)	40	$\text{nV}/\sqrt{\text{Hz}}$

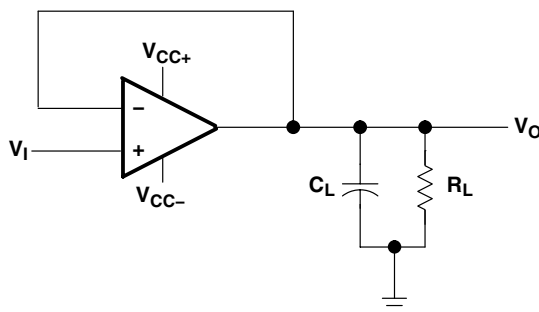


Figure 1. Unity-Gain Amplifier

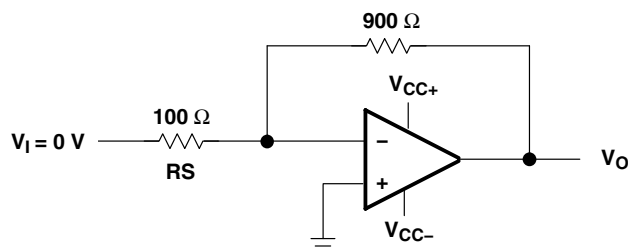


Figure 2. Noise-Test Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LM2904AVQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904AVQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904AVQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904AVQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904VQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904VQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904VQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM2904VQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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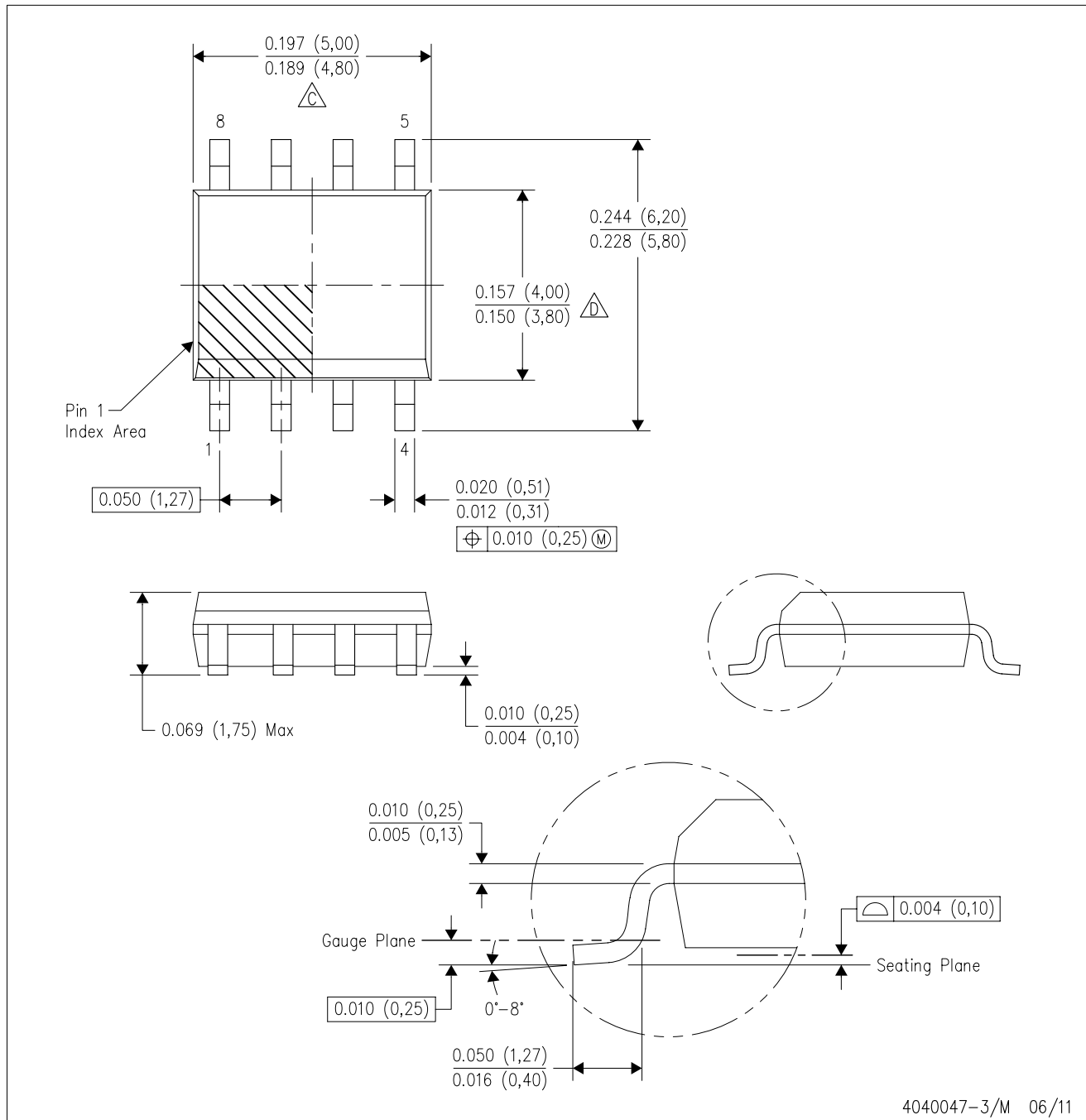
- Catalog: [LM2904](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

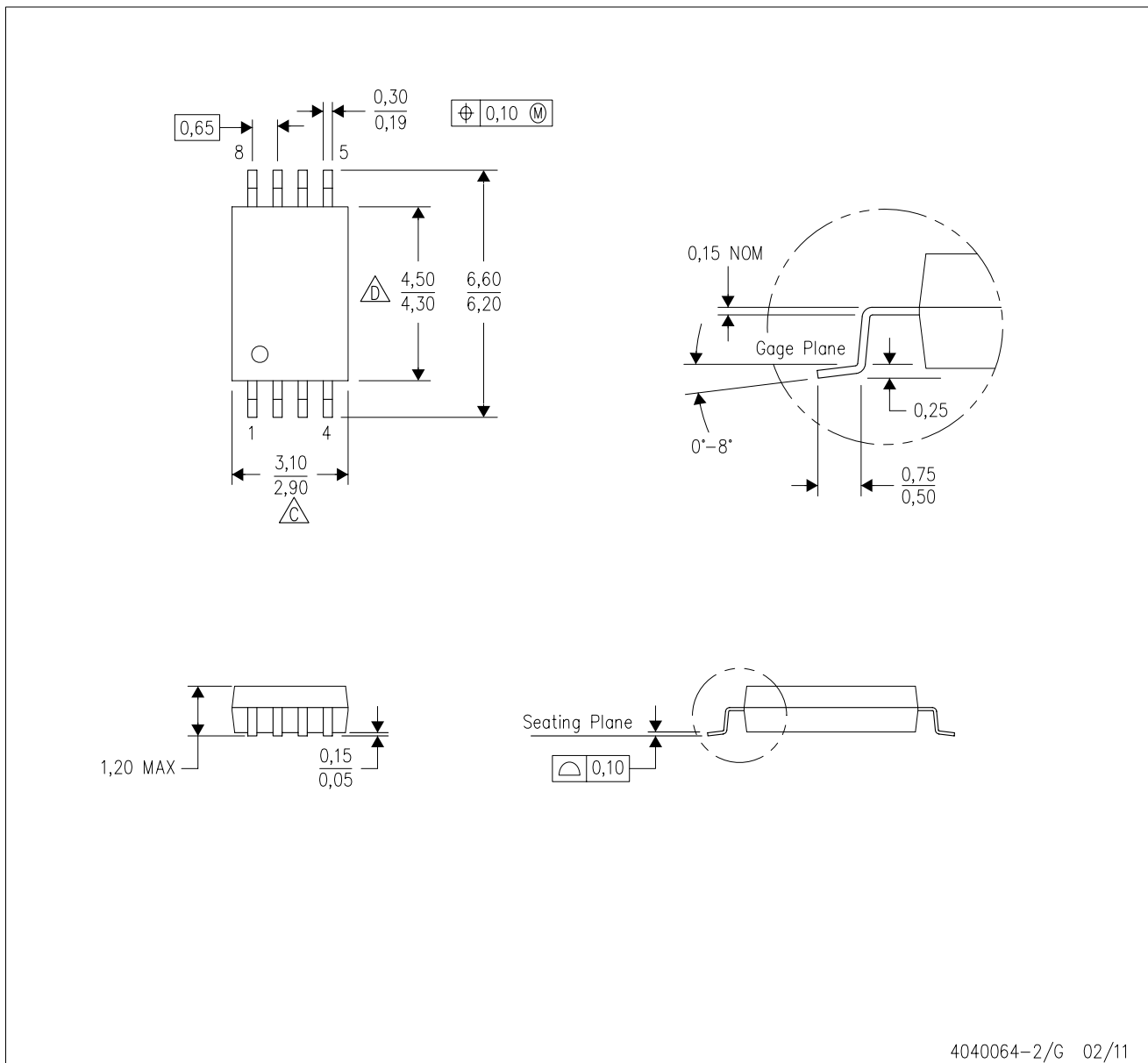
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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