EM78P176N

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

April 2010

Trademark Acknowledgments:
IBM is a registered trademark and PS/2 is a trademark of IBM.
Windows is a trademark of Microsoft Corporation.

ELAN and ELAN logo are trademarks of ELAN Microelectronics Corporation.

The contents of this specification are subject to change without further notice. ELAN Microelectronics assumes no responsibility concerning the accuracy, adequacy, or completeness of this specification. ELAN Microelectronics makes no commitment to update, or to keep current the information and material contained in this specification. Such information and material may change to conform to each confirmed order.

In no event shall ELAN Microelectronics be made responsible for any claims attributed to errors, omissions, or other inaccuracies in the information or material contained in this specification. ELAN Microelectronics shall not be liable for direct, indirect, special incidental, or consequential damages arising from the use of such information or material.

The software (if any) described in this specification is furnished under a license or nondisclosure agreement, and may be used or copied only in accordance with the terms of such agreement.

ELAN Microelectronics products are not intended for use in life support appliances, devices, or systems. Use of ELAN Microelectronics product in such applications is not supported and is prohibited.
NO PART OF THIS SPECIFICATION MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE EXPRESSED WRITTEN PERMISSION OF ELAN MICROELECTRONICS.

ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre
95 How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:
Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
3F, SSMEC Bldg., Gaoxin S. Ave. I
Shenzhen Hi-tech Industrial Park
(South Area), Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:
Elan Microelectronics Shanghai, Ltd.
#34, First Fl., 2nd Bldg.,
Lane 122, Chunxiao Rd.
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax :+86 21 5080-4600
elan-sh@elanic.com.cn

Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2010/03/24
1.0	Initial version	2010/04/21

1 General Description

The EM78P176N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has an on-chip 1K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). They provide a protection bit to prevent intrusion of user's OTP memory code. Three Code option words are also available to meet user's requirements.

With its enhanced OTP-ROM features, the EM78P176N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program your development code.

2 Features

- CPU configuration
  - 1K×13 bits on chip ROM
  - 48×8 bits on-chip registers (SRAM, General purpose)
  - 5-level stacks for subroutine nesting
  - 4 programmable level voltage detector
    LVD : 4.5, 4.0, 3.3, 2.2V
  - 3 programmable level voltage reset
    LVR : 4.0, 3.5, 2.7V
  - Less than 1.5mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 1 μA, during Sleep mode
- I/O port configuration
  - 3 bidirectional I/O ports : P5, P6, P7
  - 18 I/O pins
  - Wake-up port : P6
  - 7 Programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 8 programmable open-drain I/O pins
  - External interrupt with wake-up : P60
- Operating voltage range:
  - 2.1V~5.5V at 0~70°C (Commercial)
  - 2.3V~5.5V at -40~85°C (Industrial)
- Operating frequency range (base on 2 clocks):
  - Crystal mode:
    DC~20MHz/2clks @ 5V
    DC~8MHz/2clks @ 3V
    DC~4MHz/2clks @ 2.1V
  - ERC mode:
    DC~2 MHz/2clks @ 2.1V
  - IRC mode:

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.1V~5.5V)	Process	Total
4MHz	±2%	±3%	±2%	±7%
16MHz	±2%	±3%	±2%	±7%
8MHz	±2%	±3%	±2%	±7%
1MHz	±2%	±3%	±2%	±7%

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - External interrupt input pin
  - 2/4 clocks per instruction cycle selected by code option
  - Power down (Sleep) mode
  - High EFT Immunity
- Four available interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt
  - External interrupt
  - Low voltage detect interrupt
- Special features
  - Programmable free running watchdog timer
  - Power-on voltage detector available (1.8~1.9V)
  - Selectable Oscillation mode
- Package type:
  - 20-pin SSOP 209mil : EM78P176NSS20J/S
  - 20-pin SOP 300mil : EM78P176NSO20J/S
  - 18-pin DIP 300mil : EM78P176ND18J/S
  - 18-pin SOP 300mil: EM78P176NSO18J/S
  - 10-pin SSOP 150mil : EM78P176NSS10J/S
  - 10-pin MSOP 118mil: EM78P176NMS10J/S

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

(1) 20-Pin SSOP/SOP

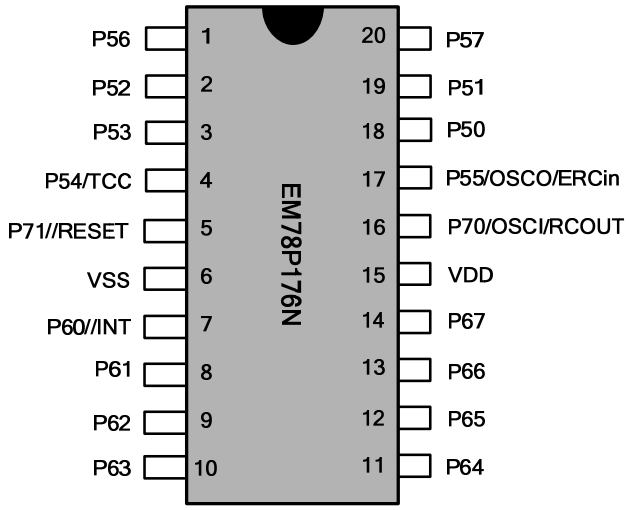


Figure 3-1 20-pin EM78P176N

(2) 18-Pin DIP/SOP

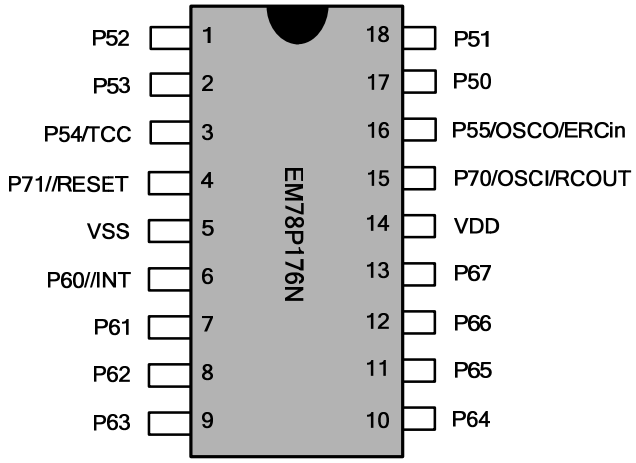


Figure 3-2 18-pin EM78P176N

(3) 10-Pin SSOP/MSOP

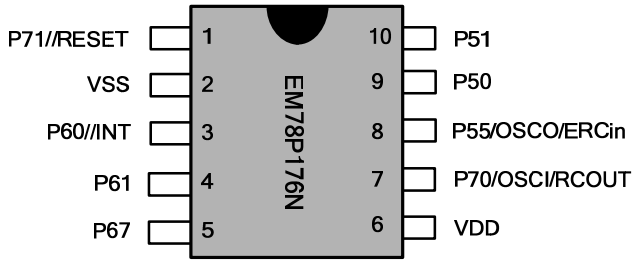


Figure 3-3 10-pin EM78P176N

4 Pin Description

4.1 EM78P176N-20PIN

Name	Function	Input Type	Output Type	Description
P50~P52	P50~P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down.
P53	P53	ST	CMOS	Bidirectional I/O pin
P54/TCC	P54	ST	CMOS	Bidirectional I/O pin
	TCC	ST	–	Real Time Clock/Counter clock input
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin.
	OSCO	–	XTAL	Clock output of crystal/resonator oscillator
	ERCin	AN	–	External RC input pin
P56~P57	P56~P57	ST	CMOS	Bidirectional I/O pin
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
	/INT	ST	–	External interrupt pin
P61~P63	P61~P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
P64~P67	P64~P67	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wake-up.
P70/OSCI/RCOUT	P70	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P71//RESET	P71	ST	CMOS	Bidirectional I/O pin
	/RESET	ST	–	Internal pull-high reset pin
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

Legend: ST: Schmitt Trigger input, AN: analog pin, CMOS: CMOS output, XTAL: oscillation pin for crystal/ resonator

4.2 EM78P176N-18PIN

Name	Function	Input Type	Output Type	Description
P50~P52	P50~P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down.
P53	P53	ST	CMOS	Bidirectional I/O pin
P54/TCC	P54	ST	CMOS	Bidirectional I/O pin
	TCC	ST	–	Real Time Clock/Counter clock input
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO	–	XTAL	Clock output of crystal/resonator oscillator
	ERCin	AN	–	External RC input pin
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
	/INT	ST	–	External interrupt pin
P61~P63	P61~P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
P64~P67	P64~P67	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wake-up.
P70/OSCI/RCOUT	P70	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P71//RESET	P71	ST	CMOS	Bidirectional I/O pin
	/RESET	ST	–	Internal pull-high reset pin
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

Legend: ST: Schmitt Trigger input, AN: analog pin, CMOS: CMOS output,
XTAL: oscillation pin for crystal/ resonator

4.3 EM78P176N-10PIN

Name	Function	Input Type	Output Type	Description
P50~P51	P50~P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down.
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO	–	XTAL	Clock output of crystal/resonator oscillator
	ERCin	AN	–	External RC input pin
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
	/INT	ST	–	External interrupt pin
P61	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
P67	P67	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wake-up.
P70/OSCI/RCOUT	P70	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P71//RESET	P71	ST	CMOS	Bidirectional I/O pin
	/RESET	ST	–	Internal pull-high reset pin
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

Legend: ST: Schmitt Trigger input, AN: analog pin, CMOS: CMOS output,
XTAL: oscillation pin for crystal/ resonator

5 Block Diagram

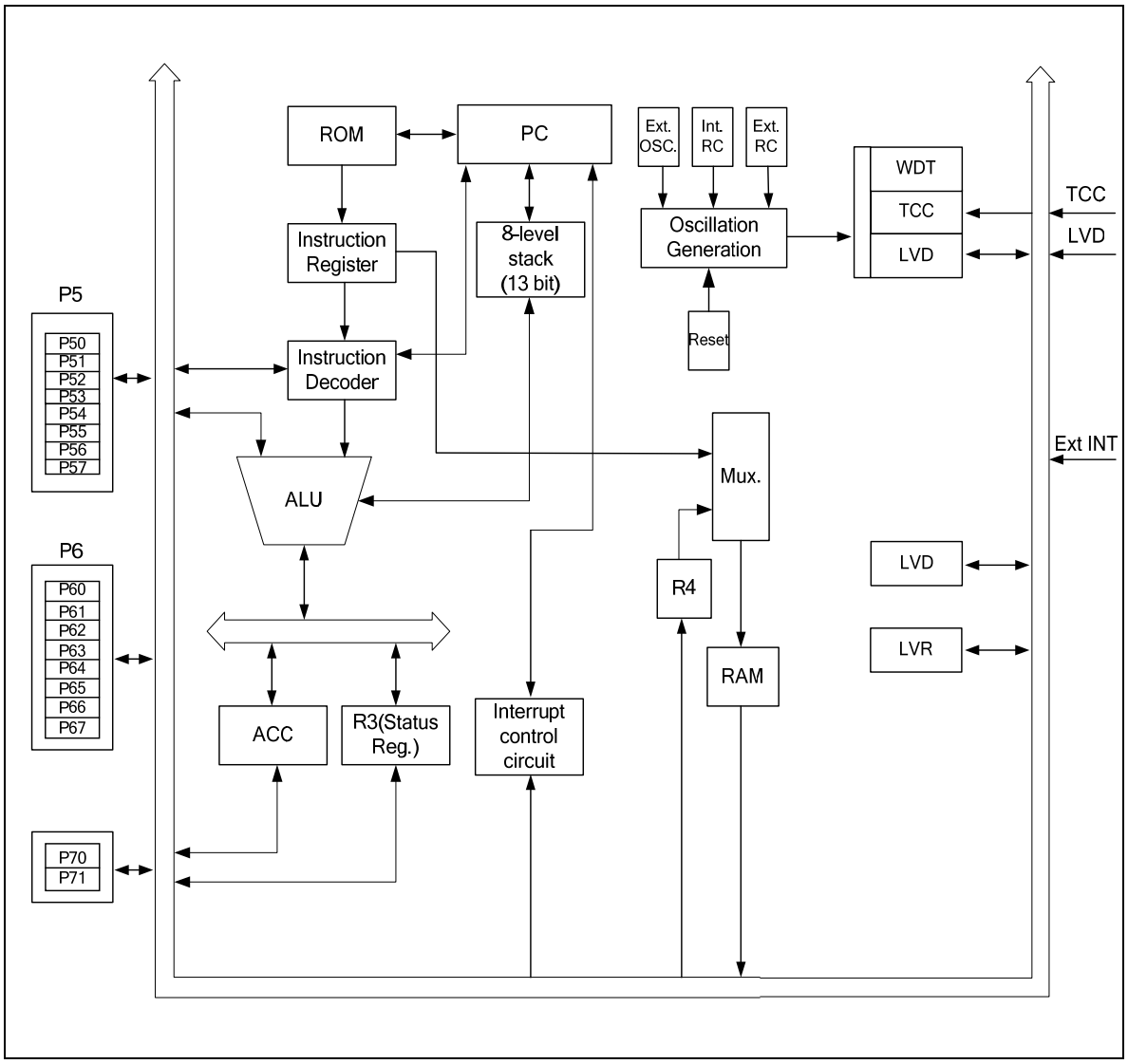


Figure 5-1 EM78P176N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

- Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

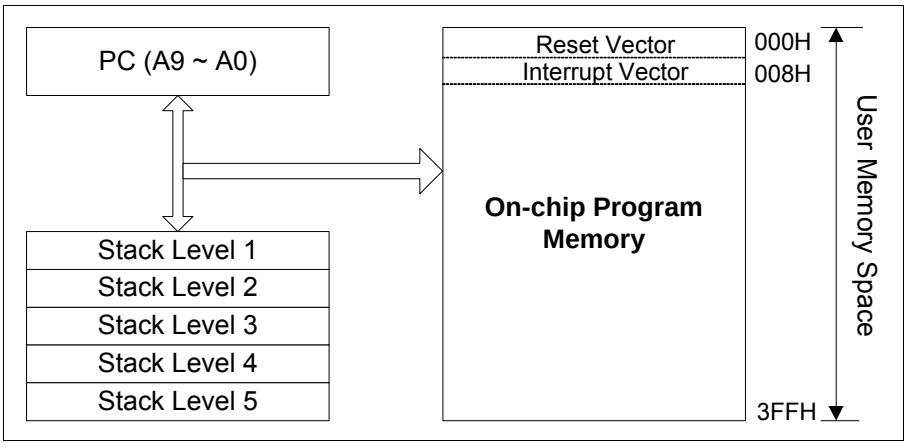


Figure 6-1 Program Counter Organization

- When ICE300N tries to simulate the stack of EM78P176N, and when the simulated stacks exceed 5 levels, the simulated result will be inconsistent with the EM78P176N.
- The configuration structure generates 1024×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0" when under RESET condition.

- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETLk", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.

Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6" etc.) will cause the ninth bit and above bits of the PC to remain unchanged.

- All instructions are single instruction cycle (fclk/2 or fclk/4) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.

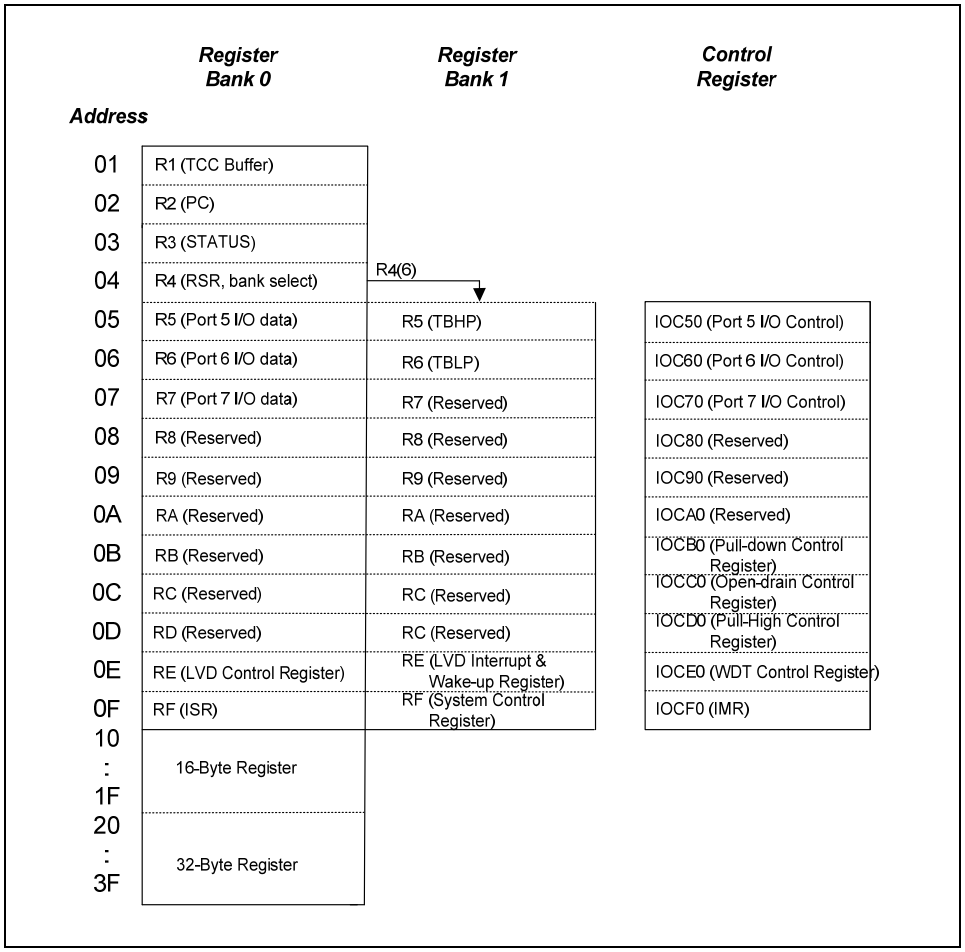


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GP1	GP0	T	P	Z	DC	C

Bit 7 (RST): Bit for reset type

0 : Set to 0 if the device wakes up from other reset type.

1 : Set to 1 if the device wakes up from sleep mode on a pin change, external interrupt or low voltage detector interrupt.

Bits 6 ~ 5 (GP1 ~ GP0): General-purpose read/write bits

Bit 4 (T): Time-out bit

Set to “1” with the "SLEP" and "WDTC" commands, or during power up; and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit

Set to “1” during power on or by a "WDTC" command; and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7: General-purpose read/write bits.

Bit 6: Used to select Banks 0~1.

See the Data Memory Configuration in Figure 6-3.

6.1.6 R5 ~ R7 (Port 5 ~ Port 7)

R5, **R6 and P70 ~ P71** are I/O registers.

P72 ~ P77 are fixed to 0.

6.1.7 Bank 0 RE (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/LVD	LVDIF	-	-	-	-	-	LVDWE

Bit 7 (/LVD): Low voltage Detector state.

When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bit 6 (LVDIF): LVD Interrupt Flag bit.

0: no interrupt occurs

1: with interrupt request

Bits 5 ~ 1: Not used. Set to "0" at all time**.**

Bit 0 (LVDWE): Low Voltage Detect wake-up.

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

6.1.8 Bank 0 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

NOTE

" 1 " means with interrupt request " 0 " means no interrupt occurs

Bits 7 ~ 3: Not used. Set to "0" at all time.

Bit 2 (EXIF): External Interrupt Flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

6.1.9 Bank 1 R5 (TBHP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	-	-	RBit9	RBit8

Bit 7 (MLB): Chooses the MSB or LSB machine code to move into the register.

The machine code is pointed by TBLP and TBHP register.

Bits 6 ~ 2: Not used. Set to "0" at all time.

Bits 1 ~ 0: Most 2 significant bits of address for program code

6.1.10 Bank 1 R6 (TBLP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bits 7 ~ 0: These are the least 8 significant bits of address for program code.

6.1.11 Bank 1 RE (LVD Interrupt and Wake-up Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD1	LVD0	-	-	-	EXWE

Bit 7 (LVDIE): Low voltage detector interrupt enable bit

0: Disable the low voltage detector interrupt

1: Enable the low voltage detector interrupt

Bit 6 (LVDEN): Low voltage detector enable bit

0: Disable the Low voltage detector function

1: Enable the Low voltage detector function

Bits 5 ~ 4: Low voltage detector level bits

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	N/A	1

NOTE

IF Vdd has crossover at LVD voltage in interrupt level as VDD varies, LVD interrupt will occur.

Bits 3 ~ 1: Not used. Set to “0” at all time.

Bit 0 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin wake-up

1: Enable External /INT pin wake-up

6.1.12 Bank 1 RF (System Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	-	-	RCM1	RCM0

Bits 7, 3 ~ 2: not used, fixed to "0" all the time.

Bit 6 (TIMERSC): TCC clock source select.

0 : Fs is used as Fc

1 : Fm is used as Fm/2 or Fm/4 (default)

Bit 5 (CPUS): CPU Oscillator Source Select

0 : Fs : sub frequency for WDT internal RC time base 16kHz

1 : Fm : main oscillator (Fm) (default)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit.

From SLEP instruction, this bit will determine as to which mode to choose.

0 : IDLE = '0' + SLEP instruction → sleep mode (default)

1 : IDLE = '1' + SLEP instruction → idle mode

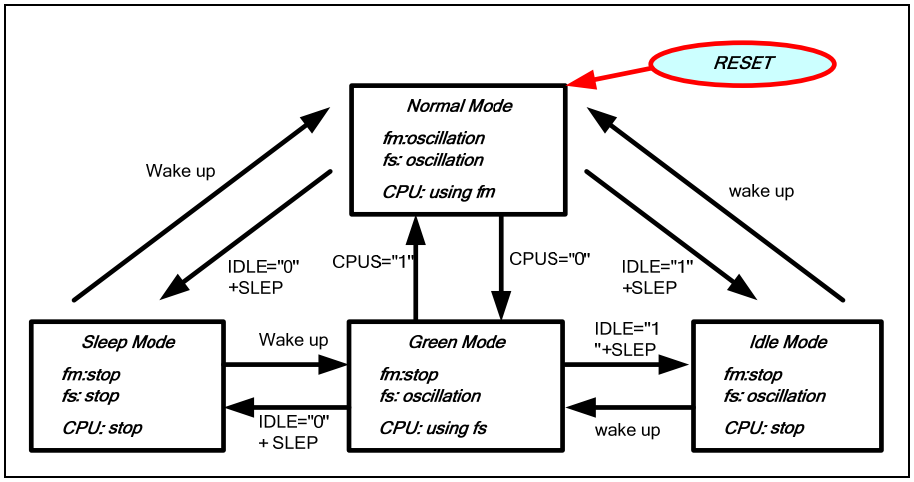


Figure 6-3 CPU Operation Mode Diagram

Oscillator (Normal Mode Source)	CPU Mode Status	Oscillator Stable Time (S)[1]	Count from Normal/Green (CLK)[2]
Crystal 1M ~ 20 MHz	Sleep/Idle → Normal	0.5 ms ~ 2 ms	510 CLK
	Green → Normal		510 CLK
	Sleep/Idle → Green	< 100 µs	8 CLK
ERC 2 MHz	Sleep/Idle → Normal	< 5 µs	8 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	
IRC 1M, 4M, 8M, 16 MHz	Sleep/Idle → Normal	< 2 µs	8 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	

NOTE

- *[1]The oscillator stable time depends on the oscillator characteristics.*
- *[2]After the oscillator has stabilized, the CPU will count 510/8 CLK in Normal/Green mode and continue to work in Normal/Green mode.*

Ex 1 : The 4 MHz IRC wakes-up from Sleep mode to Normal mode, the total wake-up time is 2 µs + 8 CLK @ 4 MHz.

Ex 2 : The 4 MHz IRC wakes-up from Sleep mode to Green mode, the total wake-up time is 100 µs + 8 CLK @ 16kHz.

Bits 1 ~ 0 (RCM1 ~ RCM0): IRC mode select bits.

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	16
0	1	8
0	0	1

Bank 1 RF<1,0> will be enabled.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**1**	**1**	**4 MHz ± 2%**	2.1V ~ 5.5V	< 5 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1MHz ± 10%	2.1V ~ 5.5V	< 24 µs
16 MHz	1	1	4 MHz ± 10%	2.1V ~ 5.5V	< 6 µs
	1	**0**	**16 MHz ± 2%**	4.5V ~ 5.5V	< 1.25 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1MHz ± 10%	2.1V ~ 5.5V	< 24 µs
8 MHz	1	1	4 MHz ± 10%	2.1V ~ 5.5V	< 6 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	**1**	**8 MHz ± 2%**	3.0V ~ 5.5V	< 2.5 µs
	0	0	1MHz ± 10%	2.1V ~ 5.5V	< 24 µs
1 MHz	1	1	4 MHz ± 10%	2.1V ~ 5.5V	< 6 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	**0**	**1MHz ± 2%**	2.1V ~ 5.5V	< 20 µs

NOTE

- *The initial values of Bank1 RF<1,0> will be kept the same as Word 1<6,5>.*
- *If user changes the IRC frequency from A-frequency to B-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the B-frequency.*

For Example:

1st step When user selects the 4 MHz at the Writer, the initial values of Bank 1 RF<1,0> would be "11", the same as the value of Word 1<6,5> which is "11".

If the MCU is free-running, it will work at 4 MHz ± 2%. Refer to the table below.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**1**	**1**	**4 MHz ± 2%**	2.1V ~ 5.5V	< 5 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1MHz ± 10%	2.1V ~ 5.5V	< 24 µs

2nd step If it is desired to set Bank 1 RF<1,0> = "10" while the MCU is working at 4 MHz ± 2%, the MCU needs to hold for 1.5 µs, then it will continue to work at 16 MHz ± 10%.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	1	1	4 MHz ± 2%	2.1V ~ 5.5V	< 5 µs
	1	**0**	**16 MHz ± 10%**	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1MHz ± 10%	2.1V ~ 5.5V	< 24 µs

3rd step If it is desired to set Bank 1 RF<1,0> = "00" while the MCU is working at 16 MHz ± 10%, the MCU needs to hold for 24 µs, then it will continue to work at 1 MHz ± 10%.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	1	1	4 MHz ± 2%	2.1V ~ 5.5V	< 5 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	**0**	**1MHz ± 10%**	2.1V ~ 5.5V	< 24 µs

4th step If it is desired to set Bank 1 RF<1,0> = "11" while the MCU is working at 1 MHz ± 10%, the MCU needs to hold for 5 µs, then it will continue to work at 4 MHz ± 2%.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**1**	**1**	**4 MHz ± 2%**	2.1V ~ 5.5V	< 5 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1MHz ± 10%	2.1V ~ 5.5V	< 24 µs

6.1.13 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 7 (GP): General purpose register.

Bit 6 (INT): Interrupt enable flag

0 : masked by DISI or hardware interrupt

1 : enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0 : internal instruction cycle clock, P54 is a bidirectional I/O pin

1 : transition on TCC pin

Bit 4 (TE): TCC Signal Edge

0 : increment if the transition from low to high takes place on TCC pin

1 : increment if the transition from high to low takes place on TCC pin

Bit 3 (PAB): Prescaler Assigned Bit

0 : TCC

1 : WDT

Bit 2 ~ Bit 0 (PSR2 ~ PSR0): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

The CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC7 (I/O Port Control Register)

0 : defines the relative I/O pin as output

1 : puts the relative I/O pin into high impedance

IOC5 and IOC6 and P70~P71 registers are both readable and writable.

6.2.4 IOCB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD63	/PD62	/PD61	/PD60	-	/PD52	/PD51	/PD50

Bit 7 (/PD63): Control bit used to enable pull-down of the P63 pin.

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bit 3: Not used. Set to "1" at all time.

Bit 2 (/PD52): Control bit used to enable pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

The IOCB Register is both readable and writable.

6.2.5 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bit 7 (OD67): Control bit used to enable open-drain of the P67 pin.

0 : Disable open-drain output

1 : Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain of the P66 pin.

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain of the P64 pin.

Bit 3 (OD63): Control bit used to enable open-drain of the P63 pin.

Bit 2 (OD62): Control bit used to enable open-drain of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain of the P60 pin.

The IOCC Register is both readable and writable.

6.2.6 IOCD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit is used to enable pull-high of the P67 pin.

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.2.7 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	GP	GP	GP	GP	GP	GP

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

0 : Disable WDT

1 : Enable WDT

Bit 6 (EIS): Control bit is used to define the function of P60 (/INT) pin.

0 : P60, bidirectional I/O pin.

1 : /INT, external interrupt pin.

When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 6 (R6).
See Figure 6-6 under Section 6.4 for reference.

EIS is both readable and writable.

WDTE is both readable and writable.

Bits 5 ~ 0: General purpose register.

6.2.8 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Bits 7 ~ 3: Not used. Set to "1" at all time.

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-10.

Bit 2 (EXIE): EXIF interrupt enable bit

0 : disable EXIF interrupt

1 : enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 : disable ICIF interrupt

1 : enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0 : disable TCIF interrupt

1 : enable TCIF interrupt

The IOCF register is both readable and writable.

6.3 TCC/WDT and Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or the WDT only at the same time and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the "WDTC" or "SLEP" instructions. Figure 6-4 depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal or external clock input (edge selectable from TCC pin). If the TCC signal source is from an internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). Referring to Figure 6-4, CLK=Fm/2 or CLK=Fm/4, depends on the Code Option bit CLK. CLK=Fm/2 is used if CLK bit is "0", and CLK=Fm/4 is used if CLK bit is "1". If the TCC signal source is from an external clock input, TCC is incremented by 1 at every falling edge or rising edge of the TCC pin.

- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of the IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

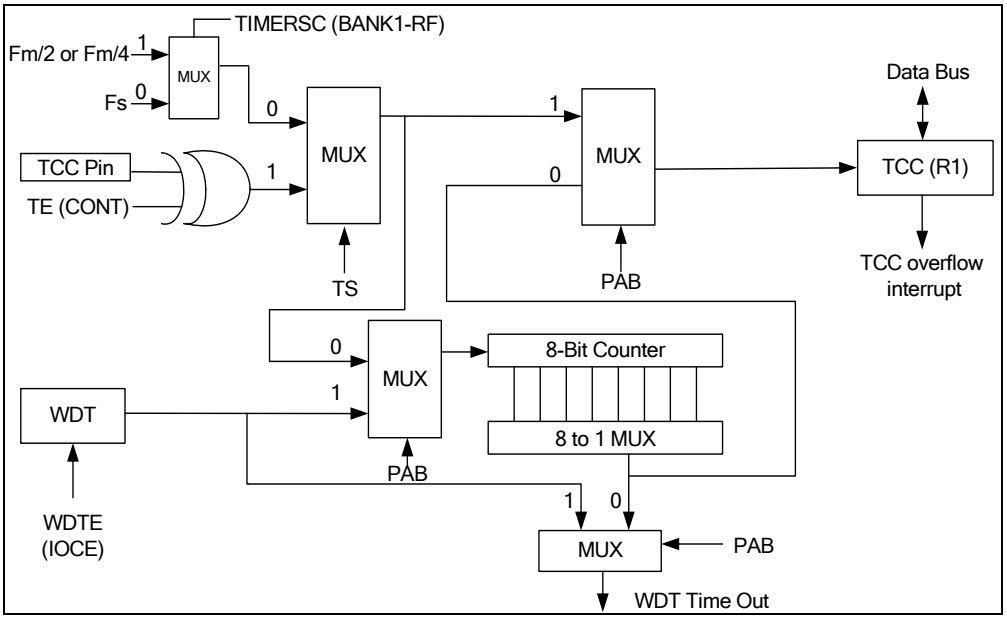
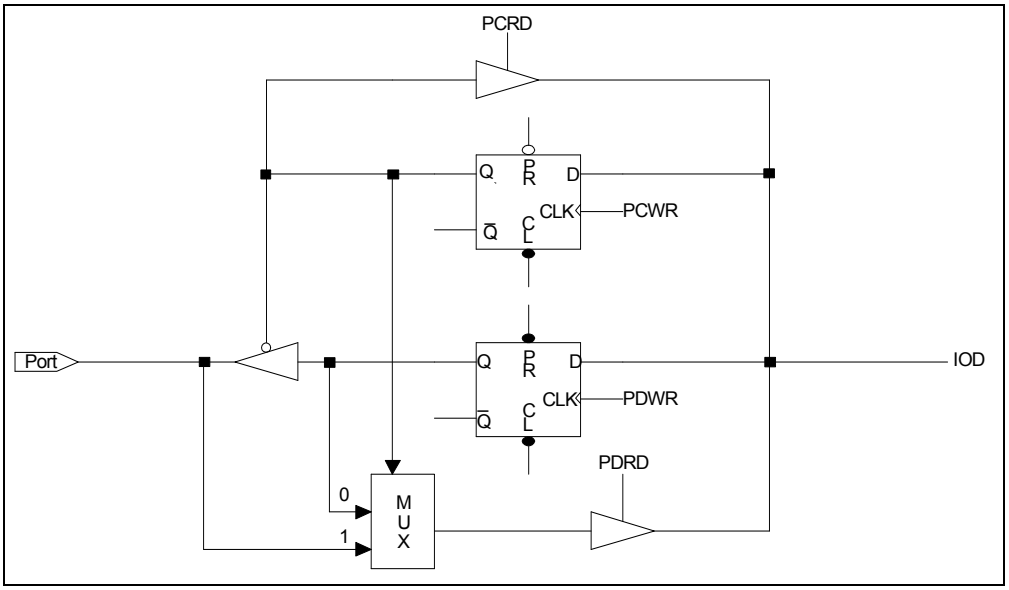


Figure 6-4 TCC and WDT Block Diagram

6.4 I/O Ports

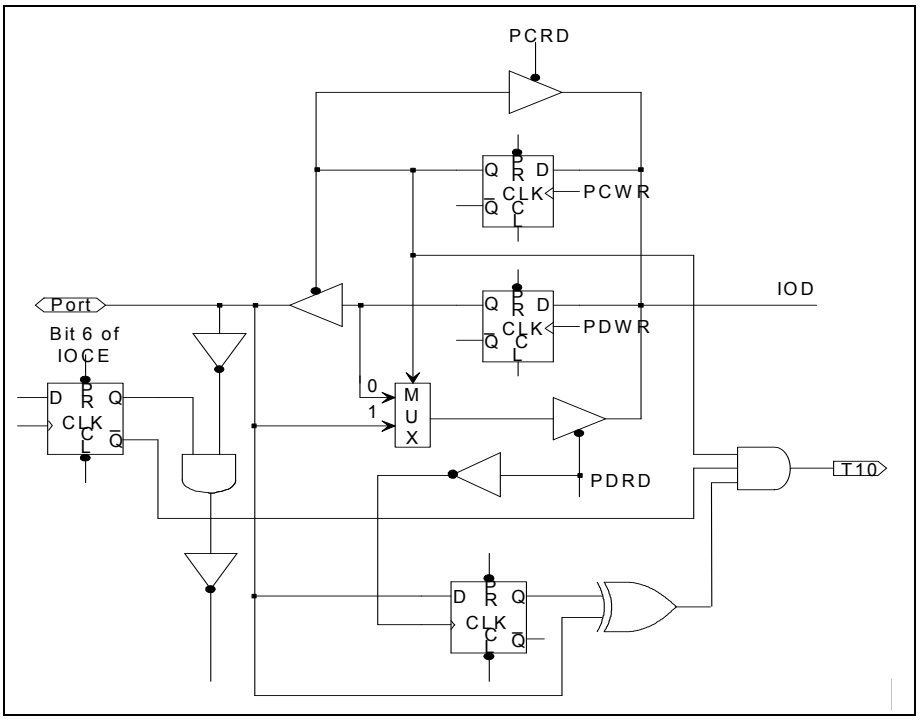
The I/O registers, Port 5, Port 6 and Port 70~71, are bidirectional tri-state I/O ports. Port 6 can be pulled-high internally by software. In addition, Port 6 can also have open-drain output by software. Input status changed interrupt (or wake-up) function is available from Port 6. P50 ~ P52 and P60 ~ P63 pins can be pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC7). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6 and Port 7 are shown in Figure 6-5, Figure 6-6 and Figure 6-7 respectively.

[1] Vdd = 5V, WDT time-out period = 16.8ms ± 30% at 25°C
Vdd = 3V, WDT time-out period = 18ms ± 30% at 25°C



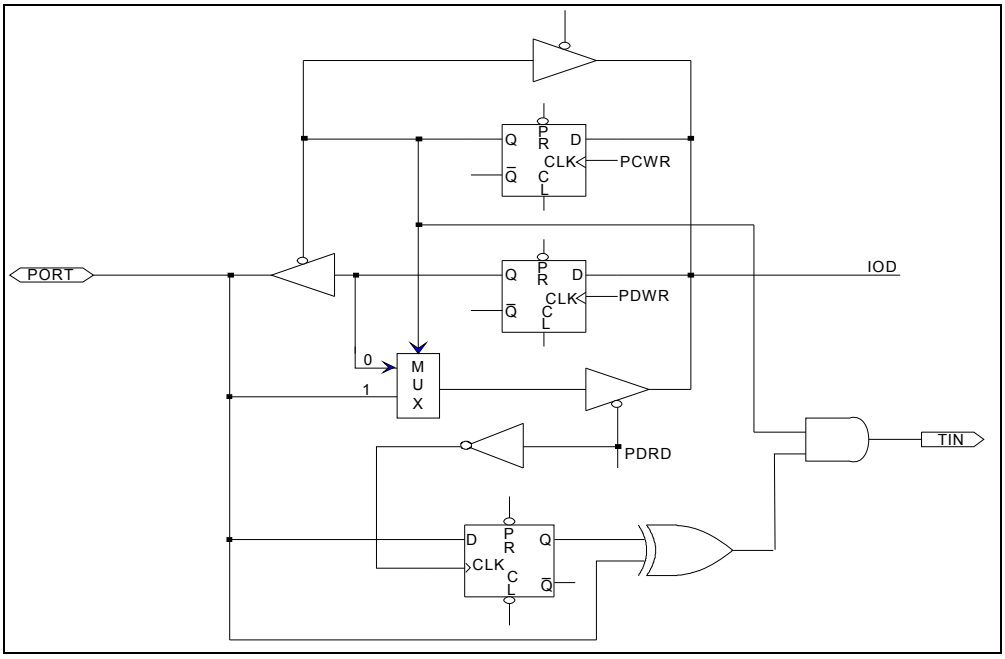
Note: Pull-down is not shown in the figure.

Figure 6-5 I/O Port and I/O Control Register Circuit for Port 5, 6 and Port 70~71



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-6 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-7 I/O Port and I/O Control Register Circuit for P61~P67

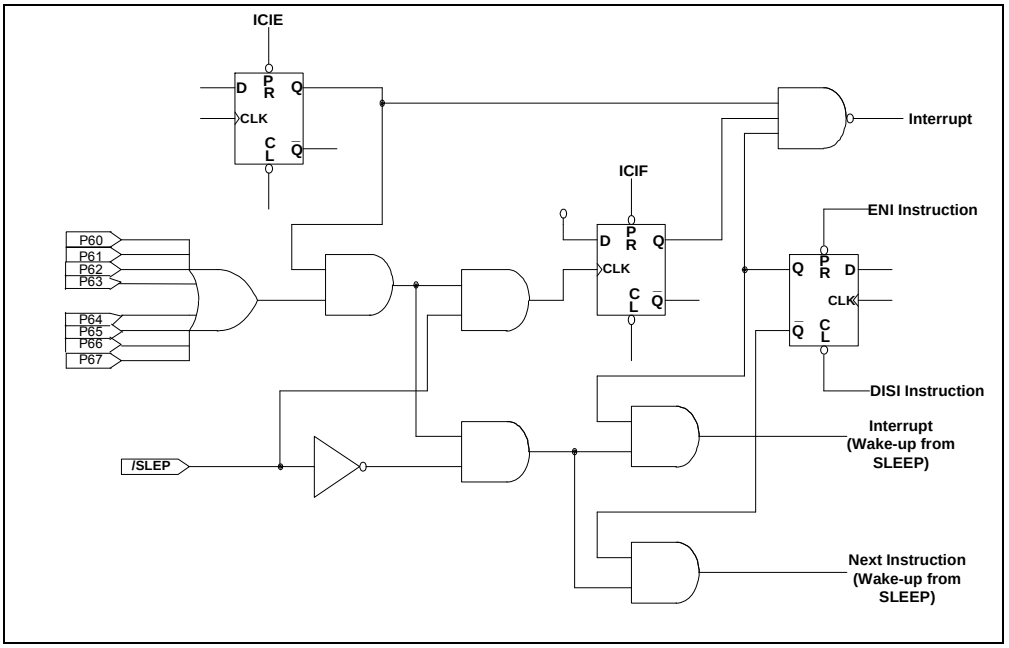


Figure 6-8 Block Diagram of I/O Port 6 with input change interrupt/wake-up

Table 6-1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt Vector (008H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute “ENI” 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt Vector (008H)

6.5 Reset and Wake-up

6.5.1 Reset

A Reset is initiated by one of the following events:

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)
4) Low Voltage Reset

The device is kept under reset condition for a period of approximately 18 ms or 150 µs (Events 1 and 4 are approximately 18 ms and Events 2 and 3 are approximately 150 µs) after a reset is detected.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0."
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for Bit 6 (INT flag).
- The bits of the IOCB register are set to all "1."
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1."
- Bit 7 of the IOCE register is set to "1," and Bits 4 and 6 are cleared.
- Bits 0 ~ 2 of RF and Bits 0 ~ 2 of IOCF registers are cleared.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. After a wake-up, in IRC mode (IRC 4MHz / 5V) the wake-up time 1.5 μs, XT mode (4MHz / 5V) wake-up time is 1.5 ms.

The controller can be awakened by:

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) Port 6 Input Status changed (if enabled)
4) External (P60, /INT) pin changes (if EXWE is enabled)
5) Low voltage detector (if LVDWE is enabled). The first two cases will cause the EM78P176N to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 008H after a wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after a wake-up.

After a wake-up in IRC mode (IRC 4 MHz / 5V), the wake-up time is 1.5 μs, in XT mode (4 MHz / 5V), the wake-up time is 1.5 ms.

One or mode of Cases 2 and 5 can be enabled before going into Sleep mode. That is,

[a] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P176N can be awakened only by Case 1 or Case 2. Refer to Section 6.6, *Interrupt* for further details.

[b] if Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled. Hence, the EM78P176N can be awakened only by Case 3.

[c] if External (P60,INT) pin change is used to wake-up EM78P176N and EXWE bit of Bank 1-RE register is enabled before SLEP, WDT must be disabled. Hence, the EM78P176N can be waken-up only by Case 4.

[d] if Low voltage detector is used to wake up the EM78P176N and LVDWE bit of Bank 0-RE register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78P176N can be awakened only by Case 5.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P176N (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xxxx1110b     ; Select the WDT prescaler, it must be
                      ; set over 1:1
CONTW
WDTC                  ; Clear WDT and prescaler
MOV A, @0xxxxxxxb     ; Disable WDT
IOW RE
MOV R6, R6            ; Read Port 6
MOV A, @00000x1xb     ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)         ; Enable (or disable) global interrupt
SLEP                  ; Sleep
```

NOTE

1. *After waking up from sleep mode, WDT is automatically enabled. The WDT enable/disable operation after waking up from sleep mode should be appropriately defined in the software.*
2. *To avoid a reset from occurring when the Port 6 Input Status Changed Interrupt enters into interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above the 1:1 ratio.*

6.5.2 Wake-up and Interrupt Modes Operation Summary

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0 EXIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	EXWE = 0 EXIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1 EXIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	EXWE = 1 EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 6 Pin change	ICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector
TCC Overflow	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Detector	LVDWE = 0 LVDIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	LVDWE = 0 LVDIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWE = 1 LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	LVDWE = 1 LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

6.5.3 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	×	×	×	×	×	×	C71	C70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up	P	P	P	P	P	P	P	P
0×06	P6	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up	P	P	P	P	P	P	P	P
0×06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	P7	Bit Name	×	×	×	×	×	×	P71	P70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	P	P
		Wake-up	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	GP	INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up	Jump to Address 0x08 or continue to execute next instruction							

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×03	R3 (SR)	Bit Name	RST	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	*	*	P	P	P
		Wake-up	1	P	P	*	*	P	P	P
0×04	R4 (RSR)	Bit Name	GP	Bank 0	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up	P	P	P	P	P	P	P	P
0×0E	Bank 0 RE (LVDCR)	Bit Name	/LVD	LVDIF	×	×	×	×	×	LVDWE
		Power-on	1	0	0	0	0	0	0	0
		/RESET and WDT	1	0	0	0	0	0	0	0
		Wake-up	P	P	P	P	P	P	P	P
0×0F	Bank 0 RF (ISR)	Bit Name	×	×	×	×	×	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up	0	0	0	0	0	P	P	P
0×05	Bank 1 R5 (TBHP)	Bit Name	MLB	×	×	×	×	×	RBit 9	RBit 8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up	P	P	P	P	P	P	P	P
0×06	Bank 1 R6 (TBLP)	Bit Name	RBit7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up	P	P	P	P	P	P	P	P
0×0E	Bank 1 RE (LVD ICR)	Bit Name	LVDIE	LVDEN	LVD1	LVD0	×	×	×	EXWE
		Power-on	0	0	1	1	0	0	0	0
		/RESET and WDT	0	0	1	1	0	0	0	0
		Wake-up	P	P	P	P	P	P	P	P
0×0F	Bank 1 RF (SC & COCR)	Bit Name	×	TIMERSC	CPUS	IDLE	×	×	RCM1	RCM0
		Power-on	0	1	1	0	0	0	Word 1 <6,5>	
		/RESET and WDT	0	1	1	0	0	0		
		Wake-up	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	/PD63	/PD62	/PD61	/PD60	x	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up	P	P	P	P	1	P	P	P
0×0C	IOCC	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0D	IOCD	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up	P	P	P	P	P	P	P	P
0×0E	IOCE	Bit Name	WDTE	EIS	GP	GP	GP	GP	GP	GP
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up	1	P	P	P	P	P	P	P
0×0F	IOCF	Bit Name	×	×	×	×	×	EXIE	ICIE	TCIE
		Power-on	1	1	1	1	1	0	0	0
		/RESET and WDT	1	1	1	1	1	0	0	0
		Wake-up	1	1	1	1	1	P	P	P
0×10~ 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up	P	P	P	P	P	P	P	P

Legend: ×: Not used **U:** Unknown or don't care **P:** Previous value before reset

* Refer to the tables provided in the next section (Section 6.5.4).

6.5.4 Status of RST, T, and P of the Status Register

A Reset condition is initiated by the following events

1) A power-on condition
2) A high-low-high pulse on /RESET pin
3) Watchdog timer time-out

The values of T and P listed in the table below are used to check how the processor wakes up.

Table 6-2 Values of RST, T, and P after a Reset

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	*P
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

The following table shows the events that may affect the status of T and P.

Table 6-3 Status of T and P Being Affected by Events

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

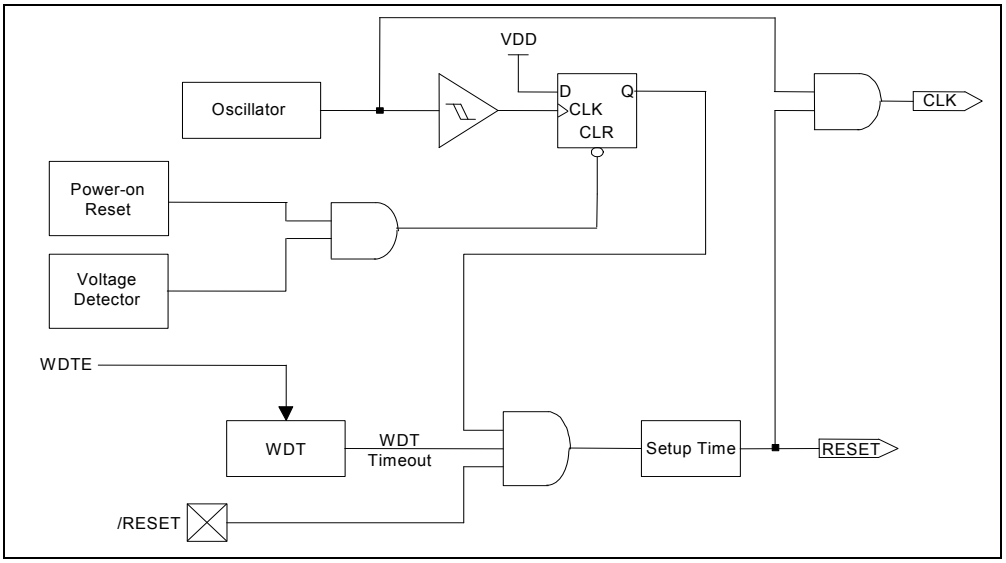


Figure 6-9 Controller Reset Block Diagram

6.6 Interrupt

The EM78P176N has four interrupts as listed below:

1) TCC overflow interrupt

2) Port 6 Input Status Change Interrupt

3) External interrupt [(P60, /INT) pin]

4) Low Voltage Detect Interrupt

Before the Port 6 Input Status Changed Interrupt is enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P176N from Sleep mode if Port 6 is enabled prior to going into Sleep mode by executing SLEP instruction. When the chip wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt Vector 008H.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Figure 6-10). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

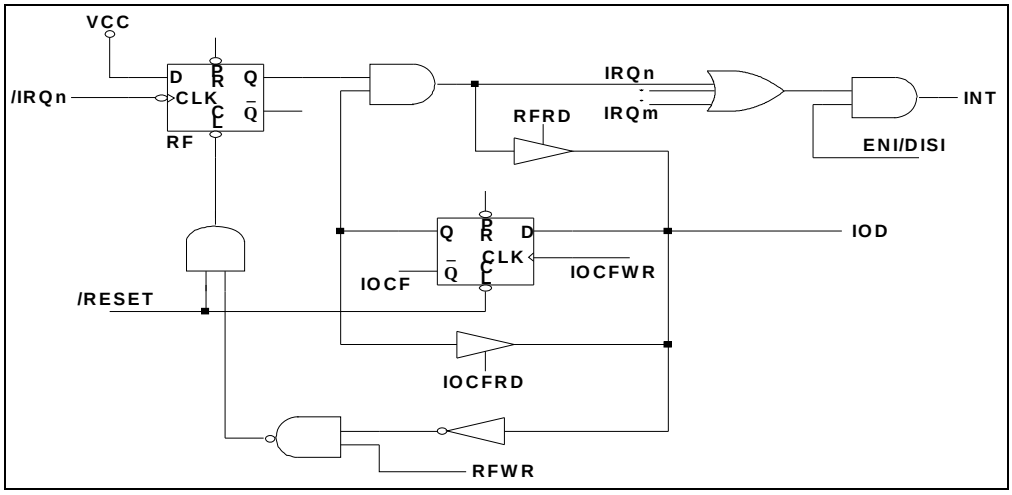


Figure 6-10 Interrupt Input Circuit

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers will be saved by the hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, the ACC, R3, and R4 registers are restored.

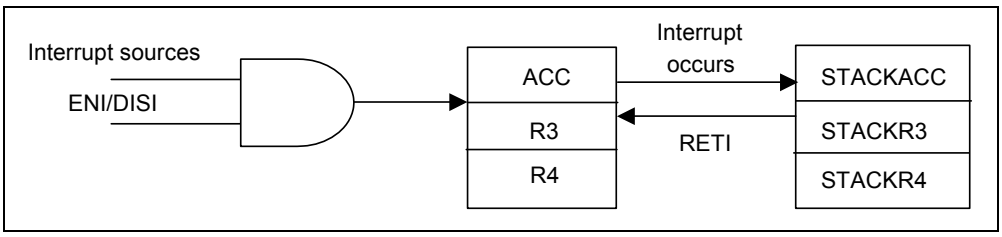


Figure 6-11 Interrupt Backup Diagram

6.7 Oscillator

6.7.1 Oscillator Modes

The EM78P176N can be operated in four different oscillator modes, such as External RC oscillator mode (ERC), Internal RC oscillator mode (IRC), High Crystal oscillator mode (XT, HXT12), and Low Crystal oscillator mode (LXT1, 2). The desired mode can be selected by programming OSC3, OSC2, OSC1 and OSC0 in the Code Option register. Table 6-4 shows how these four oscillator modes are defined.

Table 6-4 Oscillator Modes Defined by OSC

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P70/RCOUT act as P70	0	0	0	0
ERC[1] (External RC oscillator mode); P70/RCOUT act as RCOUT	0	0	0	1
IRC[2] (Internal RC oscillator mode); P70/RCOUT act as P70	0	0	1	0
IRC[2] (Internal RC oscillator mode); P70/RCOUT act as RCOUT	0	0	1	1
LXT1[3] (Frequency range of LXT1 mode is 1MHz~100kHz)	0	1	0	0
HXT1[3] (Frequency range of HXT1 mode is 20 MHz~12 MHz)	0	1	0	1
LXT2[3] (Frequency range of LXT2 mode is 32.768kHz)	0	1	1	0
HXT2[3] (Frequency range of HXT2 mode is 12 MHz~6 MHz)	0	1	1	1
XT (Frequency range of XT mode is 6 MHz~1 MHz) (default)	1	1	1	1

[1] In ERC mode, ERCin is used as oscillator pin. RCOUT/P70 is defined by Code Option Word 1 Bit 4 ~ Bit 1.

[2] In IRC mode, P55 is normal I/O pin. RCOUT/P70 is defined by code option Word 1 Bit 4 ~ Bit 1.

[3] In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

The maximum operational frequency of the crystal/resonator under different VDD is listed below.

Table 6-5 Summary of Maximum Operating Speeds

Conditions	VDD	Max Freq. (MHz)
Two cycles with two clocks	2.1	4.0
	3.0	8.0
	5.0	20.0

6.7.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P176N can be driven by an external clock signal through the OSCI pin as shown in the following figure.

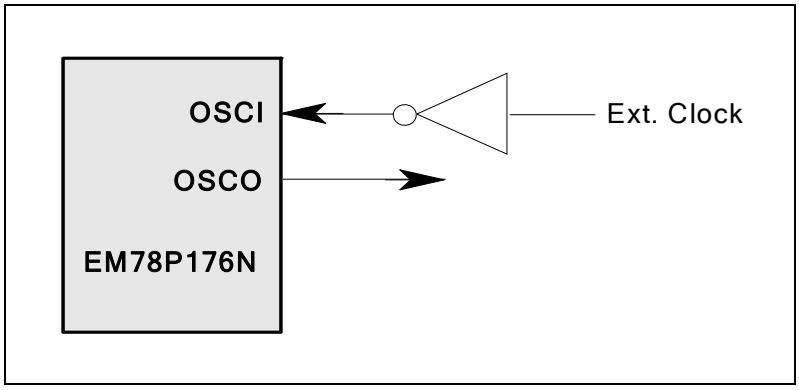


Figure 6-12 Circuit for External Clock Input

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-13 depicts such a circuit. The same thing applies whether it is in the HXT mode or in the LXT mode.

In Figure 6-14, when the connected resonator in OSCI and OSCO is used in applications, the 1 MΩ R1 needs to be shunted with resonator.

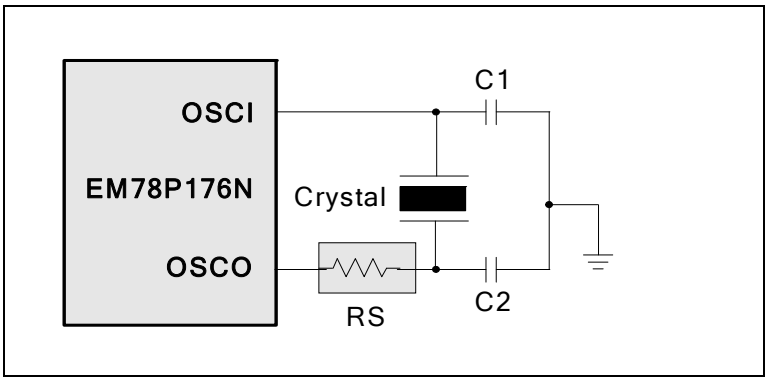


Figure 6-13 Circuit for Crystal/Resonator

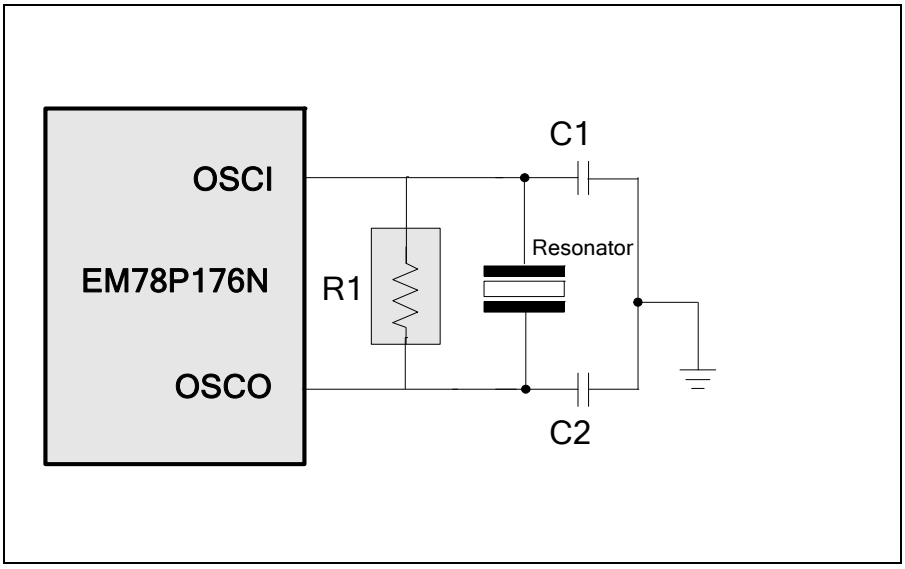


Figure 6-14 Circuit for Crystal/Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

Table 6-6 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	40pF	40pF
	LXT1 (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1~6 MHz)	455kHz	30pF	30pF
		1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MHz	30pF	30pF
	HXT2 (6~12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	20pF	20pF
		10.0 MHz	30pF	30pF
		12.0 MHz	30pF	30pF
	HXT1 (12~20 MHz)	12.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF
		20.0 MHz	15pF	15pF

6.7.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (Figure 6-15) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

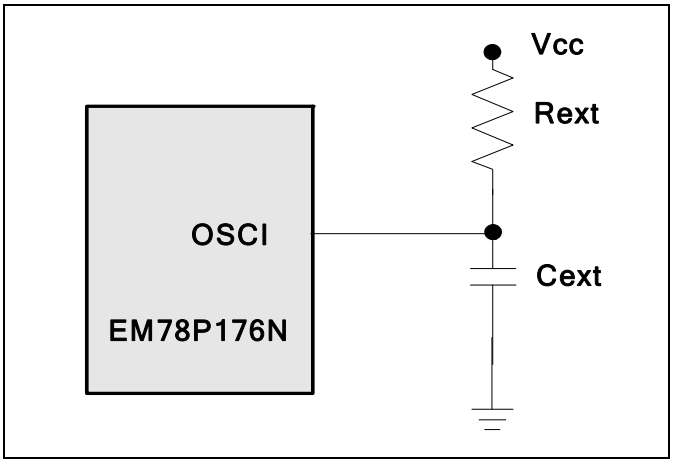


Figure 6-15 External RC Oscillator Mode Circuit

Table 6-7 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20pF	3.3k	2.064 MHz	1.901 MHz
	5.1k	1.403 MHz	1.316 MHz
	10k	750kHz	719.7kHz
	100k	81.45kHz	81.33kHz
100pF	3.3k	647.3kHz	615.1 MHz
	5.1k	430.8kHz	414.3kHz
	10k	225.8kHz	219.8kHz
	100k	23.88kHz	23.96kHz
300pF	3.3k	256.6kHz	245.3kHz
	5.1k	169.5kHz	163.0kHz
	10k	88.53kHz	86.14kHz
	100k	9.283kHz	9.255kHz

Note: 1: These are measured in DIP packages.

2. The values are for design reference only.

3. The frequency drift is ± 30%.

6.7.4 Internal RC Oscillator Mode

EM78P176N offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz, and 16 MHz) that can be set by Code Option (Word 1), RCM1, and RCM0. All these four main frequencies can be calibrated by programming the Option Bits C0 ~ C4. The table below describes the EM78P176N internal RC drift with variation of voltage, temperature, and process.

Table 6-8 Internal RC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.1V~5.5V)	Process	Total
4 MHz	± 2%	± 3%	± 2%	± 7%
16 MHz	± 2%	± 3%	± 2%	± 7%
8 MHz	± 2%	± 3%	± 2%	± 7%
1 MHz	± 2%	± 3%	± 2%	± 7%

Note: *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

6.8 Code Option Register

The EM78P176N has a Code Option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

■ **Code Option Register and Customer ID Register Arrangement Distribution:**

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.8.1 Code Option Register (Word 0)

Word 0													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	RESETEN	ENWDT	CLKS	LVR1	LVR0	–	–	–	NRHL	NRE	Protect		
1	disable	disable	4 clocks	High	High	–	–	–	High	High	Disable		
0	enable	enable	2 clocks	Low	Low	–	–	–	Low	Low	Enable		

Bit 12 (RESETEN): Define Pin 71 as a reset pin

0 : /RESET enable

1 : /RESET disable

Bit 11 (ENWDT): Watchdog timer enable bit

0 : Enable

1 : Disable

Bit 10 (CLKS): Instruction period option bit.

0 : Two oscillator periods

1 : Four oscillator periods

Refer to the Instruction Set section.

Bits 9 ~ 8 (LVR1 ~ LVR0): Low Voltage Reset control bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.0V

Bit 7: Not used. Set to "1" at all time.

Bit 6 and Bit 5: Not used. Set to "1" at all time.

Bit 4 (NRHL): Noise rejection high/low pulse define bit. INT pin has a falling edge trigger.

0 : Pulses equal to 8/fc is regarded as signal

1 : Pulses equal to 32/fc is regarded as signal (Default)

Bit 3 (NRE): Noise rejection enable

0 : Disable noise rejection

1 : Enable noise rejection (default). However in Low Crystal oscillator (LXT2) mode, the noise rejection circuit is always disabled.

Bits 2 ~ 0 (Protect**):** Protect Bits. Each protect status is as follows:

Protect Bits	Protect
0	Enable
1	Disable **(Default)**

6.8.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	HLP	C4	C3	C2	C1	C0	RCM1	RCM0	OSC3	OSC2	OSC1	OSC0	RCOUT
1	High	High	High	High	High	High	High	High	High	High	High	High	System-clock
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Open-drain

Bit 12 (HLP): Power consumption mode

0 : Low power consumption mode, applies to operating frequency at 400kHz or below 400kHz

1 : High power consumption mode, applies to operating frequency above 400kHz (default)

Bits 11 ~ 7 (C4 ~ C0): Internal RC mode Calibration bits. These bits must always be set to "1" only (auto calibration)

Bit 6 and Bit 5 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
1	1	4
1	0	16
0	1	8
0	0	1

* Theoretical values, for reference only

Bits 4 ~ 1 (OSC3, OSC2, OSC1 and OSC0): Oscillator Mode Selection bits

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P70/RCOUT act as P70	0	0	0	0
ERC[1] (External RC oscillator mode); P70/RCOUT act as RCOUT	0	0	0	1
IRC[2] (Internal RC oscillator mode); P70/RCOUT act as P70	0	0	1	0
IRC[2] (Internal RC oscillator mode); P70/RCOUT act as RCOUT	0	0	1	1
LXT1[3] (Frequency range of LXT1 mode is 1MHz~100kHz)	0	1	0	0
HXT1[3] (Frequency range of HXT1 mode is 20 MHz~12 MHz)	0	1	0	1
LXT2[3] (Frequency range of LXT2 mode is 32.768kHz)	0	1	1	0
HXT2[3] (Frequency range of HXT2 mode is 12 MHz~6 MHz)	0	1	1	1
XT (Frequency range of XT mode is 6 MHz~1 MHz) (default)	1	1	1	1

[1] In ERC mode, ERCin is used as oscillator pin. RCOUT/P64 is defined by code option Word 1 Bit 4 ~ Bit 1.
[2] In IRC mode, P65 is normal I/O pin. RCOUT/P64 is defined by code option Word 1 Bit 4 ~ Bit 1.
[3] In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

Bit 0 (RCOUT): System clock or open-drain enable bit in IRC or ERC mode

0 : RCOUT pin is open drain

1 : RCOUT output system clock **(Default)**

6.8.3 Customer ID Register (Word 2)

Word 2													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	SFS	TYPE	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	–	16K	20 PIN	High	High	High	High	High	High	High	High	High	High
0	–	128K	18 PIN	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bit 12: Not used. Set to "1" at all time.

Bit 11 (SFS): Sub Frequency Select for Green mode.

(Not included WDT time out and POR release setup-up time)

0 : 128kHz

1 : 16kHz (default)

Bit 10 (TYPE): Type selection for EM78P176N

Type	MCU Type
0	EM78P176N-18Pin
1	EM78P176N-20Pin (Default)

Bits 9 ~ 0: Customer's ID code

6.9 Power-on Consideration

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes at its steady state. Under customer application, when power is OFF, Vdd must drop to below 1.8V and remains OFF for 10 μs before power can be switched ON again. This way, the EM78P176N will reset and operate normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

6.10 External Power-on Reset Circuits

The circuitry in the figure implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time.

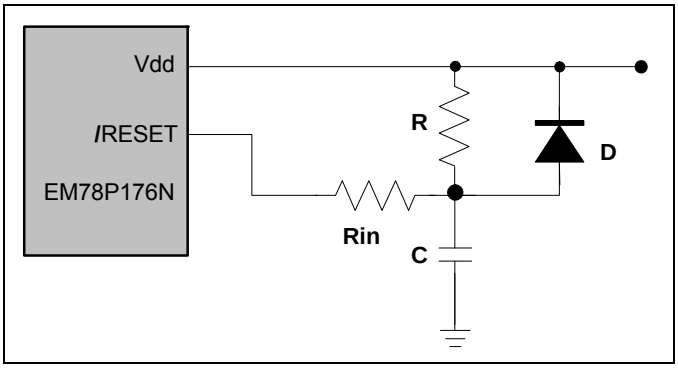


Figure 6-16 External Power-up Reset Circuit

Since the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

6.11 Residue-Voltage Protection

When the battery is replaced, the device power (Vdd) is cut off but the residue-voltage remains. The residue-voltage may trip below the minimum Vdd, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to build a residue-voltage protection circuit for the EM78P176N.

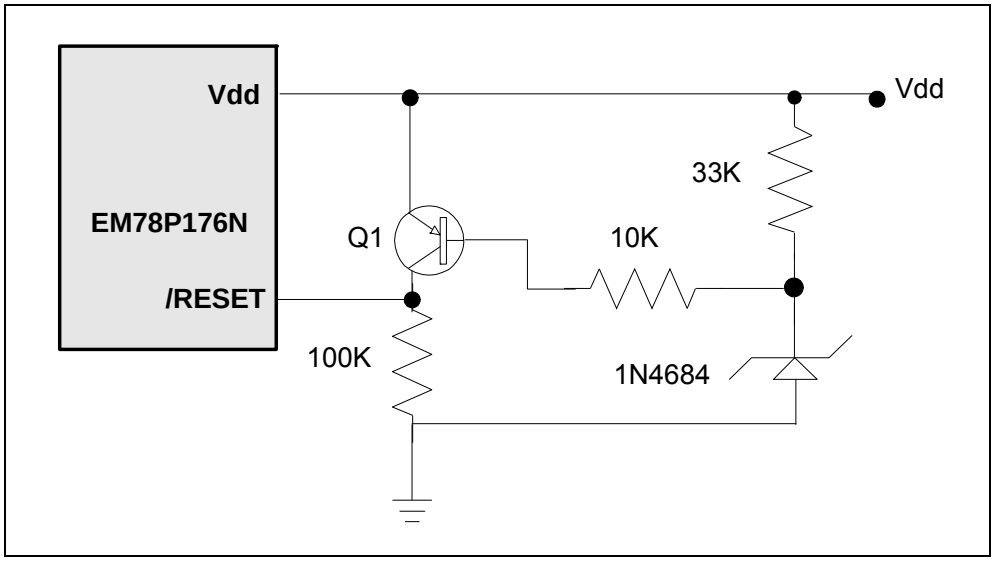


Figure 6-17 Residue Voltage Protection Circuit 1

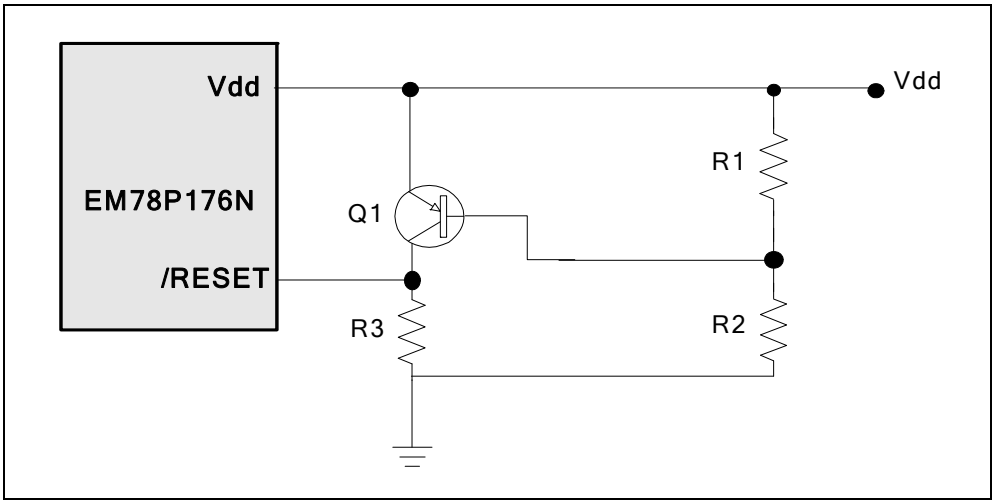


Figure 6-18 Residue Voltage Protection Circuit 2

NOTE

Figure 6-17 and Figure 6-18 should be designed to ensure that the voltage of the /RESET pin is larger than VIH (min).

6.12 Low Voltage Detector

When an unstable power source condition occurs, such as external power noise interference or EMS test condition, a violent power vibration is generated. At the same time, the Vdd becomes unstable as it could be operating below working voltage. When the system supply voltage (Vdd) is below the operating voltage, the IC kernel will automatically keep all register status.

6.12.1 Low Voltage Reset (LVR)

LVR property is set at Bits 9 and 8 of Code Option Word 0. Detailed operation mode is as follows**:**

Word 0										
Bit 12	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2 ~ Bit 0**
RESETEN	ENWDT	CLKS	LVR1	LVR0	–	–	–	NRHL	NRE	Protect

Bits 9 ~ 8 (LVR1 ~ LVR0): Low Voltage Reset enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	N/A (Power-on Reset)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

6.12.2 Low Voltage Detector (LVD)

LVD property is set at Registers Bank 0-RE and Bank 1-RE. Detailed operation mode is explained below.

6.12.2.1 Bank 0 RE (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/LVD	LVDIF	-	-	-	-	-	LVDWE

Bit 7 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than the LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bit 6 (LVDIF): Low Voltage Detector Interrupt Flag

LVDIF is reset to "**0**" by software or hardware

Bit 6 of Bank 0-RE: "1" means there's interrupt request, and "0" means no interrupt occurs.

Bit 0 (LVDWE): Low Voltage Detect wake-up enable bit

0: Disable Low Voltage Detect wake-up

1: Enable Low Voltage Detect wake-up

When the Low Voltage Detect is used to enter interrupt vector or to wake-up IC from Sleep/Idle mode with the Low Voltage Detect running, the LVDWE bit must be set to “Enable.“

6.12.2.2 Bank 1 RE (LVD Interrupt and Wake-up Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD1	LVD0	-	-	-	EXWE

NOTE

- *The BANK1-RE <7> register is both readable and writable.*
- *Individual interrupt is enabled by setting its associated control bit in the BANK1-RE<7> to "**1**."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-10 (Interrupt Input Circuit) in Section 6.6 (Interrupt).*

Bit 7 (LVDIE): Low voltage Detector interrupt enable bit

0: Disable Low Voltage Detector interrupt

1: Enable Low Voltage Detector interrupt

When a detected low level voltage state is used to enter an interrupt vector or enter the next instruction, the LVDIE bit must be set to “Enable.”

Bit 6 (LVDEN): Low Voltage Detector enable bit

0: Disable Low voltage detector

1: Enable Low voltage detector

Bits 5 ~ 4 (LVD1 ~ LVD0): Low Voltage Detector level bits

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	NA	1

NOTE

IF Vdd has crossover at LVD voltage in interrupt level as VDD varies, LVD interrupt will occur.

6.12.3 Programming Process

Follow these steps to obtain data from the LVD**:**

1. Write to the two bits (LVD1: LVD0) on the BANK1-RE (LVDCR) register to define the LVD level
2. Set the LVDWE bit if the wake-up function is in use.
3. Set the LVDIE bit if the interrupt function is in use.
4. Write “ENI” instruction if the interrupt function is in use.
5. Set LVDEN bit to “**1**”
6. Write “SLEP” instruction or Polling /LVD bit
7. Clear the interrupt flag bit (LVDIF) when Low Voltage Detect occurs.

NOTE

- *The internal LVD module uses the internal circuit, and when the code option is set to enable the LVD module, the current consumption will increase to about 5 μA.*
- *During Sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detection point, the LVDIF bit will be set and the device will wake up from Sleep mode. The LVD interrupt flag will remain set at priority status.*
- *When the system resets, the LVD flag is cleared.*

The following figure shows the LVD module detection point in an external voltage condition.

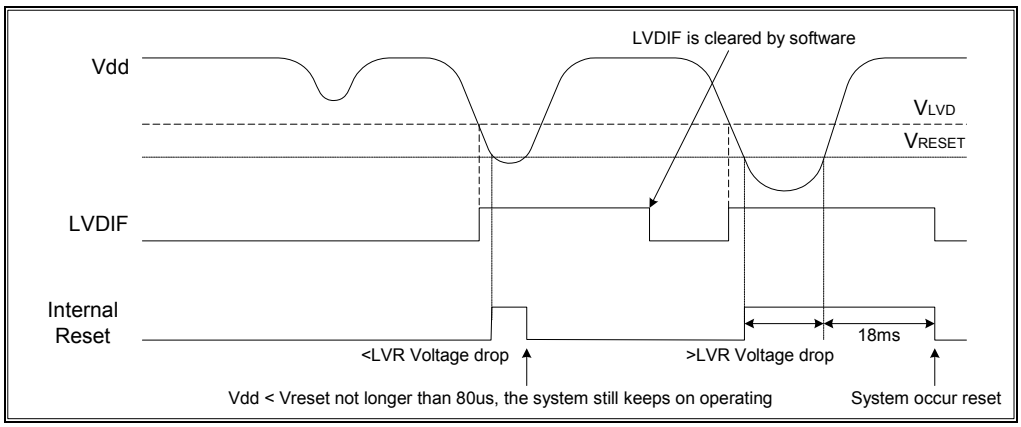


Figure 6-19 LVD/LVR Waveform with the Detection Point in an External Voltage Condition

- When the Vdd drops, but above VLVD, the LVDIF is kept at "**0**".
- When Vdd drops below VLVD, the LVDIF is set to "**1**". If global ENI is enabled, the LVDIF is also set to "**1**" and the next instruction will branch to an interrupt vector. The LVD interrupt flag is cleared to "**0**" by software.
- When Vdds drops below VRESET at less than 80 µs, the system will keep all the registers' status and halts it operation, but with the oscillation remaining active.
- When Vdd drops below VRESET at more than 80 µs, a system reset will occur. Refer to Section 6.5.1, *Reset* for the detailed Reset description.

6.13 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

A) Modify one instruction cycle to consist of four oscillator periods.

B) "JMP", "CALL", "RET", "RETL", "RETI" or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within one instruction cycle. The instructions that are written to the program counter also take one instruction cycle.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low; and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc/2.

Moreover, the instruction set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The following symbols are used in the Instruction Set table**:**

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.
Bit 6 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None

[1] This instruction is applicable to IOC5~IOC6, IOCB ~ IOCF only.

(Continuation)

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C,DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK k	k → R4(6)	None
1 1110 11rr rrrr	1Err	TBRD R	If Bank1 R5.7=0, machine code (7:0) → R Else Bank1 R5.7 = 1 machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None

Note: [2] This instruction is not recommended for RF operation.

[3] This instruction cannot operate under RF.

7 Absolute Maximum Ratings

■ **EM78P176N**

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	20 MHz

NOTE

These parameters are theoretical values and have not been tested.

8 Electrical Characteristics

8.1 DC Characteristics

Ta=25°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 2.1V	Two cycles with two clocks	DC	–	4.0	MHz
	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8.0	MHz
	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	20.0	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100pF	F±30%	940	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6, 7	2.0	–	–	V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6, 7	–	–	0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	2.0	–	–	V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	–	–	0.8	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	2.5	–	–	V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI	–	–	1.0	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6, 7	1.5	–	–	V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6, 7	–	–	0. 4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)	1.5	–	–	V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)	–	–	0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	1.5	–	–	V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI	–	–	0.6	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOH1	Output High Voltage (Ports 5, Ports 6, Ports 7)	IOH = -12mA	2.4	–	–	V
VOL1	Output Low Voltage (P50~54, P56~57, Ports 6) (Schmitt trigger)	IOL = 12mA	–	–	0.4	V
VOL2	Output Low Voltage (P70, P55)	IOL = 16.0mA	–	–	0.4	V
VOL3	Output Low Voltage (P71)	IOL = 20mA	–	–	0.4	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	70	–	85	µA
IPD	Pull-down current	Pull-down active, Input pin at VDD	25	–	40	µA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	–	1	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	10	µA
ICC1	Operating supply current at two clocks (VDD=3V)	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	15	20	µA
ICC2	Operating supply current at two clocks (VDD=3V)	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	15	25	µA
ICC3	Operating supply current at two clocks (VDD=5.0V)	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating	–	–	1.5	mA
ICC4	Operating supply current at two clocks (VDD=5.0V)	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating	–	–	2.8	mA

NOTE

These parameters are theoretical values and have not been tested.

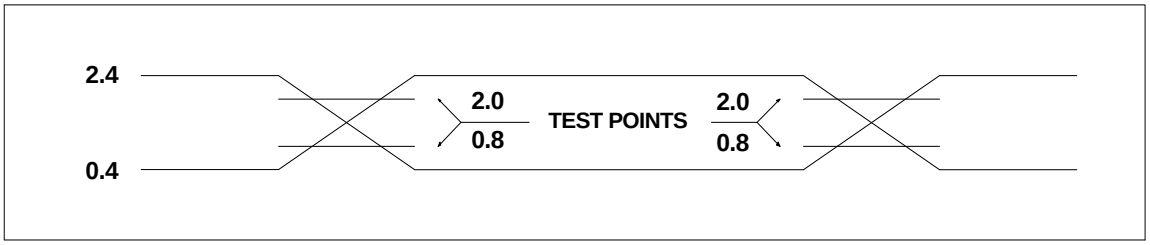
8.2 AC Characteristics

Ta=25°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C, XTAL	16.8-30%	16.8	16.8+30%	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt1	Watchdog timer period	Ta = 25°C	16.8-30%	16.8	16.8+30%	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

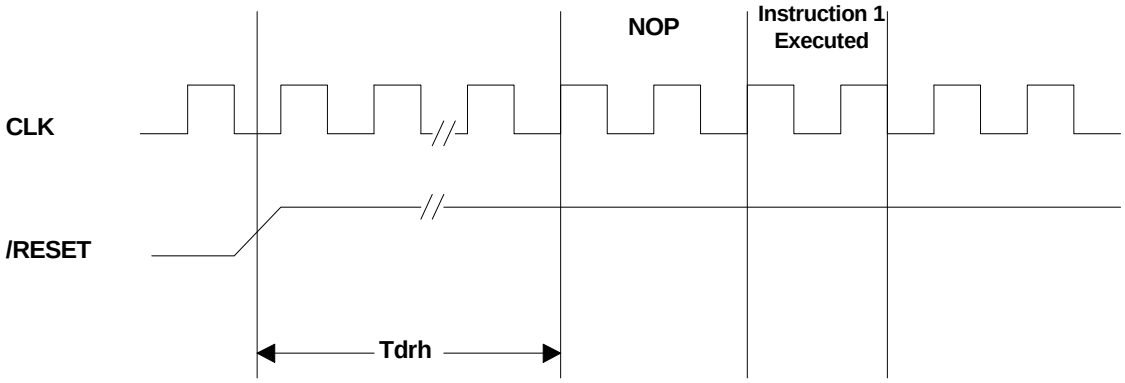
9 Timing Diagrams

AC Test Input/Output Waveform



AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")

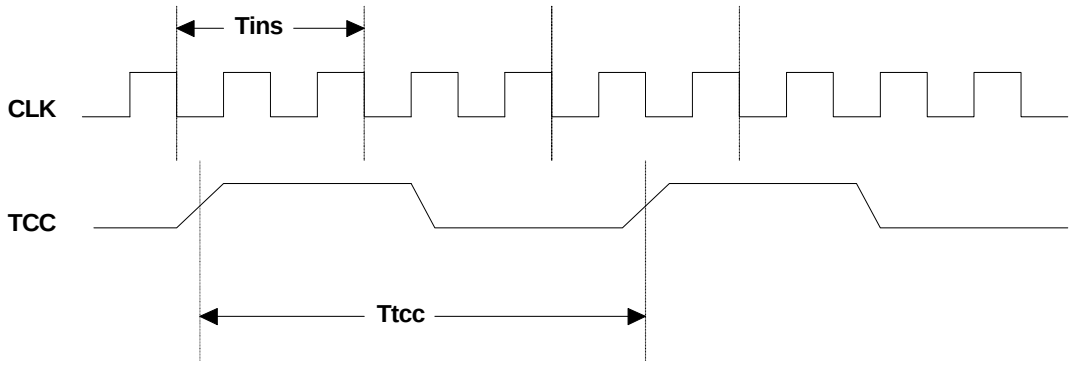


Figure 9-1 EM78P176N Timing Diagrams

APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P176NSS20J/S	SSOP	20	209 mil
EM78P176NSO20J/S	SOP	20	300 mil
EM78P176ND18J/S	DIP	18	300 mil
EM78P176NSO18J/S	SOP	18	300 mil
EM78P176NSS10J/S	SSOP	10	150 mil
EM78P176NMS10J/S	MSOP	10	118 mil

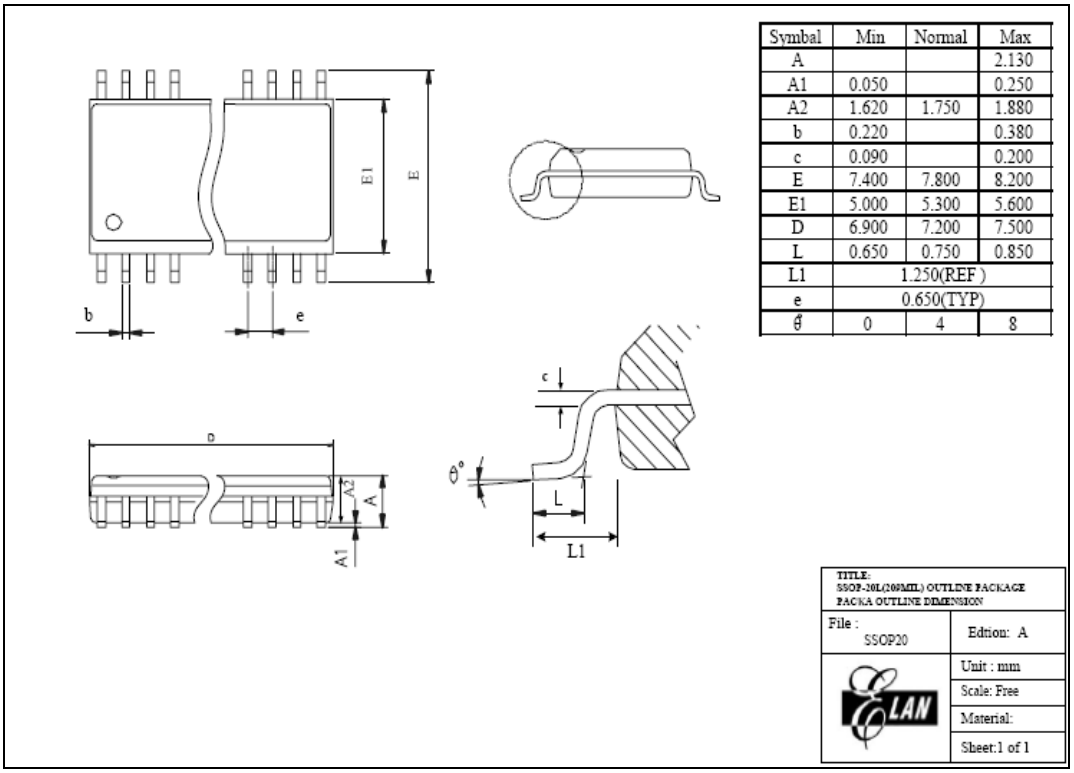
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78P176N
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

- **20-Lead Shrink Small Outline Package (SSOP) — 209 mil**



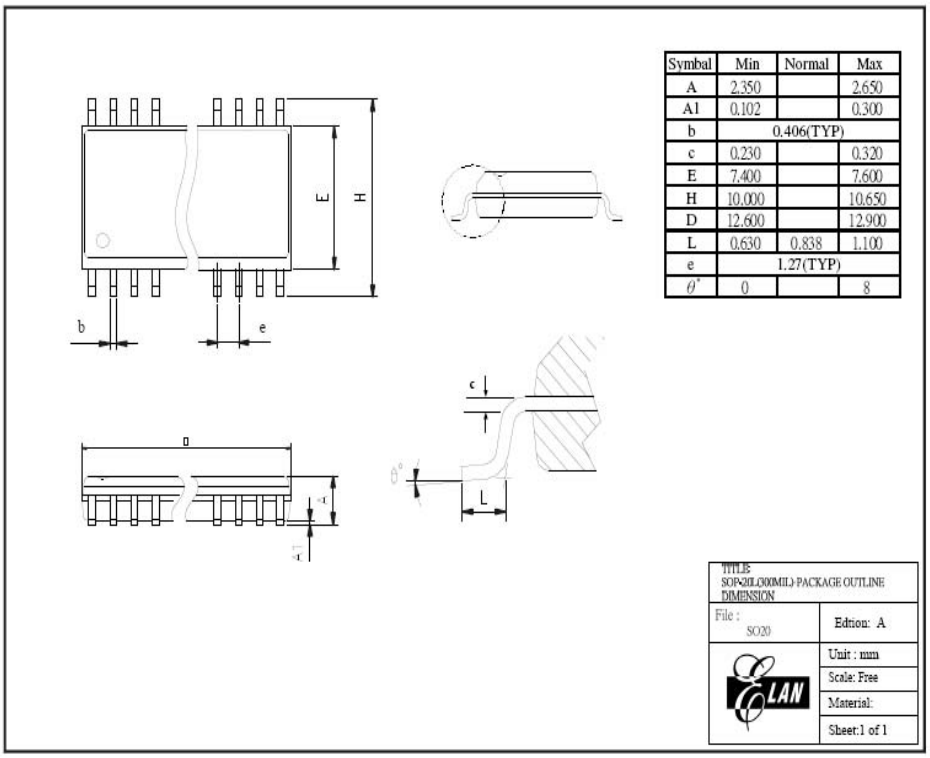
Symbal	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ	0	4	8

TITLE:
SSOP-20L(209MIL) OUTLINE PACKAGE
PACKA OUTLINE DIMENSION

File : SSOP20 | Edtion: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure B-1a EM78P176N 20-Lead SSOP Package Type

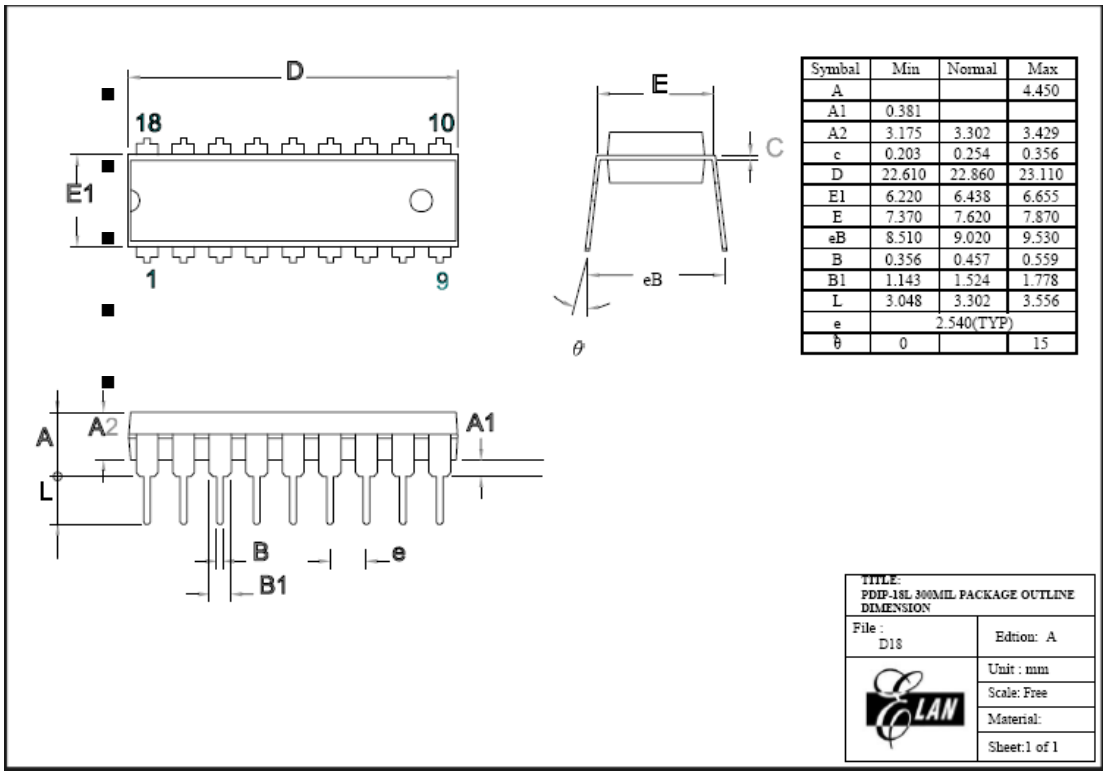
■ **20-Lead Small Outline Package (SOP) — 300 mil**



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

Figure B-1b EM78P176N 20-Lead SOP Package Type

- **18-Lead Plastic Dual In–line Package (DIP) — 300 mil**



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e		2.540(TYP)	
θ	0		15

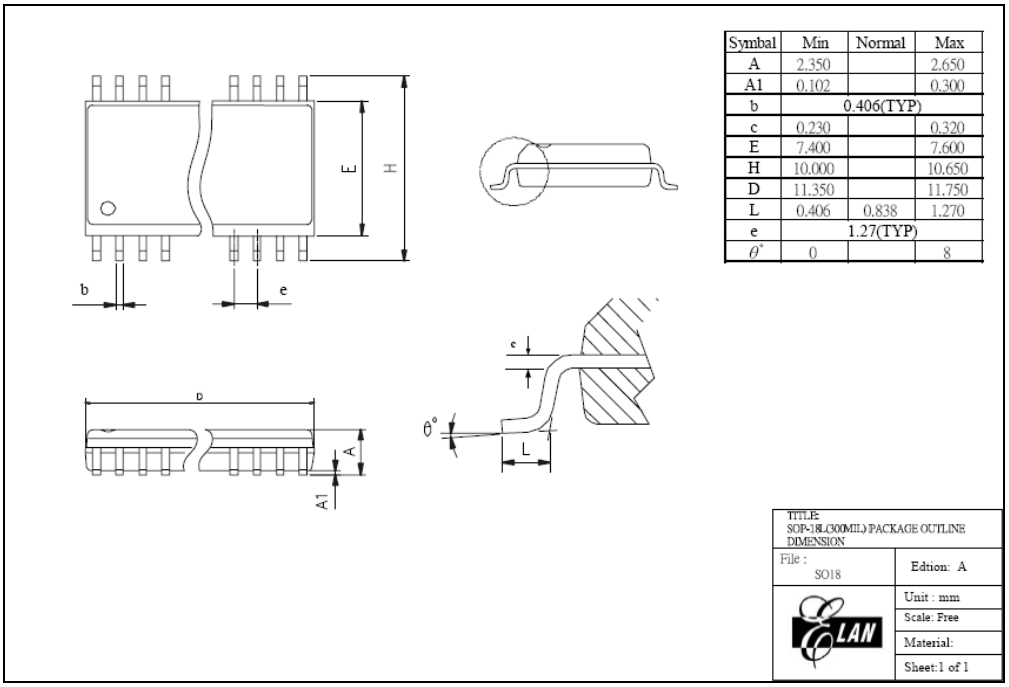
TITLE:
PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION

File : D18 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure B-1c EM78P176N 18-Lead DIP Package Type

■ 18-Lead Small Outline Package (SOP) — 300 mil

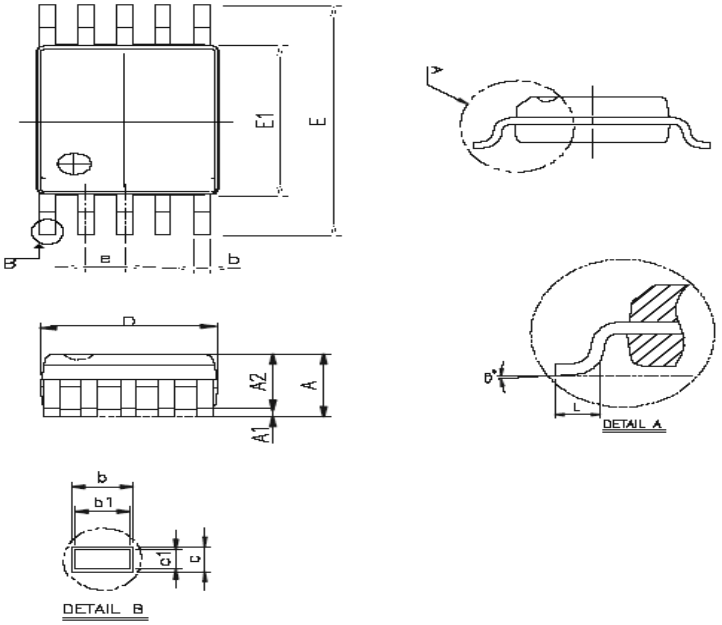


Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1d EM78P176N 18-Lead SOP Package Type

■ **10-Lead Shrink Small Outline Package (SSOP) — 150 mil**

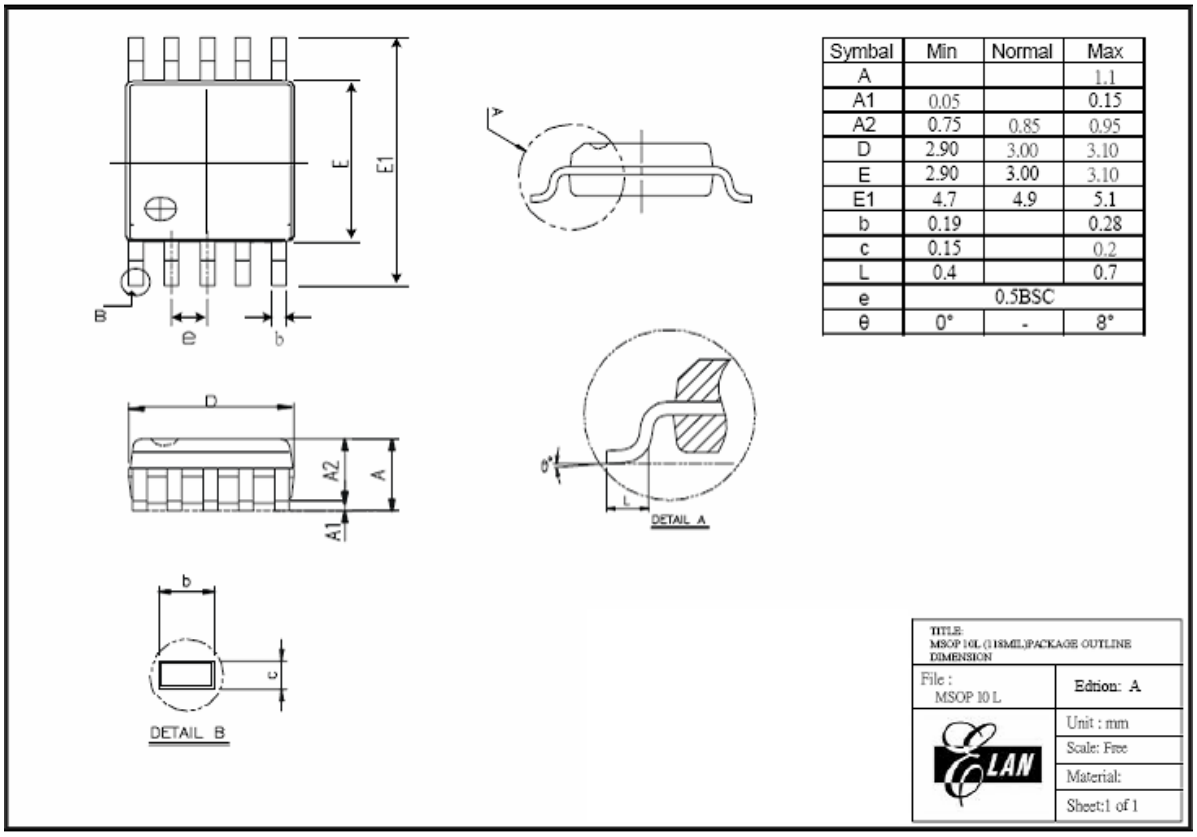


Symbal	Min	Normal	Max
A	1.35	1.55	1.75
A1	0.075	0.175	0.275
A2	1.18	1.38	1.58
D	4.7	4.9	5.1
E	5.8	6.0	6.2
E1	3.7	3.9	4.1
b	0.406		0.496
b1	0.406		0.456
c	0.178		0.278
c1	0.178		0.228
L	0.55	0.65	0.75
e		1.00TYP	
θ	0°	-	7°

TITLE: SSOP 10L (150MIL)PACKAGE OUTLINE DIMENSION	
File : SSOP 10 L	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1e EM78P176N 10-Lead SSOP Package Type

■ **10-Lead Micro Small Outline Package (MSOP) — 118 mil**



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e		0.5BSC	
θ	0°	-	8°

Figure B-1f EM78P176N 10-Lead MSOP Package Type