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SPECIFICATION

CUSTOMER ： _____

MODULE NO.: WF35CTIBCDB#

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

VERSION	DATE	REVISED PAGE NO.	SUMMARY
C	2011.02.14	19	Modify CON1=20pin

RECORDS OF REVISION

DOC. FIRST ISSUE

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2009.08.06		First issue
A	2010.11.29	19	Modify CON1=22pin
B	2011.01.03	10~17	Correct DC Characteristics & AC Characteristics &Data transfer order Setting & SSD1963 Version
C	2011.02.14	19	Modify CON1=20pin

Contents

1.Module Classification Information

W	F	35	C	T	I	B	C D B #
①	②	③	④	⑤	⑥	⑦	⑧ ⑨⑩ ⑪

① Brand：WINSTAR DISPLAY CORPORATION

② Display Type：H→Character Type, G→Graphic Type F→TFT Type

③ Display Size：3.5” TFT

④ Model serials no.

⑤ Backlight Type： F→CCFL, White T→LED, White

⑥ LCD Polarize Type/ Temperature range/ View direction

A→Reflective, N.T, 6:00	H→Transflective, W.T,6:00
D→Reflective, N.T, 12:00	K→Transflective, W.T,12:00
G→Reflective, W. T, 6:00	C→Transmissive, N.T,6:00
J→Reflective, W. T, 12:00	F→Transmissive, N.T,12:00
B→Transflective, N.T,6:00	I→Transmissive, W. T, 6:00
E→Transflective, N.T.12:00	L→Transmissive, W.T,12:00

⑦ A: TFT LCD
B: TFT+FR+CONTROL BOARD
C: TFT+FR+A/D BOARD
D:TFT+FR+A/D BOARD+CONTROL BOARD

⑧ Solution: A: 128160 B:320234 C:320240 D:480234

⑨ D: Digital A: Analog

⑩ Version

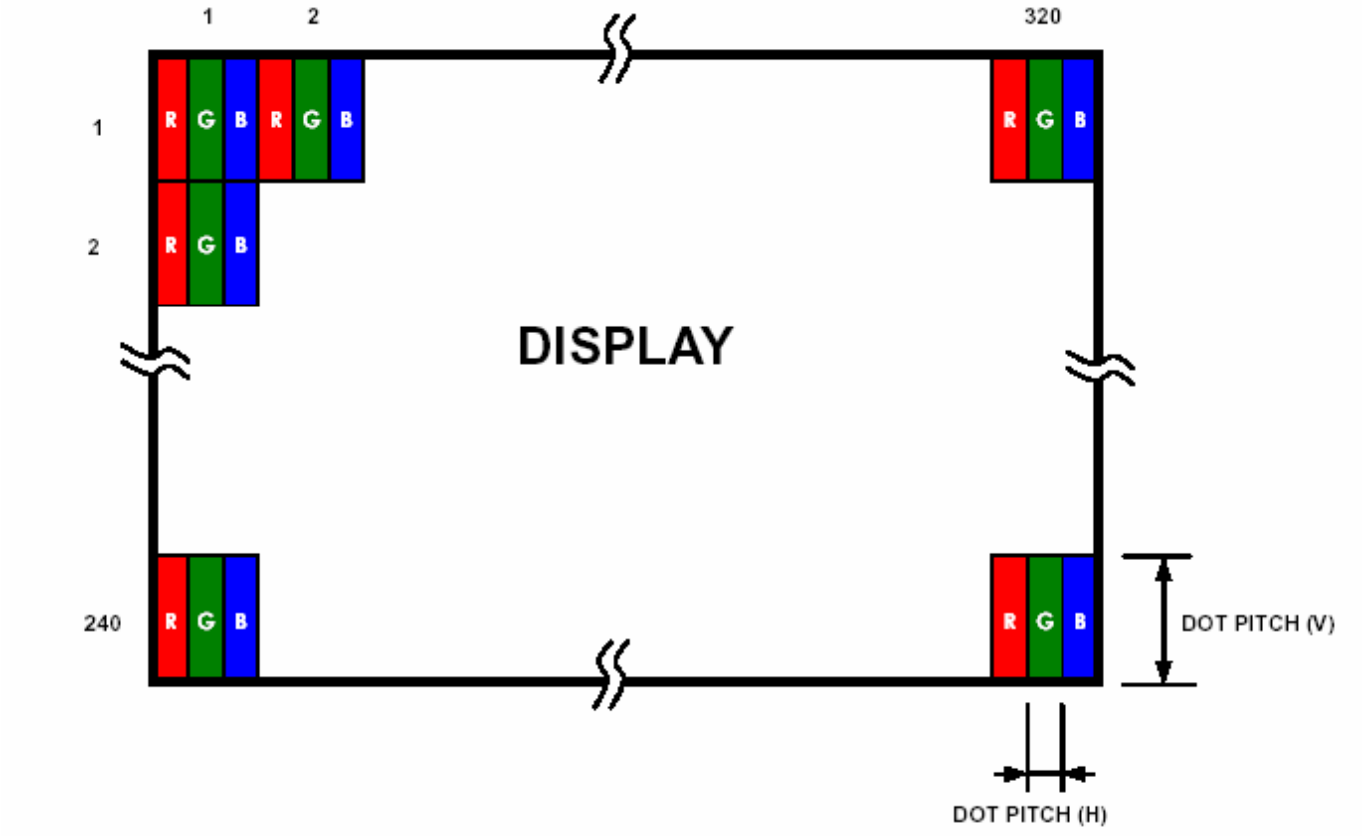
⑪ Special Code #:Fit in with ROHS directive regulations

This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of WF35CTIBCDB#

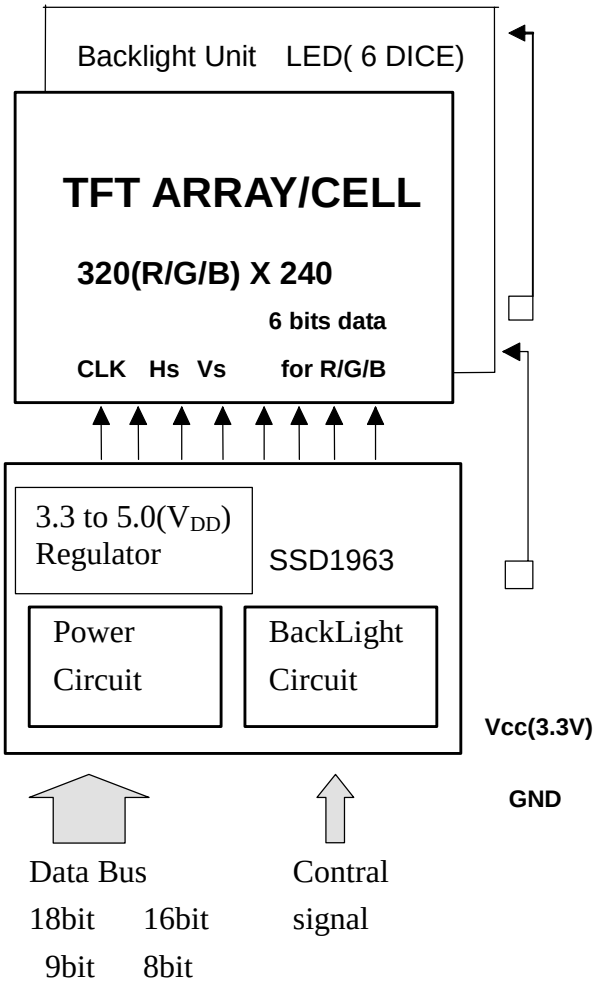
Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	93.5 x 66.44 x 7.96	mm
View area	73.1x55.6	mm
Active area	70.08 x 52.56	mm
Dot size	0.073 x 0.219	mm
Driving IC package	COG	
LCD type	TFT, Negative, Transmissive	
View direction	6 o'clock	
Backlight Type	LED,Normally White	
Controller IC	SSD1963	

*Expose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating failure.

*Color tone slight changed by temperature and driving voltage.



2.Block Diagram

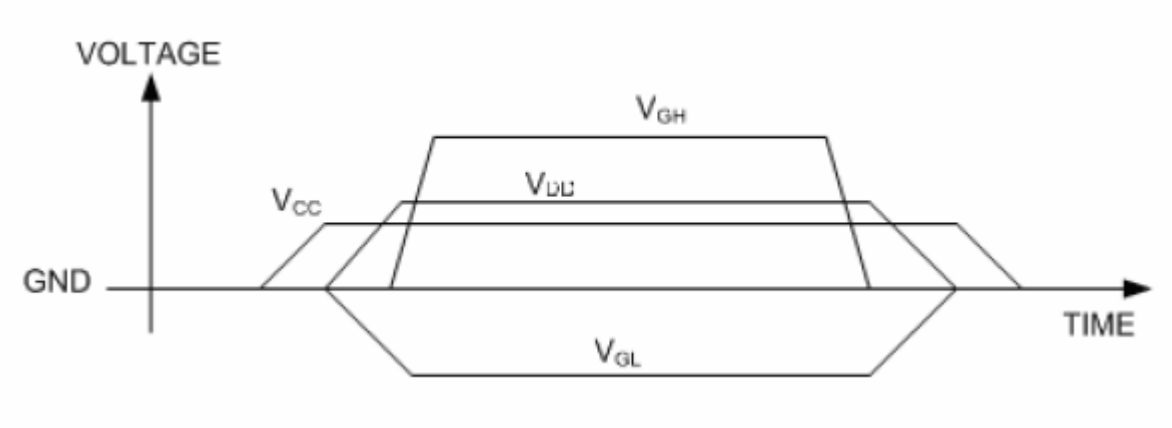


3.Electrical Characteristics

3.1 Operating conditions:

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCC	—	3.0	3.3	3.6	V
Power Supply Voltage	V_{GH}	Ta=25℃		15		V
	V_{GL}	Ta=25℃		-10		V
Supply Current	I_{cc}	V_{CC}=3		213		mA (*NOTE1)

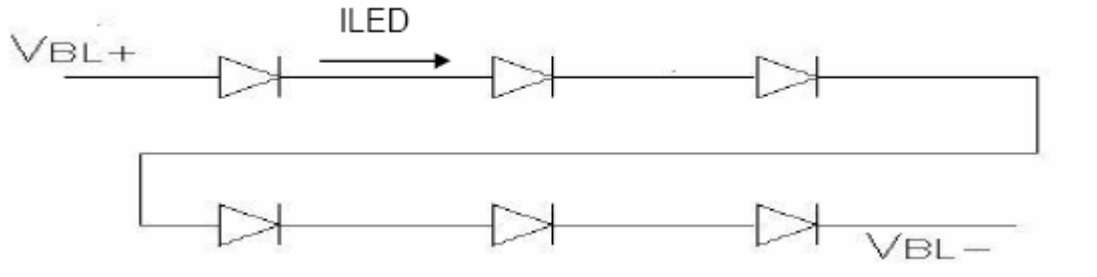
*Note1：VcomH& VcomL：Adjust the color with gamma data.



3.3 LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		-	20	-	mA	
Power Consumption		-	400	420	mW	
LED voltage	VBL+	18.6	19.8	21	V	Note 1
LED Life Time	-		(50,000)-	-	Hr	Note 2,3

Note 1 : There are 1 Groups LED



Note 2 : Ta = 25 _

Note 3 : Brightness to be decreased to 50% of the initial value

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Power Voltage	V_{GH}	-0.3	—	32.0	V
	V_{GL}	-22.0	—	0.3	V
	V_{GH} - V_{GL}	-0.3	—	+45	V
Input voltage	Vin	-0.5	—	4.6	V
Logic output Voltage	V_{OUT}	-0.5	—	4.6	V

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

5.Interface Pin Function

5.1 Pins Connection To Control Board

P/N	Symbol	8BIT Function
1	GND	Ground
2	VCC	Power supply for Logic
3	BL_E	Backlight control (H: On \ L: Off)
4	RS	Command/Data select
5	WR	8080 family MPU interface : Write signal
6	RD	8080 family MPU interface: Read signal
7	DB0	Data bus
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	CS	Chip select
16	RES	REST
17	NC	No connection
18	FGND	Frame Gnd
19	NC	No connection
20	NC	No connection

6. DC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PSTY	Quiescent Power			300	500	uW
IIZ	Input leakage current		-1		1	uA
IOZ	Output leakage current		-1		1	uA
VOH	Output high voltage		0.8VDDIO			V
VOL	Output low voltage				0.2VDDIO	V
VIH	Input high voltage		0.8VDDIO		VDDIO + 0.5	V
VIL	Input low voltage				0.2VDDIO	V

7. AC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

7.1 Clock Timing

Table 7-1:Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-2:Clock Input Requirements for CLK

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-3:Clock Input Requirements for crystal oscillator XTAL

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

7.2 MCU Interface Timing

7.2.1 Parallel 6800-series Interface Timing

Table 7-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSL	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 7-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)

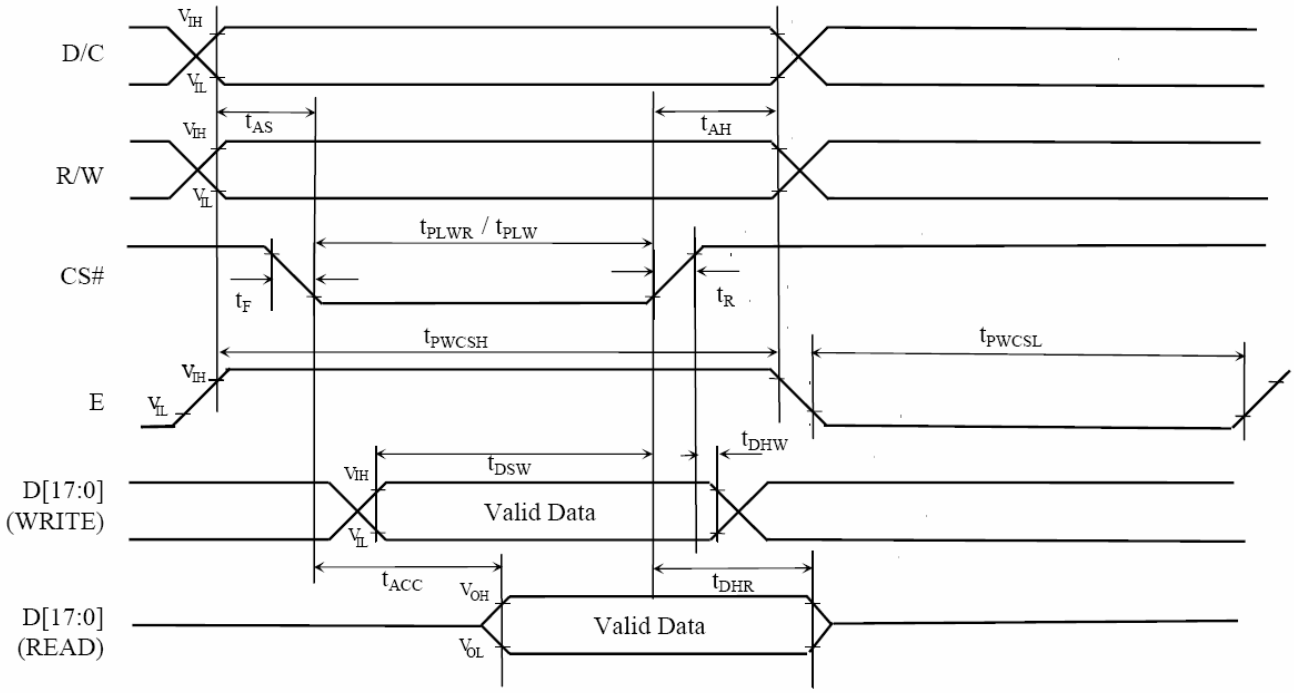
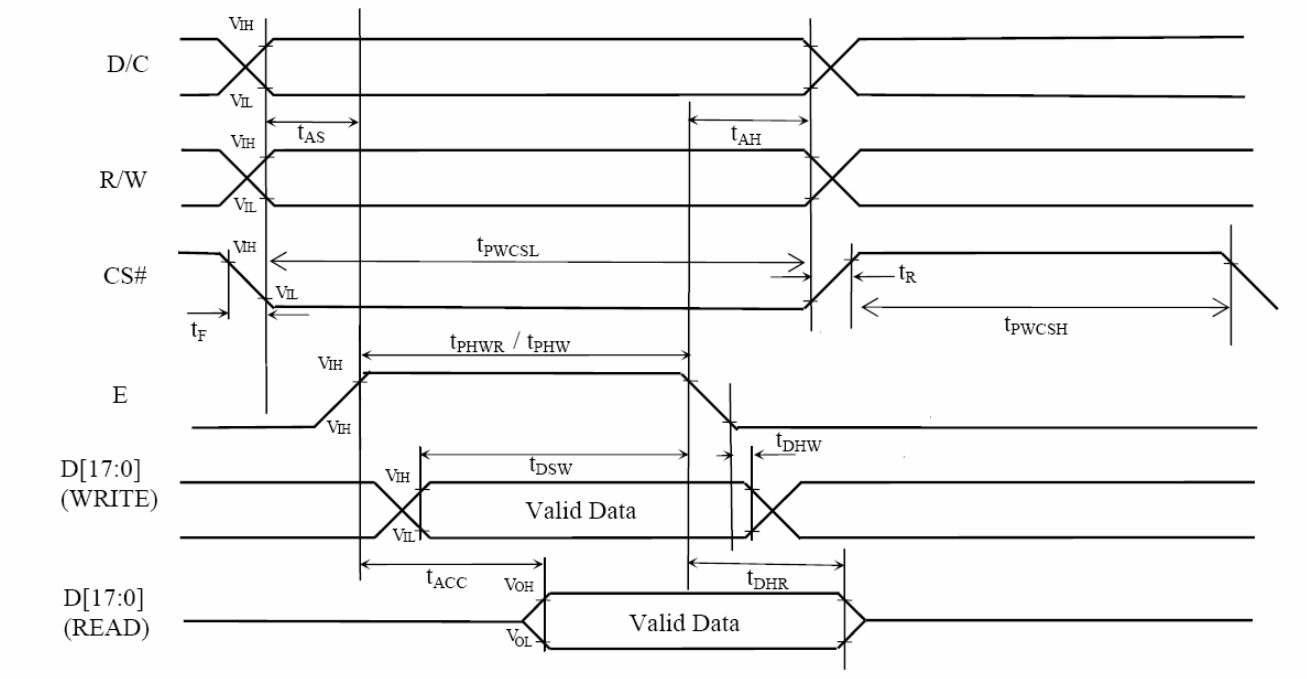


Table 7-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure7-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)



7.2.2 Parallel 8080-series Interface Timing

Table 7-6: Parallel 8080-series Interface

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		1	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Write Data Setup Time		4	-	-	ns
tDHW	Write Data Hold Time		1	-	-	ns
tPWLW	Write Low Time		12	-	-	ns
tDHR	Read Data Hold Time		1	-	-	ns
tACC	Access Time		32	-	-	ns
tPWLR	Read Low Time		36	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns
tCS	Chip select setup time		2	-	-	ns
tCSH	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 7-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

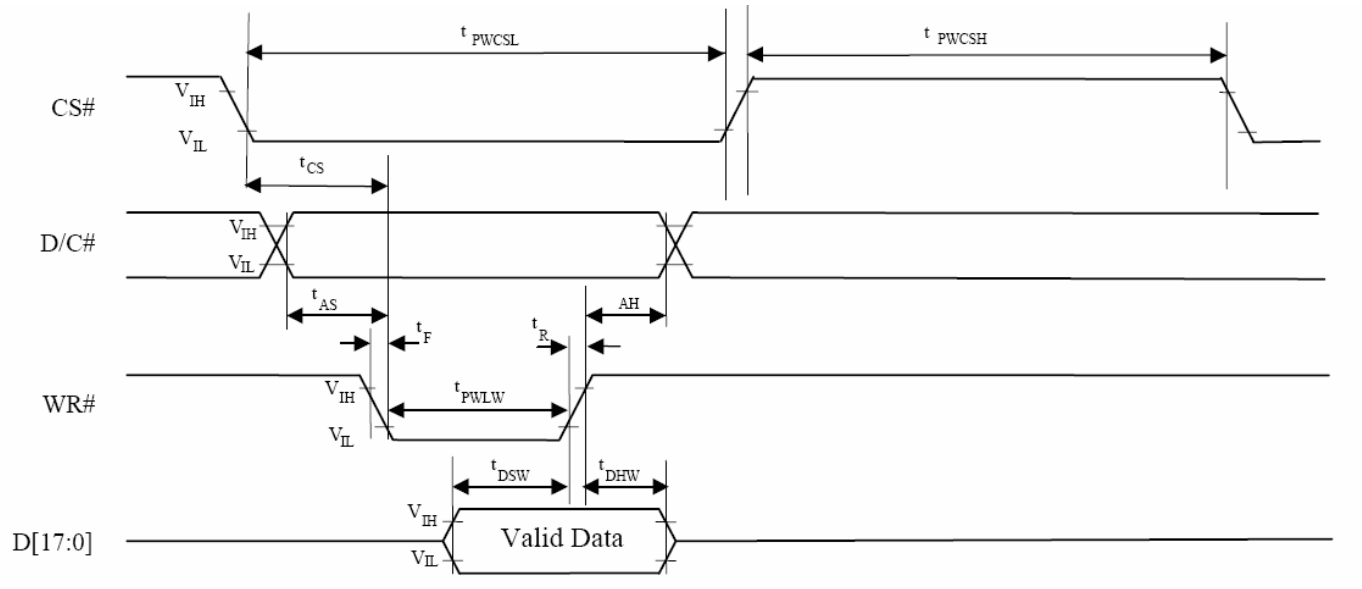
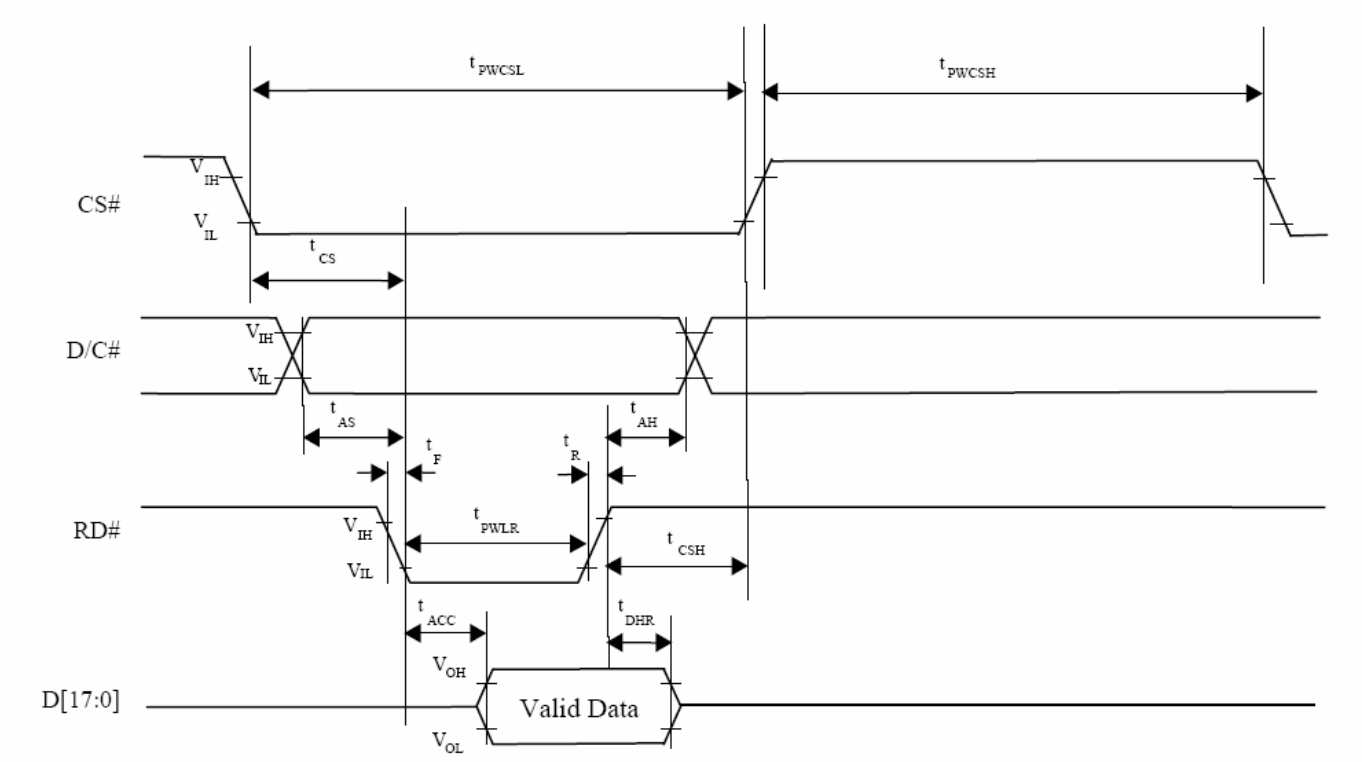


Figure 7-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)



8. Data transfer order Setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 8-1: Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd																G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

9 Register Depiction

Please consult the spec of SSD1963 Version 1.2

10. OPTICAL CHARATERISTIC

Ta=25±2℃, ILED=20mA

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr	θ =0° 、Φ=0°	-	10		ms	Note 3,5
		Tf		-	15		ms	
Contrast ratio		CR	At optimized viewing angle	300	400	-	-	Note 4,5
Color Chromaticity	White	Wx	θ =0° 、Φ=0	(0.26)	(0.31)	(0.36)		Note 2,6,7
		Wy		(0.28)	(0.33)	(0.38)		
	Red	Rx	θ =0° 、Φ=0					
		Ry						
	Green	Gx	θ =0° 、Φ=0					
		Gy						
	Blue	Bx	θ =0° 、Φ=0					
		By						
Viewing angle	Hor.	ΘR	CR≧10	(50)	(60)		Deg.	Note 1
		ΘL		(50)	(60)			
	Ver.	ΦT		(40)	(50)			
		ΦB		(45)	(55)			
Brightness		-	-	200	250	-	cd/m^2	Center of display

Ta=25±2℃, I_L=20mA

Note 1: Definition of viewing angle range

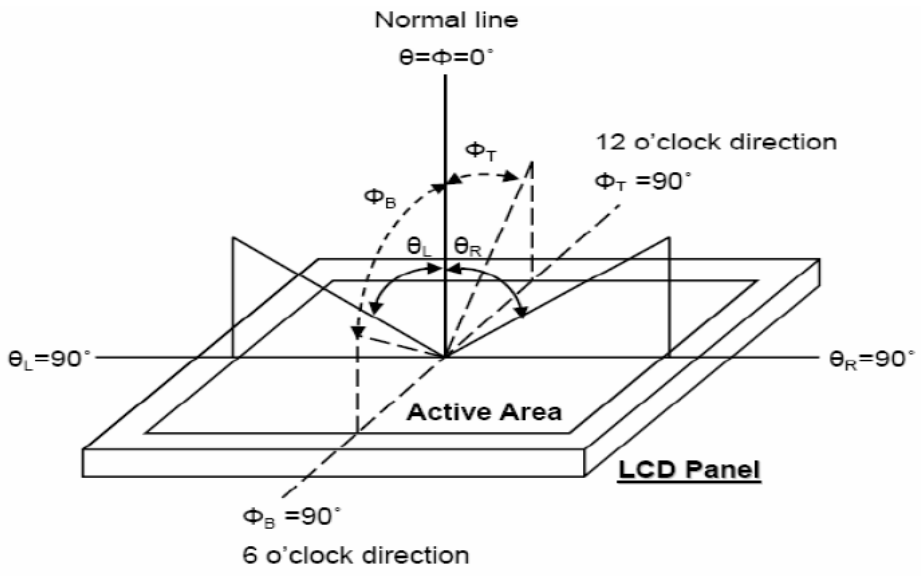


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

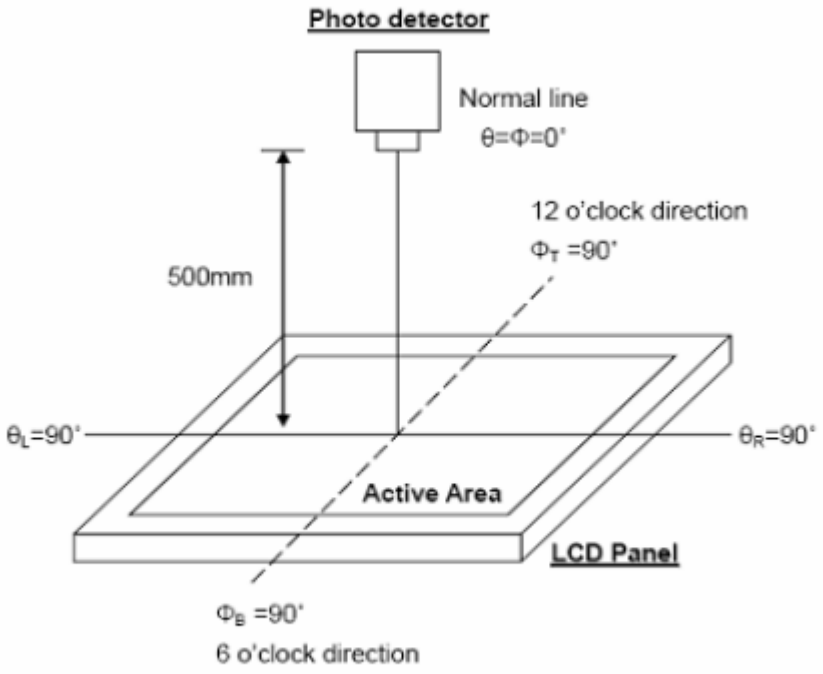


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90% to 10% . And fall time, Tf, is the time between photo detector output intensity changed from10% to 90% .

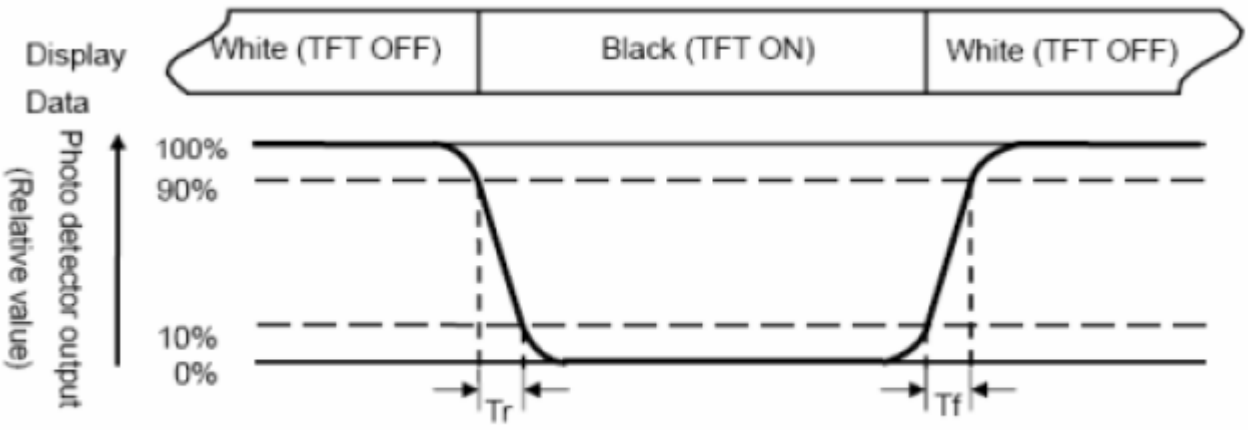


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

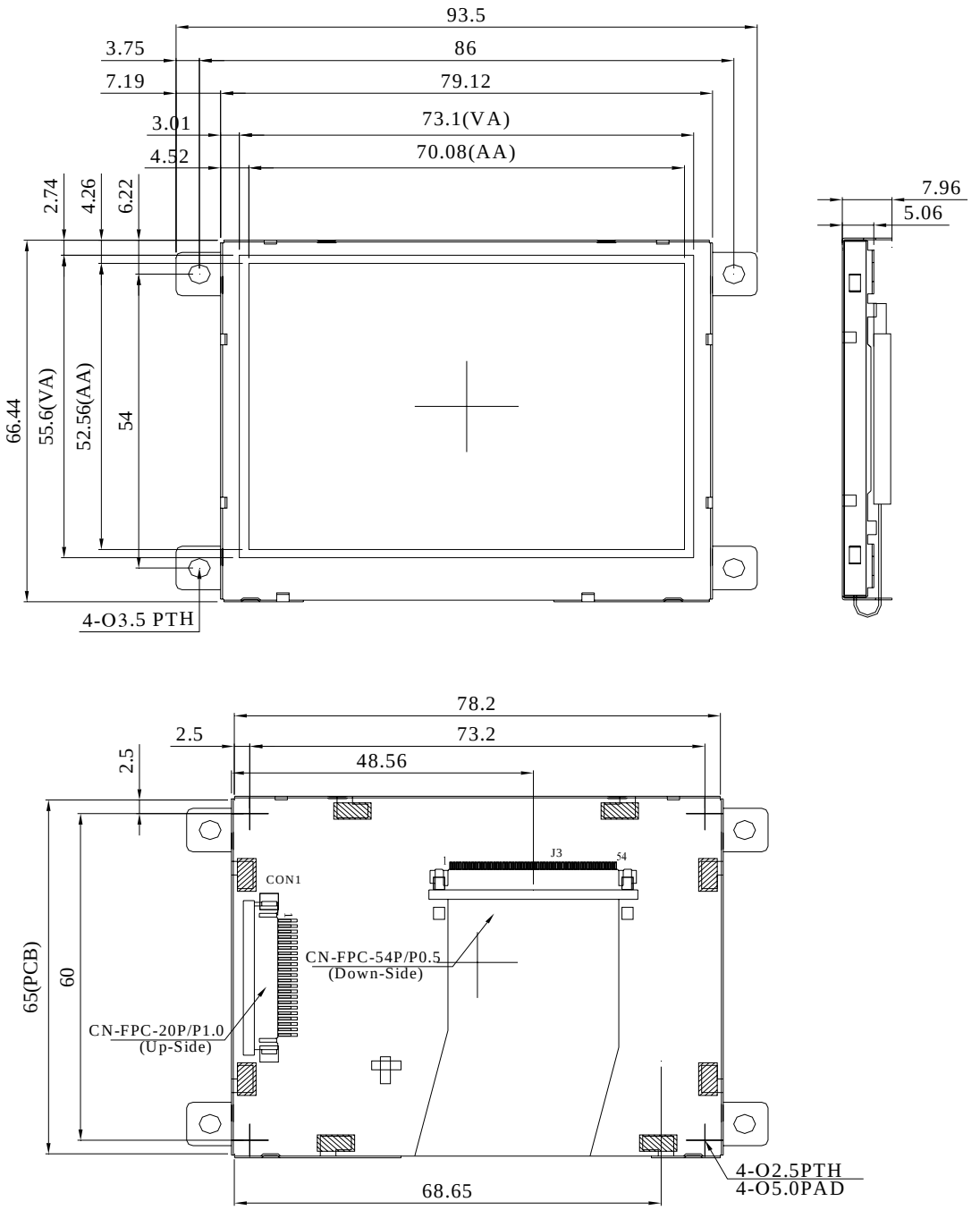
Note 5: White Vi = Vi50 ± 1.5V
Black Vi = Vi50 ± 2.0V
“±” means that the analog input signal swings in phase with VCOM signal.
“±” means that the analog input signal swings out of phase with VCOM signal.
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

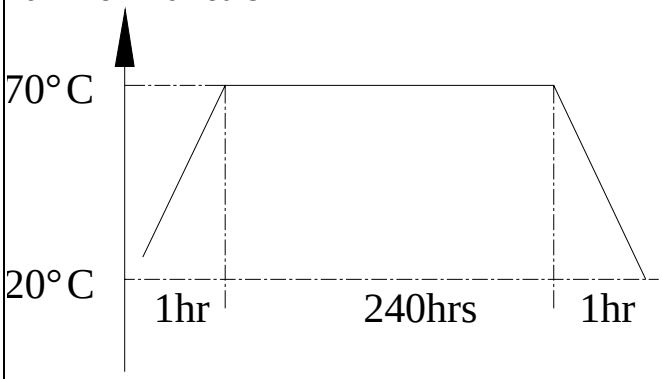
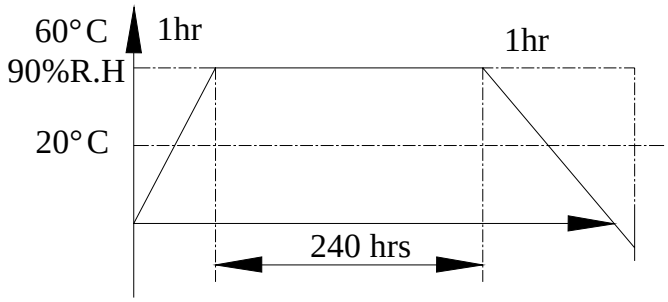
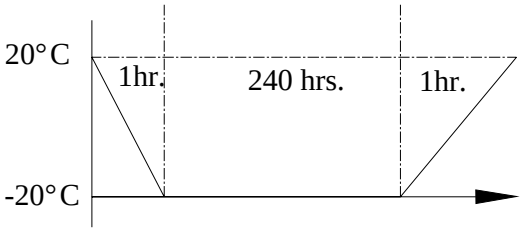
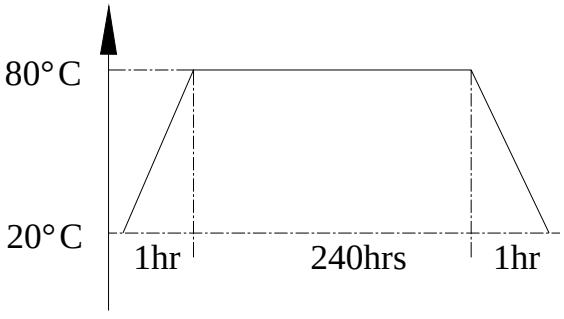
11.Contour Drawing

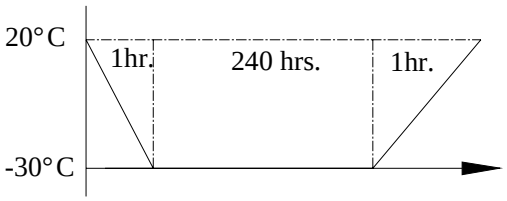
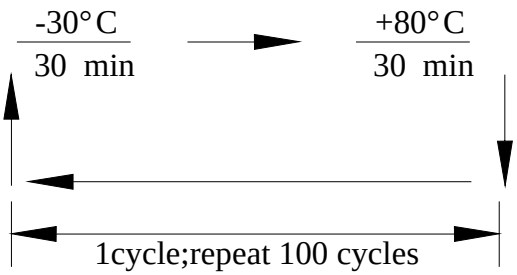
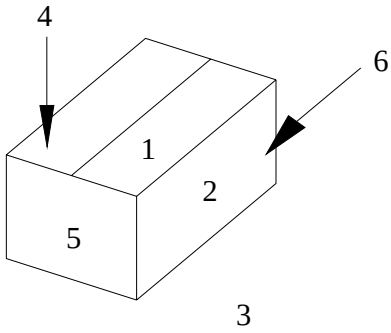


CON1

PIN NO.	SYMBOL
1	VSS
2	VCC
3	BL_E
4	RS
5	WR
6	RD
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	CS
16	RES
17	NC
18	FGND
19	NC
20	NC

12.Reliability

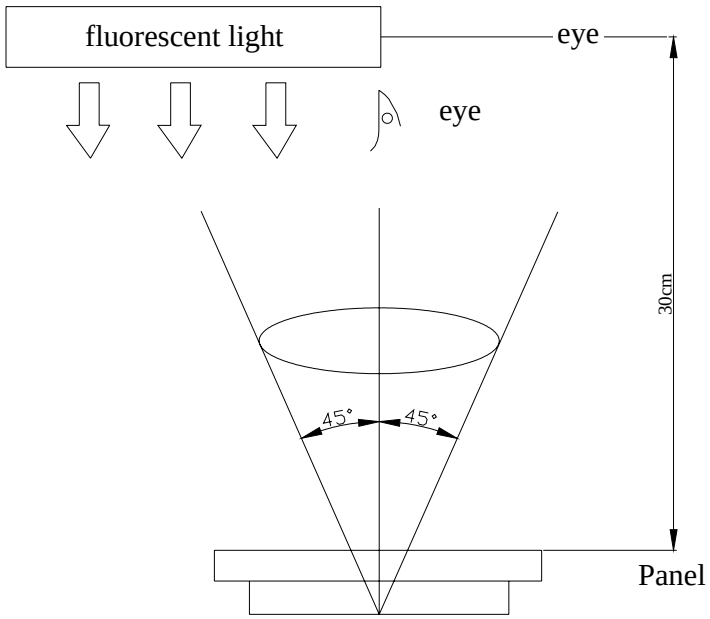
Test Item	Test Condition
High Temperature Operation	70℃ for 240 hours 
High Temperature Operation Humidity Operation	60℃,90%RH for 240 hours 
Low Temperature Operation	-20℃ for 240hours 
High Temperature Storage	80℃ for 240 hours 

Test Item	Test Condition
Low Temperature Storage	-30℃ for 240 hours 
Thermal Shock	-30℃（30min）~+80℃(30min) for 100 cycles 
Electrostatic Discharge (Not operation)	Discharge Resistance : 330Ω Energy Storage Capacitor : 150pF Output voltage (1)Contact Discharge ±4KV (2)Air Discharge ±8KV Polarity of the output voltage : positive and negative Discharge times : 5times
Package Vibration	Frequency(Random Wave)・10HZ~55HZ~10HZ Amplitude : p-p max/2.94m/s² max Orientation : X， Y ， Z (3axis) Test Time : 1 hr. each axis ,total 3 hrs
Package Drop Test	100cm height natural falling Drop sequence : 1 corner,3 edges,and 6 faces,total 10 times  1)corner2-3-5 2)edge2-5 3)edge2-3 4)edge3-5 5)face5 6)face6 7)face2 8)face4 9)face3 10)face1

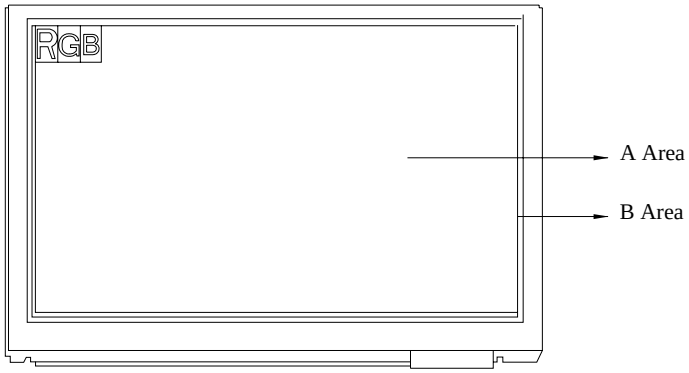
13. Cosmetic Criteria of LCD Screen

13.1 Inspection Condition

- Sample Plan:MIL-STD-105E LEVEL: II
  AQL: Major (MA):0.65%/Minor(MI):1.5%
- Cosmetic inspect 300～500Lux fluorescent light, leaving 30～35cm between panels and eyes , and between panels and lights.
- Functional in spec under 200 Lux .
- Inspection condition is 23±5℃,50±20%RH maximum.



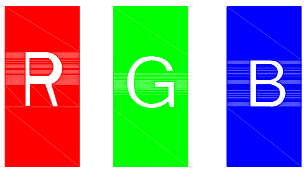
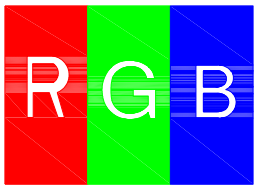
·Definition of area

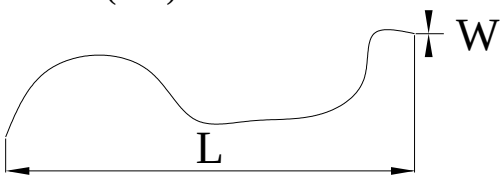


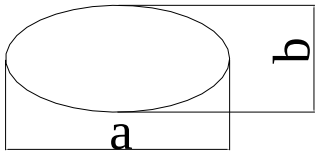
A Area: Viewing area.

B Area: Out of viewing.(Don’t care cosmetic in outside viewing area)

13.2 Inspection specification

NO	Item	Acceptable specification	Judgment Criterion
1	Electrical Testing (MA)	**1-1 sub pixel classification** ● sub pixel: Number of sub pixel doesn't exceed Five dot.  Sub Pixel(Dot) a>Dark dot ----Four Allowed b>Bright dot---one Allowed c>The definition of dot ----The size of a defective dot over 1/2 of whole dot is regarded as one defective dot. d> Dark sub pixel: The distance more than 5mm between dot and dot. e>Bright sub pixel: The distance more than 20mm between bright dot and bright dot . ● Pixel : Three dots link together-----one allowed.  Pixel 1-2Leakage to light ● Leakage to light be not allowed. 1-3 Picture to shake ● Picture had shake ,twinkle and noise etc. instable of defect that be not allowed. 1-4 Function ● No display or No function is not allowed. ● Source Line, Gate Line is not allowed. ● Contrast Ratio exceeds product specifications. ● Current consumption exceeds product specifications. ● Display malfunction.	N≤4 N≤1 N≤1 N=0 N=0 N=0
02	Mechanical Dimension(MA)	2.1 Mechanical Dimension exceeds product specifications. 2-2 Out of frame and boss of plastic changed shape that be not allowed.	N=0

<table>
<tr><th>NO</th><th>Item</th><th>Acceptable specification</th><th>Judgment Criterion</th></tr>
<tr><td>3</td><td>Cosmetic Inspection(MA)</td><td>
3-1 Fiber / Line shapes of defect
<table>
<tr><th>Length</th><th>Width</th><th>Acceptable number</th><th>Mini. space</th><th>Acceptable number</th></tr>
<tr><td>----</td><td>W≦0.05</td><td>Ignore</td><td rowspan="2">5mm</td><td>Ignore</td></tr>
<tr><td>L≦3</td><td>0.05<W≦0.1</td><td>3</td><td>3</td></tr>
<tr><td>----</td><td>W>0.1</td><td>Not allowed</td><td rowspan="2">---</td><td>Not allowed</td></tr>
<tr><td>L>3</td><td>----</td><td>Not allowed</td><td>Not allowed</td></tr>
</table>
L: length(mm)
W: width(mm)


3-2 Blemish: dot shapes of defect.
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Mini. space</th></tr>
<tr><td>Φ≦0.2</td><td>Ignore</td><td>---</td></tr>
<tr><td>0.2<Φ≦0.3</td><td>3</td><td>5mm</td></tr>
<tr><td>Φ>0.3</td><td>0</td><td>----</td></tr>
</table>
3-3 Bubble
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Mini. space</th></tr>
<tr><td>Φ≦0.20</td><td>Ignore</td><td>---</td></tr>
<tr><td>0.2<Φ≦0.3</td><td>3</td><td>15mm</td></tr>
<tr><td>Φ>0.3</td><td>0</td><td>----</td></tr>
</table>
Foreign Substances


Φ=（a+ b）/2
</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Acceptable specification</th><th>Judgment Criterion</th></tr>
<tr><td>3</td><td>Cosmetic Inspection(MA)</td><td>3-4 Scratch
● Impassive scratch as below.
<table><tr><th>Length</th><th>Width</th><th>Acceptable number</th><th>Mini. space</th></tr><tr><td>----</td><td>W≦0.05</td><td>lgnore</td><td rowspan="2">5mm</td></tr><tr><td>L≦3</td><td>0.05<W≦0.1</td><td>3</td></tr><tr><td>----</td><td>W>0.1</td><td>Not allowed</td><td rowspan="2">---</td></tr><tr><td>L>3</td><td>----</td><td>Not allowed</td></tr></table>
3-5 Newton Ring
● D≦8mm----allowed
● D≧8mm----NG</td><td></td></tr>
<tr><td>4</td><td>Crack/Break(MA)</td><td>Not Allowed.</td><td>N=0</td></tr>
<tr><td>5</td><td>Package (MI)</td><td>5-1 Mixed product types
5-2 Shipping q’ ty should be the same as “shipping notice form” q’ ty.
5-3 Outer box can’ t broken .</td><td>N=0</td></tr>
</table>