# 64Mb H-die SDRAM Specification 54 TSOP-II with Pb-Free (RoHS compliant)

Revision 1.3 August 2004

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Rev. 1.3 August 2004

### **Revision History**

Revision 1.0 (September, 2003)

Finalized

Revision 1.1 (October, 2003) Deleted speed -7C and AC parameter notes 5.

### Revision 1.2 (May, 2004)

Added Note 5. sentense of tRDL parameter

Revision 1.3 (August, 2004) • Corrected typo.



### 4M x 4Bit x 4 / 2M x 8Bit x 4 / 1M x 16Bit x 4 Banks Synchronous DRAM

### FEATURES

- JEDEC standard 3.3V power supply
- $\bullet$  LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM (x4,x8) & L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)
- Pb-free Package
- RoHS compliant

### **GENERAL DESCRIPTION**

The K4S640432H / K4S640832H / K4S641632H is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 4 bits, / 4 x 2,097,152 words by 8 bits, / 4 x 1,048,576 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### **Ordering Information**

Part No.	Orgainization	Max Freq.	Interface	Package	
K4S640432H-UC(L)75	16Mb x 4	133MHz(CL=3)			
K4S640832H-UC(L)75	8Mb x 8	133MHz(CL=3)			
K4S641632H-UC(L)60		166MHz(CL=3)	LVIIL	54pin TSOP(II)	
K4S641632H-UC(L)70	4Mb x 16	143MHz(CL=3)			
K4S641632H-UC(L)75		133MHz(CL=3)	]		

Organization	Row Address	Column Address
16Mx4	A0~A11	A0-A9
8Mx8	A0~A11	A0-A8
4Mx16	A0~A11	A0-A7

### Row & Column address configuration



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### Package Physical Dimension



54Pin TSOP(II) Package Dimension



## **CMOS SDRAM**

### FUNCTIONAL BLOCK DIAGRAM



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### **PIN CONFIGURATION** (Top view)

x16	x8	x4			x4	<b>x</b> 8	x16	
VDD	VDD	VDD		54	Vss	Vss	Vss	
DQ0	DQ0	N.C		53	N.C	DQ7	DQ15	
VDDQ	VDDQ	VDDQ	<b>D</b> 3	52 🗖	Vssq	VSSQ	VSSQ	
DQ1	N.C	N.C	<b>4</b>	51 🗖	N.C	N.C	DQ14	
DQ2	DQ1	DQ0	<b>5</b>	50 Þ	DQ3	DQ6	DQ13	
Vssq	VSSQ	VSSQ	<b>6</b>	49 🗖	VDDQ	VDDQ	VDDQ	
DQ3	N.C	N.C	<b>d</b> 7	48 🗖	N.C	N.C	DQ12	
DQ4	DQ2	N.C	<b>B</b>	47 🗖	N.C	DQ5	DQ11	
VDDQ	VDDQ	VDDQ	<b>9</b>	46 🗖	Vssq	Vssq	VSSQ	
DQ5	N.C	N.C	<b>d</b> 10	45 🗖	N.C	N.C	DQ10	
DQ6	DQ3	DQ1	<b>d</b> 11	44 🗖	DQ2	DQ4	DQ9	
Vssq	VSSQ	VSSQ	<b>d</b> 12	43 🗖	VDDQ	VDDQ	VDDQ	
DQ7	N.C	N.C	<b>1</b> 3	42 🗖	N.C	N.C	DQ8	
VDD	VDD	VDD	<b>a</b> 14	41 🗖	Vss	Vss	Vss	
LD <u>QM</u>	N.C	<u>N.C</u>	<b>1</b> 5	40 🗖	N.C/RFU	N.C/RFU	N.C/RFU	
WE	WE	WE	<b>□</b> 16	39 🗖	DQM	DQM	UDQM	
CAS	CAS	CAS	<b>D</b> 17	38 🗖	CLK	CLK	CLK	
R <u>AS</u>	R <u>AS</u>	R <u>AS</u>	<b>a</b> 18	37 🗖	CKE	CKE	CKE	
CS	CS	CS	<b>□</b> 19	36 🗖	N.C	N.C	N.C	
BA0	BA0	BA0	□ 20	35 🗖	A11	A11	A11	
BA1	BA1	BA1	<b>a</b> 21	34 🗖	A9	A9	A9	
A10/AP	A10/AP	A10/AP	<b>2</b> 2	33 🗖	A8	A8	A8	
A0	A0	A0	<b>2</b> 3	32 🗖	A7	A7	A7	
A1	A1	A1	<b>2</b> 4	31 🗖	A6	A6	A6	
A2	A2	A2	<b>2</b> 5	30 🗖	A5	A5	A5	54PIN TSOP (II)
A3	A3	A3	<b>q</b> 26	29 🗖	A4	A4	A4	(400mil x 875mil)
VDD	VDD	VDD	<b>2</b> 7	28	Vss	Vss	Vss	(0.8 mm Pin pitch)

### **PIN FUNCTION DESCRIPTION**

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
CS	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : (x4 : CA0 ~ CA9, x8 : CA0 ~ CA8 , x16 : CA0 ~ CA7)
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
WE	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tsHz after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ X15	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.



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### **CMOS SDRAM**

#### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	Tstg	-55 ~ +150	С
Power dissipation	PD	1	W
Short circuit current	los	50	mA

Note : Permanent device damage may occur if "ASOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

#### DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70 C)

Parameter	Symbol	Min	Тур	Мах	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	Vн	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	VIL	-0.3	0	0.8	V	2
Output logic high voltage	Voh	2.4	-	-	V	Iон = -2mA
Output logic low voltage	Vol	-	-	0.4	V	IOL = 2mA
Input leakage current	lu	-10	-	10	uA	3

**Notes :** 1. VIH (max) = 5.6V AC. The overshoot voltage duration is  $\leq 3$  ns.

2. VIL (min) = -2.0V AC. The undershoot voltage duration is  $\leq$  3ns.

3. Any input  $0V \le VIN \le VDDQ$ .

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

### CAPACITANCE (VDD = 3.3V, TA = 23 C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Мах	Unit	Note
Clock	CCLK	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	СN	2.5	5.0	pF	2
Address	CADD	2.5	5.0	pF	2
DQ0 ~ DQ3	Солт	4.0	6.5	pF	3

Notes: 1. -75 only specify a maximum value of 3.5pF

2. -75 only specify a maximum value of 3.8pF

3. -75 only specify a maximum value of 6.0pF



### DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70 C for x4, x8)

Parameter	Parameter Symbol Test Condition			Version	Unit	Note
Falameter	Symbol	lest condition		75		Note
Operating current (One bank active)	ICC1	Burst length = 1 tRC $\ge$ tRC(min) IO = 0 mA		75	mA	1
Precharge standby current in	ICC2P	CKE ≤ VIL(max), tCC = 10ns		1	mA	
power-down mode	ICC2PS	CKE & CLK $\leq$ V L(max), tCC = $\infty$		1		
Precharge standby current in	ICC2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCC = Input signals are changed one time (	= 10ns during 20ns	15	mA	
non power-down mode	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc Input signals are stable	6	IIIA		
Active standby current in	ICC3P	$CKE \le VIL(max)$ , tCC = 10ns		3	mΔ	
power-down mode	ICC3PS	CKE & CLK $\leq$ V L(max), tCC = $\infty$	3			
Active standby current in	ICC3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCC = Input signals are changed one time of	30	mA		
(One bank active)	ICC3NS	$CKE \ge VIH(min)$ , $CLK \le VIL(max)$ , tcc Input signals are stable	c) = ∞	25		
Operating current (Burst mode)	ICC4	IO = 0 mA Page burst 4Banks Activated tccD = 2CLKs	115	mA	1	
Refresh current	ICC5	tRC ≥ tRC(min)		135	mA	2
Self refresh current	1006	CKE < 0.2V	С	1	mA	3
	1000		L	400	uA	4

Notes: 1. Measured with outputs open.

2. Refresh period is 64ms.

3. K4S6404(08)32H-TC\*\*

4. K4S6404(08)32H-TL\*\*

5. Unless otherwise noted, input swing level is CMOS(V H /VIL=VDDQ/VSSQ)



### DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70 C for x16 only)

Parameter	Symbol	Test Condition		Version			Unit	Note
i didilicici	Symbol	rest condition		60	70	75	Onit	Note
Operating current (One bank active)	ICC1	Burst length = 1 tRC $\ge$ tRC(min) IO = 0 mA		140	115	110	mA	1
Precharge standby current in	ICC2P	CKE ≤ VIL(max), tCC = 10ns			1		mA	
power-down mode	ICC2PS	CKE & CLK $\leq V$ L(max), tCC = $\infty$			1			
Precharge standby current in	ICC2N	CKE $\ge$ VIH(min), $\overline{CS} \ge$ VIH(min), tCC = 10ns Input signals are changed one time during 2	0ns		15		mA	
non power-down mode	ICC2NS	$CKE \ge VIH(min)$ , $CLK \le VIL(max)$ , $tCC = \infty$ Input signals are stable	6			mA		
Active standby current in	ICC3P	CKE ≤ VIL(max), tCC = 10ns		3			m۸	
power-down mode	ICC3PS	CKE & CLK $\leq$ V L(max), tCC = $\infty$	3			IIIA		
Active standby current in	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tCC = 10ns Input signals are changed one time during 20ns			30			
(One bank active)	ICC3NS	$CKE \ge VIH(min)$ , $CLK \le VIL(max)$ , $tCC = \infty$ Input signals are stable			25			
Operating current (Burst mode)	ICC4	IO = 0 mA Page burst 4Banks Activated tccD = 2CLKs	160	140	135	mA	1	
Refresh current	ICC5	tRC≥ tRC(min)	tRC≥ tRC(min)					2
Solf refresh current	locs	CKE < 0.2V	С	1			mA	3
	1000		L	400		uA	4	

Notes: 1. Measured with outputs open.

2. Refresh period is 64ms.

3. K4S641632H-TC\*\*

4. K4S641632H-TL\*\*

5. Unless otherwise noted, input swing level is CMOS(V H /VIL=VDDQ/VSSQ)



### **CMOS SDRAM**

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Vtt = 1.4V

50**Ω** 

30pF

#### AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70 C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	





(Fig. 2) AC output load circuit

 $\overline{TTT}$ 

 $Z0 = 50\Omega$ 

#### **OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

Parameter		Symbol		Version		Unit	Note
raiameter		Symbol	60	70	75		Note
Row active to row active delay		tRRD(min)	12	14	15	ns	1
RAS to CAS delay		tRCD(min)	18	18 20 20		ns	1
Row precharge time		tRP(min)	18	20	20	ns	1
Row active time		tRAS(min)	42	49	45	ns	1
		tRAS(max)		100	us		
Row cycle time		tRC(min)	60	68	65	ns	1
Last data in to row precharge		tRDL(min)		2	CLK	2,5	
Last data in to Active delay		tDAL(min)	2 CLK + tRP			-	5
Last data in to new col. address	s delay	tCDL(min)		1			2
Last data in to burst stop		tBDL(min)		1			2
Col. address to col. address delay		tccd(min)		1			3
Number of valid output data	CAS late	ency = 3		2		0.9	4
	CAS late	ency = 2		1		ea	4

**Notes :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

- 2. Minimum delay is required to complete write.
- 3. All parts allow every cycle column address change.
- 4. In case of row precharge interrupt, auto precharge and read burst stop.
- 5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.



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### **CMOS SDRAM**

Para	motor	Symbol	6	60		70		75		Note
Faia	meter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
	CAS latency=3	tee	6	1000	7	1000	7.5	1000	ne	1
CER Cycle unie	CAS latency=2		-	1000	-	1000	10	1000	115	· ·
CLK to valid	CAS latency=3	teac		5		6		5.4	ne	10
output delay	CAS latency=2	ISAC		-		-		6	115	1,2
Output data hold time	CAS latency=3	tou	2.5		3		3		200	2
	CAS latency=2	IOH	-		-		3		115	2
CLK high pulse width		tCH	2.5		3		2.5		ns	3
CLK low pulse width		tCL	2.5		3		2.5		ns	3
Input setup time		tss	1.5		2		1.5		ns	3
Input hold time		tsH	1		1		0.8		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output	CAS latency=3	teuz		5		6		5.4	ne	
in Hi-Z	CAS latency=2	IONZ		-		-		6	115	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Notes: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.

If tr & tf is longer than 1ns, transient time compensation should be considered,

i.e., [(tr + tf)/2-1]ns should be added to the parameter.

#### DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition Min Typ Max Unit		Notes			
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

Notes : 1. Rise time specification based on 0pF + 50  $\Omega$  to Vss, use these values to design to.

2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.

3. Measured into 50pF only, use these values to characterize to.

4. All measurements done with respect to Vss.



### **IBIS SPECIFICATION**

#### Iон Characteristics (Pull-up)

Voltago	133MHz	133MHz			
vollage	Min	Max			
(V)	I (mA)	I (mA)			
3.45	-	-1.68			
3.30	-	-19.11			
3.00	-0.35	-51.87			
2.70	-3.75	-90.44			
2.50	-6.65	-107.31			
1.95	-13.75	-137.9			
1.80	-17.75	-158.34			
1.65	-20.55	-173.6			
1.50	-23.55	-188.79			
1.40	-26.2	-199.01			
1.00	-36.25	-241.15			
0.20	-46.5	-351.68			



oL Characteristics (Pull-down)								
Voltage	133MHz	133MHz						
voltage	Min	Max						
(V)	I (mA)	I (mA)						
3.45	43.92	155.82						
3.30	-	-						
3.00	43.36	153.72						
1.95	41.20	148.40						
1.80	40.56	146.02						
1.65	39.60	141.75						
1.50	38.40	136.08						
1.40	37.28	131.39						
1.00	30.08	105.84						
0.85	26.64	93.66						
0.65	21.52	75.25						
0.40	14.16	49.14						

133MHz Pull-down





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### **CMOS SDRAM**

VDD Clamp @	CLK, CKE, CS, DQM	& DQ
VDD (V)	I (mA)	
0.0	0.0	
0.2	0.0	
0.4	0.0	
0.6	0.0	
0.7	0.0	
0.8	0.0	
0.9	0.0	
1.0	0.23	
1.2	1.34	
1.4	3.02	
1.6	5.06	
1.8	7.35	
2.0	9.83	
2.2	12.48	
2.4	15.30	
2.6	18.31	

Minimum VDD clamp current (Referenced to VDD)

Vss Clamp @ CLK, CKE, CS, DQM & DQ I (mA) Vss(V) -57.23 -2.6 -2.4 -2.2 -45.77 -38.26 -2.0 -31.22 -24.58 -1.8 -1.6 -18.37 -1.4 -12.56 -1.2 -7.57 -1.0 -3.37 -0.9 -1.75 -0.58 -0.8 -0.7 -0.05 -0.6 0.0 0.0 -0.4 -0.2 0.0 0.0 0.0







### SIMPLIFIED TRUTH TABLE

## **CMOS SDRAM**

SIMPLIFIED TRUTH TABLE (V=Valid, X=Don't care, H=Logic high, L=Logic low)													
Command			CKEn-1	CKEn	cs	RAS	CAS	WE	DQM	<b>BA</b> 0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode regist	er set	Н	Х	L	L	L	L	Х	OP code			1,2
Refresh	Auto refresh		ц	Н				ц	v	v			3
	o. #	Entry		L		L	<b>L</b>		^				3
	Self	Exit	L	н	L	Н	Н	Н	х	х			3
					Н	Х	Х	Х					3
Bank active & row	addr.		Н	Х	L	L	Н	Н	Х	V Row address			
Read &	Auto precha	Auto precharge disable		v	-	Ц		ц	v	V	L Column	Column	4
column address	Auto precha	arge enable		^	Ŀ		<b>L</b>	п	~	v	Н	address	4,5
Write &	Auto precha	Auto precharge disable		х	L	Н	L	L	х	V	L	Column address	4
column address	Auto precharge enable									v	Н		4,5
Burst stop		Н	Х	L	Н	Н	L	Х		Х		6	
Bank selection		ion	- н	х	L	L	н	L	x	V	LX		
Treenarge	All banks									Х	H	~	
		Entry	Ц		Н	Х	Х	Х	×				
Clock suspend or active power down		Linuy		L	L	V	V	V	~	Х			
		Exit	L	Н	Х	Х	Х	Х	Х				
Precharge power down mode Exit		Ц		Н	Х	Х	Х	x					
		Linuy		L	L	Н	Н	Н	~	x			
		Evit	L	н	Н	Х	Х	Х	Y				
					L	V	V	V	~				
DQM			Н			Х			V		Х		7
No operation command		н	v	Н	Х	Х	Х	x	x				
			~	L	Н	Н	Н	^					

Notes: 1. OP Code : Operand code

Ao ~ A11 & BAo ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state. A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM. The automatical precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses. If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected. If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected. If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected. If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected. If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at tRP after the end of burst.

- 6. Burst stop command is valid at every burst length.
- 7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

