ISO752xC Low-Power 5 kV_{RMS} Dual-Channel Digital Isolators

1 Features

- Highest Signaling Rate: 1 Mbps
- Propagation Delay Less Than 20 ns
- Low-Power Consumption
- Wide Ambient Temperature: –40°C to 105°C
- 50 kV/μs Transient Immunity Typical
- Operates From 3.3-V or 5-V Supply and Logic Levels
- 3.3-V and 5.0-V Level Translation
- Safety and Regulatory Approvals
  - 6000 V_{PK} Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 4243 V_{RMS} Isolation for 1 Minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1 End Equipment Standards
  - TUV 5000 V_{RMS} Isolation per EN 60950-1 and EN 61010-1
  - CQC Certification per GB4943.1-2011

2 Applications

- Opto-Coupler Replacement in:
  - Industrial Field-Buses
    - ProfiBuses
    - ModBuses
    - DeviceNet™ Data Buses
  - Servo Control Interfaces
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

The ISO7520C and ISO7521C provide galvanic isolation of up to 4243 V_{RMS} for 1 minute per UL and 6000 V_{PK} per VDE. These devices are also certified to 5000 V_{RMS} reinforced insulation per end equipment standards IEC 60950-1, IEC 61010-1, and IEC 60601-1. These digital isolators have two isolated channels with unidirectional (ISO7520C) and bidirectional (ISO7521C) channel configurations. Each isolation channel has a logic input and output buffer separated by a silicon oxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 3.3- and 5-V supplies. All inputs are 5-V tolerant when supplied from 3.3-V supplies.

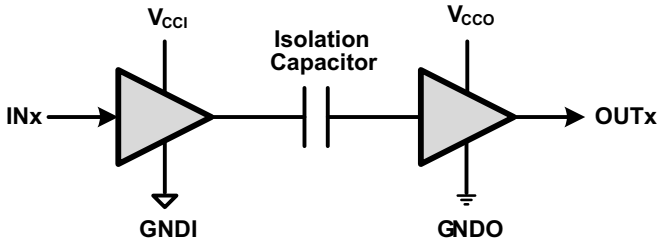
NOTE: The ISO7520C and ISO7521C are specified for signaling rates up to 1 Mbps. Due to their fast response time, these devices will also transmit faster data with much shorter pulse widths. Designers must add external filtering to remove spurious signals with input pulse duration < 20 ns, if desired.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7520C	SOIC (16)	10.30 mm × 7.50 mm
ISO7521C		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 4
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V ± 5% ... 6
6.6 Electrical Characteristics: V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5% ... 6
6.7 Electrical Characteristics: V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5% ... 7
6.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V ± 5% ... 7
6.9 Power Dissipation Characteristics ... 7
6.10 Switching Characteristics: V_{CC1} and V_{CC2} at 5 V ± 5% ... 8
6.11 Switching Characteristics: V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5% ... 8
6.12 Switching Characteristics: V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5% ... 8
6.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V ± 5% ... 9
6.14 Typical Characteristics ... 9
7 Parameter Measurement Information ... 10
8 Detailed Description ... 11
8.1 Overview ... 11
8.2 Functional Block Diagram ... 11
8.3 Feature Description ... 12
8.4 Device Functional Modes ... 14
9 Application and Implementation ... 15
9.1 Application Information ... 15
9.2 Typical Application ... 15
10 Power Supply Recommendations ... 17
11 Layout ... 17
11.1 Layout Guidelines ... 17
11.2 Layout Example ... 17
12 Device and Documentation Support ... 18
12.1 Documentation Support ... 18
12.2 Related Links ... 18
12.3 Community Resources ... 18
12.4 Trademarks ... 18
12.5 Electrostatic Discharge Caution ... 18
12.6 Glossary ... 18
13 Mechanical, Packaging, and Orderable Information ... 18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (November 2011) to Revision D — **Page**

- Deleted Note 1 from the INSULATION CHARACTERISTICS table ... 12
- Changed the REGULATORY INFORMATION table, TUV column From: Certificate Number: U8V 11 08 77311 006 To: Certificate Number: U8V 1309 77311 010 ... 14

Changes from Revision B (June 2011) to Revision C — **Page**

- Changed all the devices numbers by adding a 'C' to the end ... 1
- Changed the Safety and Regulatory Approvals Feature ... 1
- Changed the Description section ... 1
- Changed the IEC 60664-1 Ratings Table ... 12
- Changed the INSULATION CHARACTERISTICS table ... 12

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Changes from Revision A (September 2010) to Revision B **Page**

- Changed 5th Features subbullets ... 1
- Changed the first SWITCHING CHAR table, MAX value, 2nd row from 3.5 to 3.7 and third row from 4 to 4.9 ... 8
- Changed the second SWITCHING CHAR table, MAX value, 2nd row from 4 to 5.6 and third row from 5 to 6.3 ... 8
- Changed the third SWITCHING CHAR table, MAX value, 3rd row from 5 to 8.5 ... 8
- Changed the fourth SWITCHING CHAR table, MAX value, 3rd row from 6 to 6.8 ... 9
- Changed REGULATORY INFORMATION table , from: File Number: pending, to: File Number: E181974 ... 14

Changes from Original (June 2010) to Revision A **Page**

- Added PIN DESCRIPTION table ... 4
- Changed t_{fs} units in Switching Characteristics Table ... 8
- Changed t_{fs} units in Switching Characteristics Table ... 8
- Changed t_{fs} units in Switching Characteristics Table ... 8
- Changed t_{fs} units in Switching Characteristics Table ... 9
- Deleted V_{IORM} test conditions from INSULATION CHARACTERSISTCS table ... 12
- Added V_{PR} parameter and Specifications in INSULATION CHARACTERSISTCS table ... 12
- Changed V_{IOTM} row of the INSULATION CHARACTERISTICS tables ... 12
- Changed V_{ISO} Specifications in INSULATION CHARACTERISTICS table ... 12
- Changed Minimum internal gap limit from 0.016 to 0.014 mm ... 12

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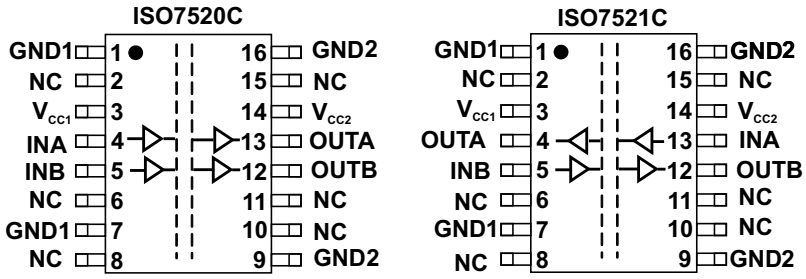
5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO7520C	ISO7521C		
GND1	1, 7	1, 7	—	Ground connection for V_{CC1}
GND2	9, 16	9, 16	—	Ground connection for V_{CC2}
INA	4	13	I	Input, channel A
INB	5	5	I	Input, channel B
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	—	No internal connection
OUTA	13	4	O	Output, channel A
OUTB	12	12	O	Output, channel B
V_{CC1}	3	3	—	Power supply, V_{CC1}
V_{CC2}	14	14	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	–0.5	6	V
V_I	Voltage at INx, OUTx	–0.5	V_{CC} + 0.5(3)	V
I_O	Output Current	–15	15	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage - 3.3-V Operation	3.15	3.3	3.45	V
	Supply voltage - 5-V Operation	4.75	5	5.25	
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level output voltage	2		5.25	V
V_{IL}	Low-level output voltage	0		0.8	V
T_A	Ambient temperature	-40		105	°C
T_J (1)	Junction temperature	–40		136	°C
$1/t_{ui}$	Signaling rate	0		1	Mbps
t_{ui}	Input pulse duration	1			µs

(1) To maintain the recommended operating conditions for T_J, see *Thermal Information*.

6.4 Thermal Information

THERMAL METRIC(1)		ISO7520C, ISO7521C	UNIT
		DW [SOIC]	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V ± 5%

V_{CC1} and V_{CC2} at 5 V ±5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 4		V_{CCO} –0.8 (1)	4.6		V
		I_{OH} = –20 µA; See Figure 4		V_{CCO} –0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 4			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 4			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at V_{CCI} (2)				10	µA
I_{IL}	Low-level input current	INx at 0 V		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; See Figure 6		25	50		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
ISO7520C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		0.4	1	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		3	6	mA
ISO7521C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		2	4	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		2	4	mA

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.
(2) V_{CCI} is the supply voltage, V_{CC1} or V_{CC2}, for the input channel that is being measured.

6.6 Electrical Characteristics: V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%

V_{CC1} at 5 V ±5%, V_{CC2} at 3.3 V ±5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 4	ISO7521C (5-V side)	V_{CCO} –0.8	4.6		V
			ISO7520C/7521C(3.3-V side)	V_{CCO} –0.4	3		
		I_{OH} = –20 µA; See Figure 4		V_{CCO} –0.1	V_{CCO}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 4			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 4			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at V_{CCI}				10	µA
I_{IL}	Low-level input current	INx at 0 V		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; See Figure 6		25	40		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
ISO7520C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		0.4	1	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		2	4.5	mA
ISO7521C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		2	4	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		1.5	3.5	mA

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6.7 Electrical Characteristics: V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%

V_{CC1} at 3.3 V ±5%, V_{CC2} at 5 V ±5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 4	ISO7520C/7521C (5-V side)	V_{CCO} –0.8	4.6		V
			ISO7521C (3.3-V side)	V_{CCO} –0.4	3		
		I_{OH} = –20 µA; See Figure 4		V_{CCO} –0.1	V_{CCO}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 4			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 4			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at V_{CCI}				10	µA
I_{IL}	Low-level input current	INx at 0 V		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; See Figure 6		25	40		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
ISO7520C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		0.2	0.7	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		3	6	mA
ISO7521C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		2	4	mA

6.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V ± 5%

V_{CC1} and V_{CC2} at 3.3 V ±5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 4		V_{CCO} –0.4	3		V
		I_{OH} = –20 µA; See Figure 4		V_{CCO} –0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 4			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 4			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at V_{CCI}					µA
I_{IL}	Low-level input current	INx at 0 V		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; See Figure 6		25	40		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
ISO7520C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		0.2	0.7	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		2	4.5	mA
ISO7521C							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15-pF load		1.5	3.5	mA

6.9 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		ISO7520C, ISO7521C DW [SOIC] 16 PINS	UNIT
P_D	Device power dissipation, V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, C_L = 15 pF, Input a 0.5 MHz 50% duty cycle square wave	42	mW

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6.10 Switching Characteristics: V_{CC1} and V_{CC2} at 5 V ± 5%

V_{CC1} and V_{CC2} at 5 V ±5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 4		9	14	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
t_r	Output signal rise time	See Figure 4		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 5		6		µs

(1) Also known as pulse skew.

6.11 Switching Characteristics: V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%

V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 4		10	17	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.5	5.6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 4		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 5		6		µs

(1) Also known as pulse skew.

6.12 Switching Characteristics: V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%

V_{CC1} at 3.3 V ±5%, V_{CC2} at 5 V ±5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 4		10	17	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 4		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 5		6		µs

(1) Also known as pulse skew.

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6.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V ± 5%

V_{CC1} and V_{CC2} at 3.3 V ±5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 4		12	20	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			1	5	ns
$t_{sk(pp)}$	Part-to-part skew time				6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time				5.5	ns
t_r	Output signal rise time	See Figure 4		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 5		6		µs

(1) Also known as pulse skew.

6.14 Typical Characteristics

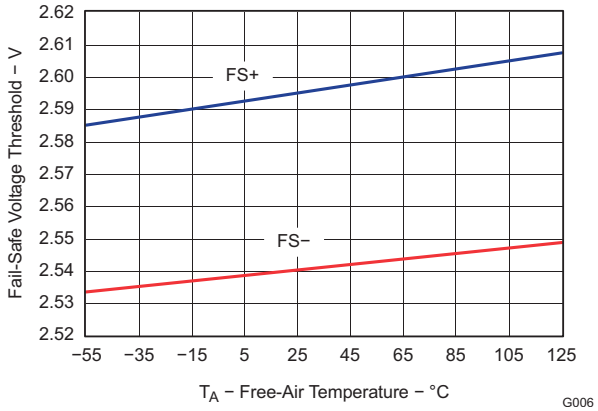


Figure 1. Fail-Safe Voltage Threshold vs Free-Air Temperature

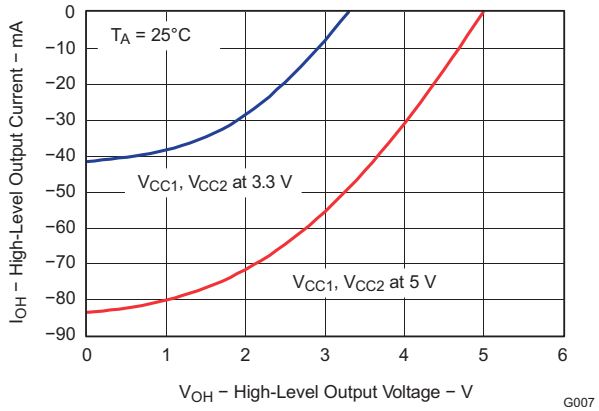


Figure 2. High-Level Output Current vs High-Level Output Voltage

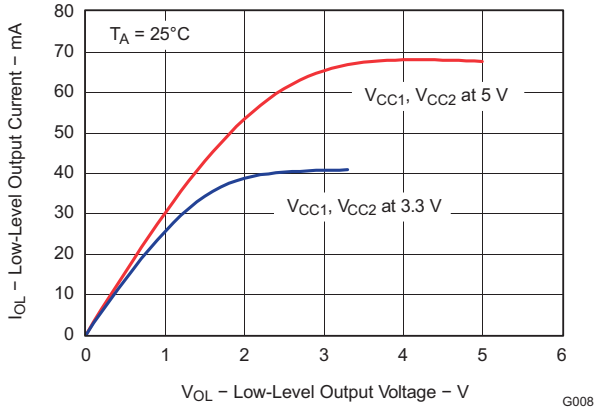
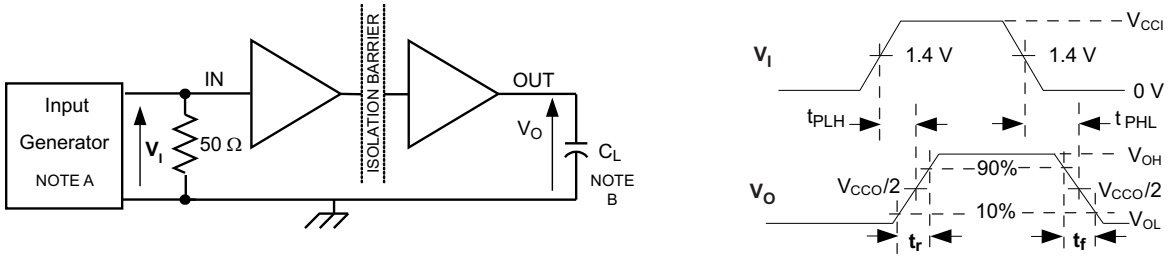


Figure 3. Low-Level Output Current vs Low-Level Output Voltage

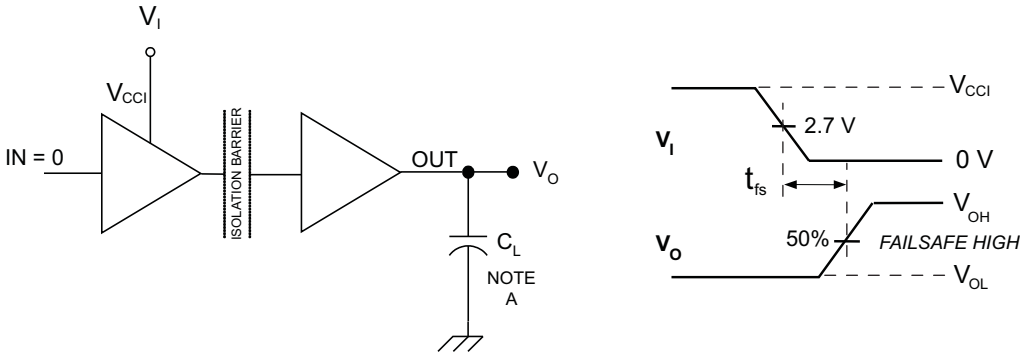
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

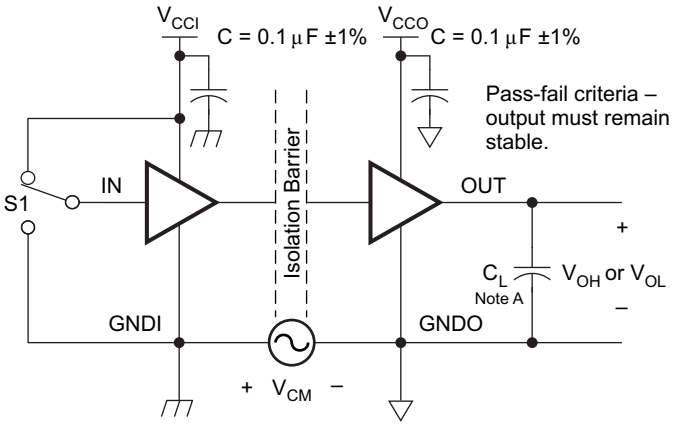
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 5. Fail-safe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6. Common-Mode Transient Immunity Test Circuit

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8 Detailed Description

8.1 Overview

The isolator in Figure 7 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 1 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low frequency channel. Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

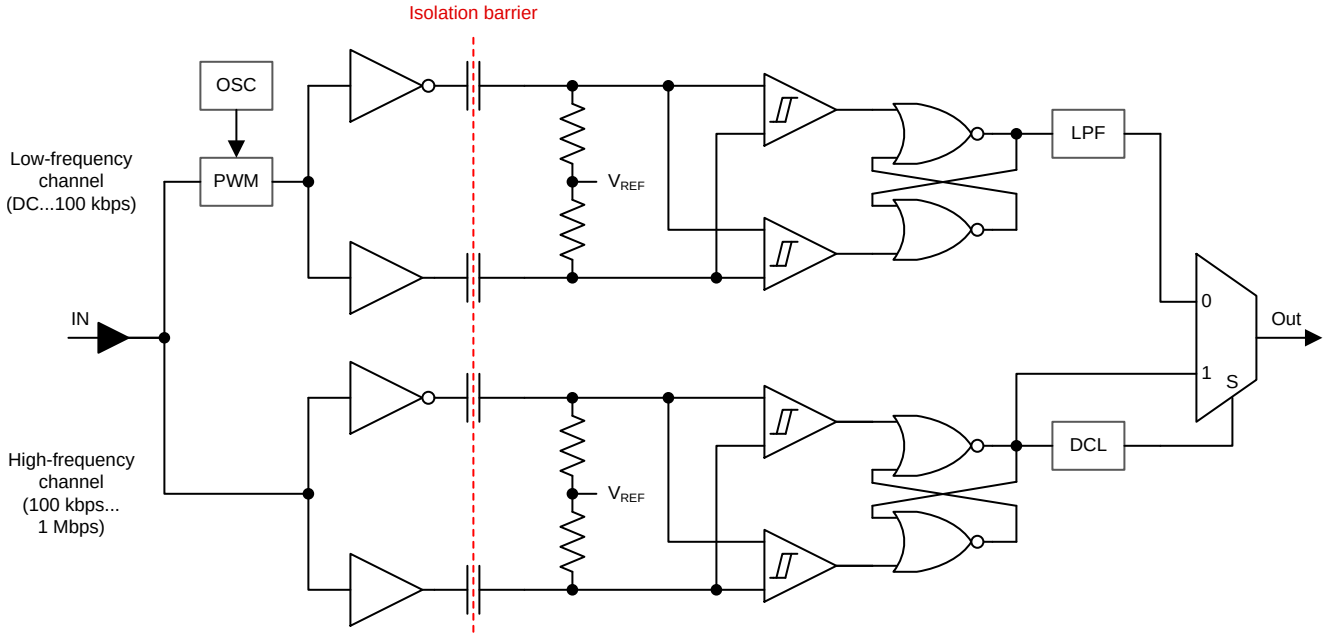

Figure 7. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

8.3.1 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum repetitive peak isolation voltage		1414	V_{PEAK}
V_{PR}	Input to output test voltage	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial discharge < 5 pC	2262	V_{PEAK}
		Method b1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	2651	
		After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	1697	
V_{IOTM}	Maximum Transient Isolation voltage	t = 60 sec (qualification)	6000	V_{PEAK}
V_{ISO}	Withstanding Isolation voltage per UL 1577	$V_{TEST} = V_{ISO}$ = 4243 V_{RMS}, t = 60 sec (qualification); V_{TEST} = 1.2 × V_{ISO} = 5092 V_{RMS}, t = 1 sec (100% production)	4243	V_{RMS}
R_S	Isolation resistance	V_{IO} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	

8.3.2 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation Classification	Rated mains voltages <= 150 Vrms	I - IV
	Rated mains voltages <= 600 Vrms	I - III
	Rated mains voltages <= 1000 Vrms	I - II

8.3.3 Package Insulation and Safety-Related Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
	Minimum internal gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25ºC		$>10^{12}$		Ω
		V_{IO} = 500 V, 100ºC ≤ T_A ≤ T_A max		$>10^{11}$		
C_{IO}	Barrier capacitance input to output(1)	V_{IO} = 0.4 sin(2πft), f = 1 MHz		2		pF
C_I	Input capacitance to ground(2)	$V_I = V_{CC}/2$ + 0.4 sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a 2-terminal device.
(2) Measured from input pin to ground.

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NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance.

Creepage and clearance on a PCB become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current-limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Is	Safety input, output, or supply current	θ_{JA} =79.9°C/W, V_I = 5.25 V, T_J = 150°C, T_A = 25°C			298	mA
		θ_{JA} =79.9°C/W, V_I = 3.45 V, T_J = 150°C, T_A = 25°C			453	
Ts	Maximum Case Temperature				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

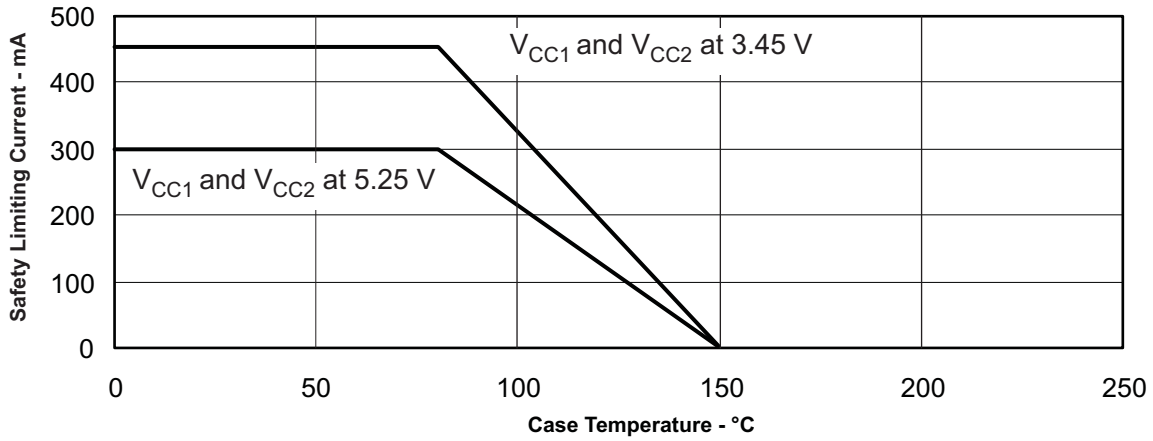

Figure 8. DW-16 $R_{\Theta JC}$ Thermal Derating Curve for VDE

8.3.5 Regulatory Information

VDE	TUV	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Certified according to EN 60950-1 and EN 61010-1	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1	Recognized under 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Basic Insulation Maximum Transient Isolation voltage, 6000 V_{PK} Maximum Repetitive Peak Isolation Voltage, 1414 V_{PK}	5000 V_{RMS} Isolation Rating; Reinforced Insulation, 400 V_{RMS} maximum working voltage; Basic Insulation, 600 V_{RMS} maximum working voltage	5000 V_{RMS} Isolation Rating; Reinforced insulation per CSA 60950-1-07+A1 and IEC 60950-1 2nd Ed.+A1, 380 V_{RMS} max working voltage; Reinforced insulation per CSA 61010-1-04 and IEC 61010-1 2nd Ed, 300 V_{RMS} max working voltage; 2 Means of Patient Protection at 125 V_{RMS} per IEC 60601-1 (3rd Ed.)	Single Protection, 4243 V_{RMS} Withstanding Isolation Voltage	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate Number: 40016131	Certificate Number: U8V 1309 77311 010	Master Contract Number: 220991	File Number: E181974	Certificate Number: CQC14001109542

8.4 Device Functional Modes

Table 1. Device Function Table

V_{CCI} (1)	V_{CCO} (1)	INPUT (INA, INB) (1)	OUTPUT (OUTA, OUTB) (1)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered Up (Vcc ≥ 3.15 V); PD = Powered Down (Vcc ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level

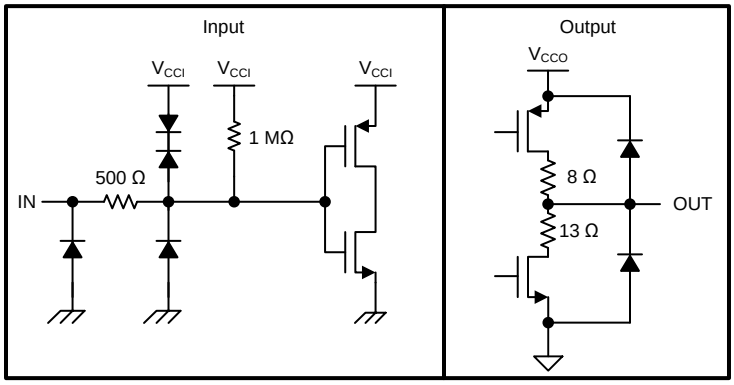

Figure 9. Equivalent Input and Output Schematic Diagrams

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7520C and ISO7521C are high-performance, dual-channel digital isolators with a 5-kV_{RMS} isolation voltage. The isolator uses single-ended TTL-logic switching technology. The supply voltage range is from 3.15 V to 5.25 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7521C can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4- to 20-mA current loop.

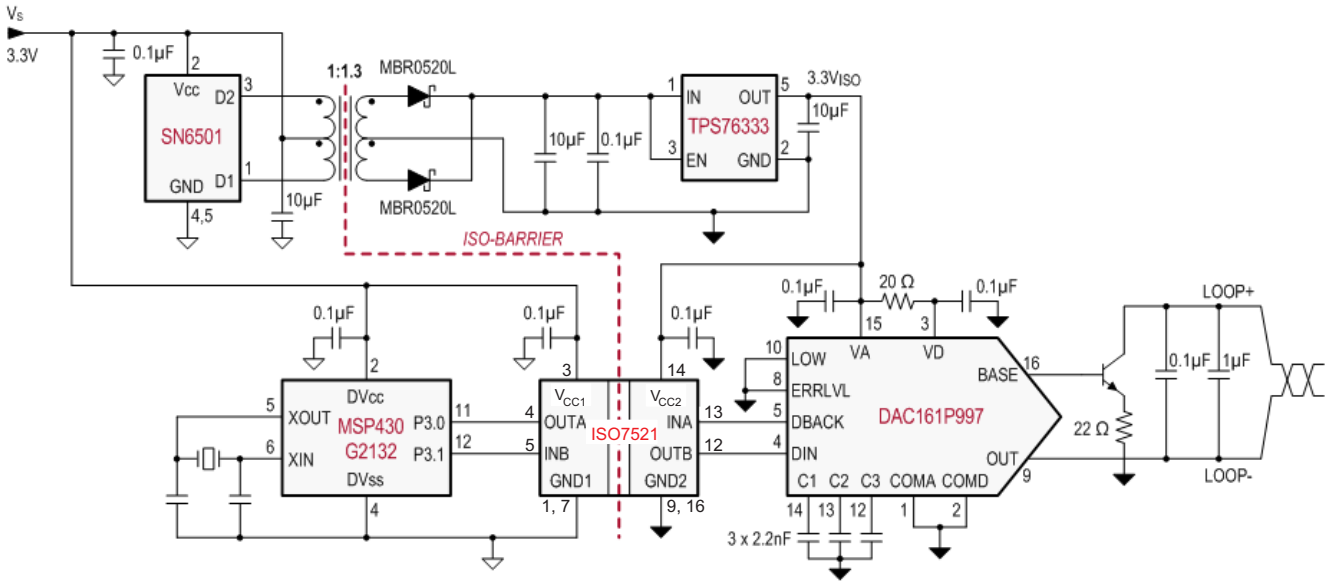

Figure 10. Isolated 4-20 mA Current Loop

9.2.1 Design Requirements

For the ISO7521C, use the parameters shown in Table 2.

Table 2. ISO752xC Design Parameters

PARAMETER	VALUE
Supply voltage	3.15 V to 5.25 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, the ISO7521C only needs two external bypass capacitors to operate.

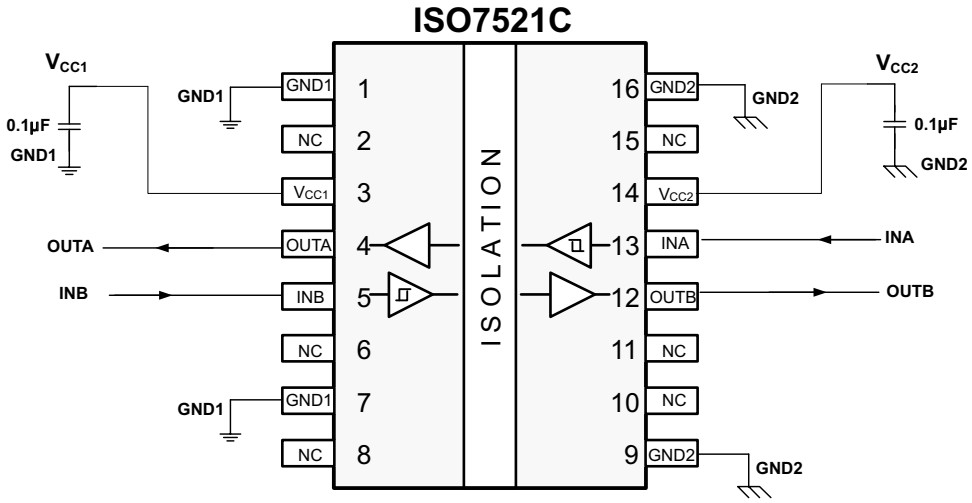

Figure 11. Typical ISO7521C Circuit Hook-up

9.2.3 Application Curve

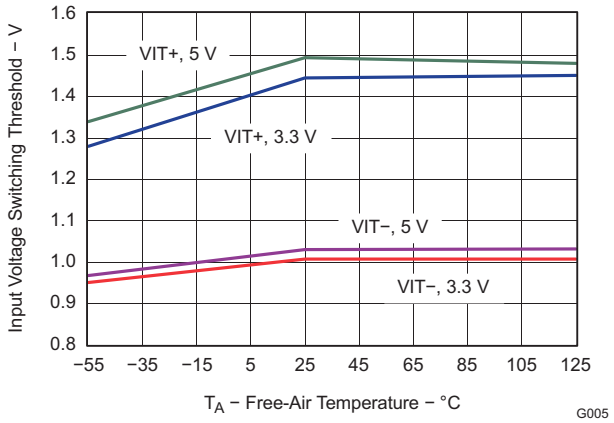

Figure 12. Input Voltage Switching Threshold vs Free-Air Temperature

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10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends placing a 0.1-µF bypass capacitor at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in the SN6501 data sheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 13). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. For detailed layout recommendations, see *Application Note Digital Isolator Design Guide* (SLLA284).

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over less expensive alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability characteristics.

11.2 Layout Example

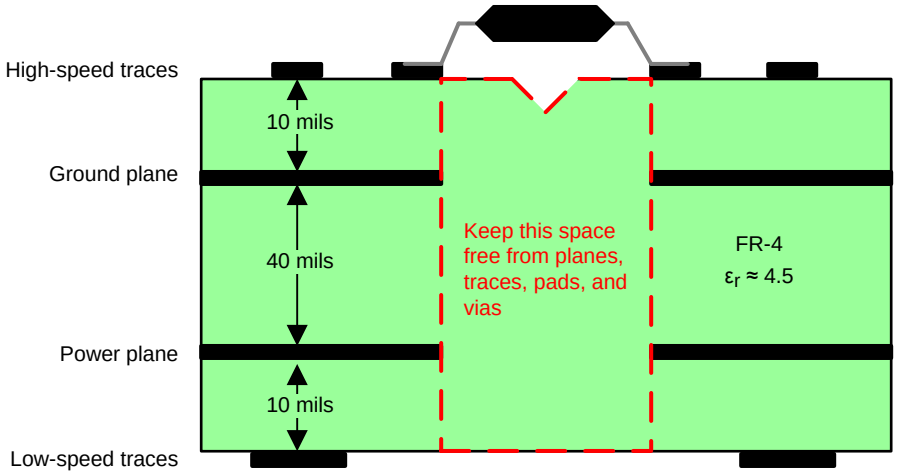

Figure 13. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Application Note Digital Isolator Design Guide (SLLA284)

Isolation Glossary (SLLA353)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7520C	Click here	Click here	Click here	Click here	Click here
ISO7521C	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
DeviceNet is a trademark of Open DeviceNet Vendor Association.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7520CDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW
ISO7520CDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW
ISO7520CDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW
ISO7520CDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW
ISO7520CDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW
ISO7520CDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW
ISO7521CDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW
ISO7521CDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW
ISO7521CDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW
ISO7521CDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW
ISO7521CDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW
ISO7521CDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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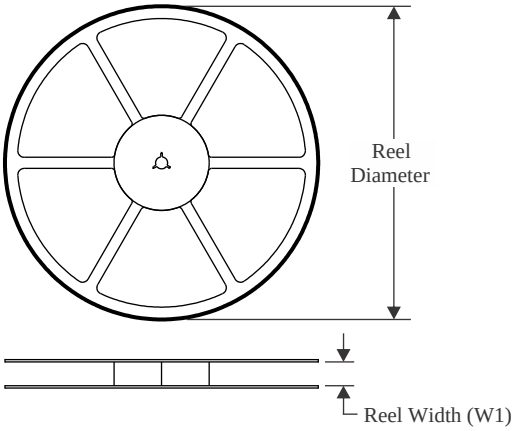
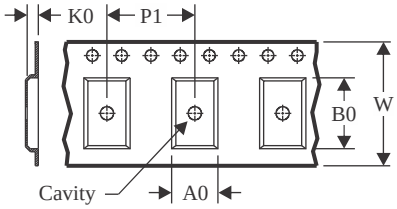
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

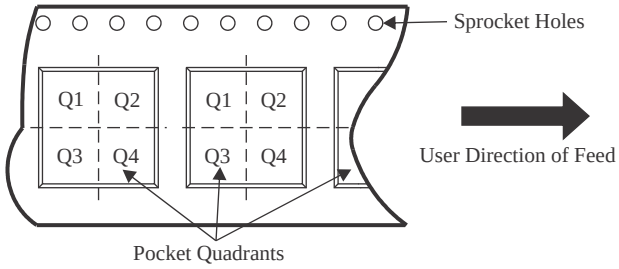


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

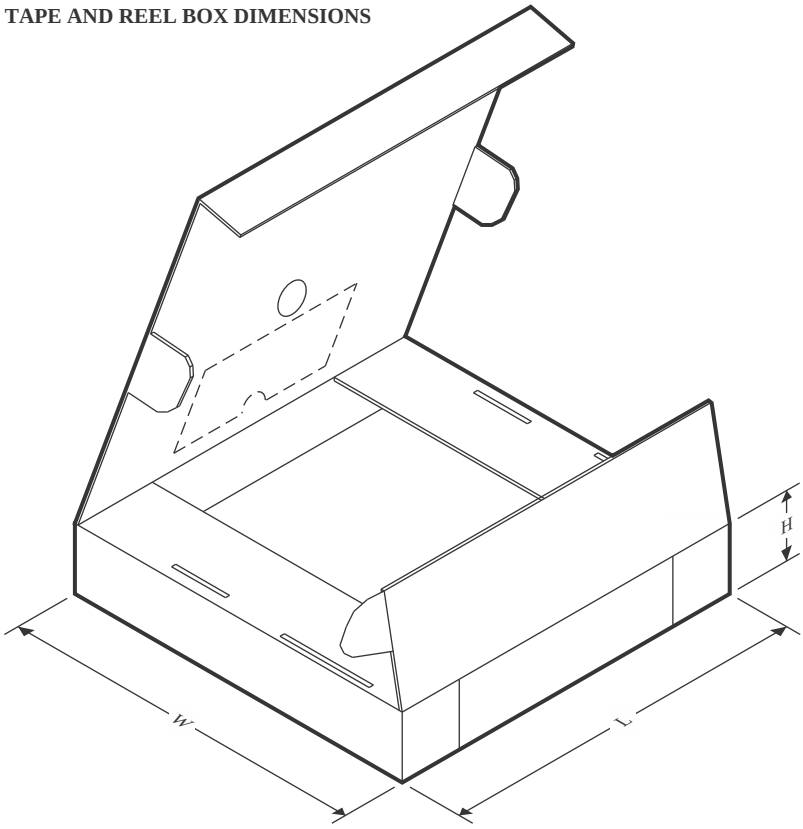
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7520CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7521CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

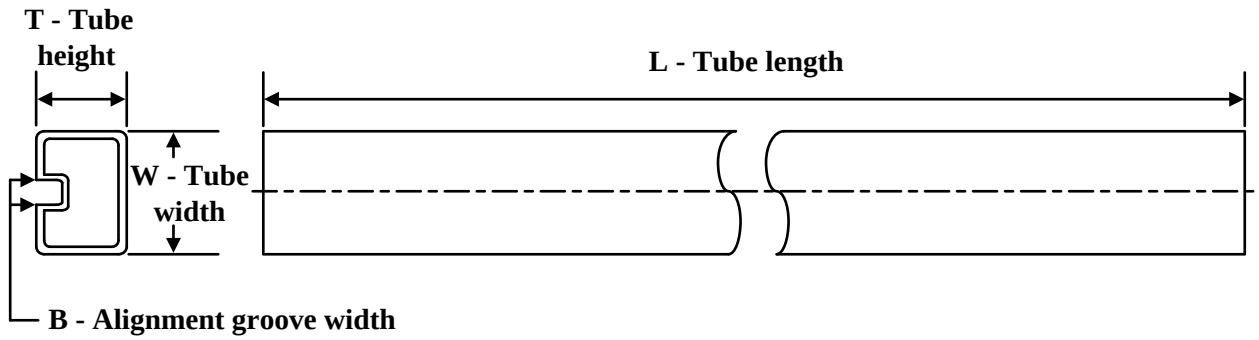
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7520CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7521CDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7520CDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7520CDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7520CDW.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7521CDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7521CDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7521CDW.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

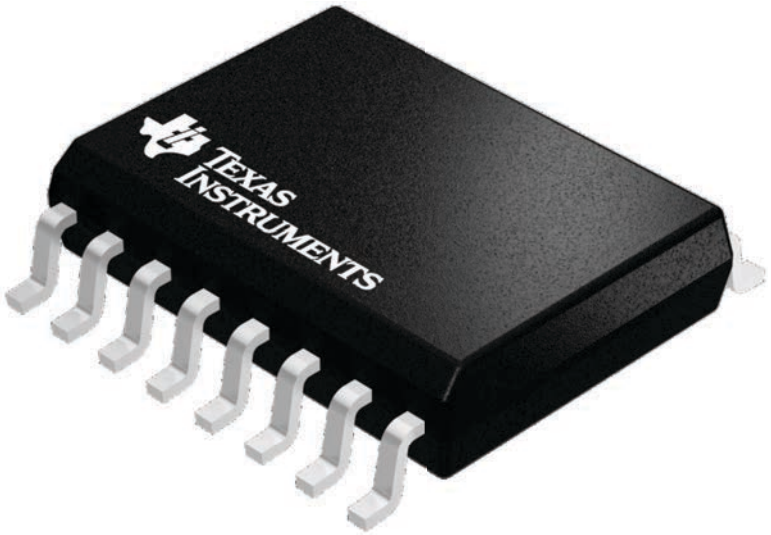
DW 16

SOIC - 2.65 mm max height

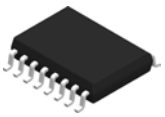
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

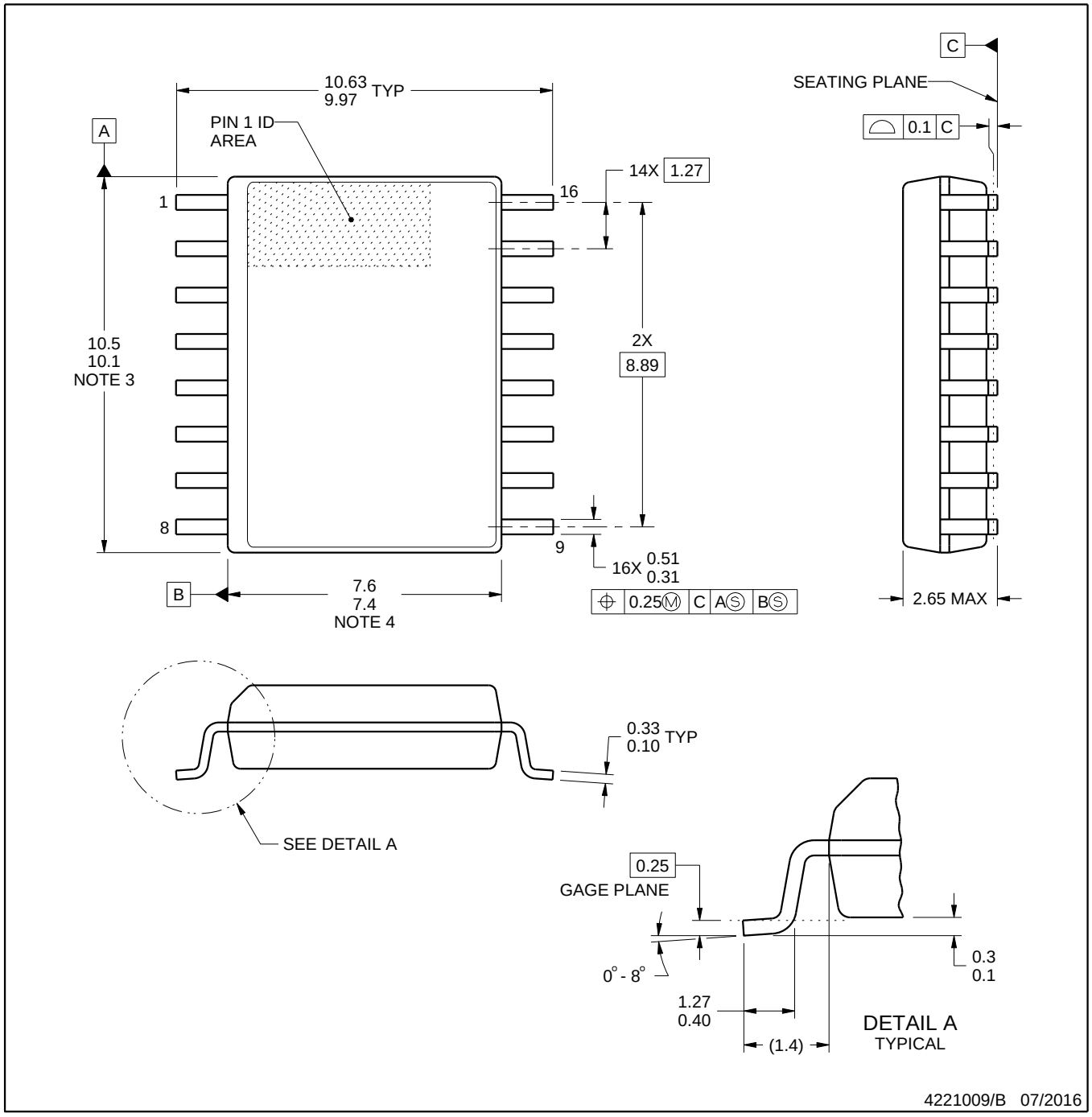


PACKAGE OUTLINE

DW0016B

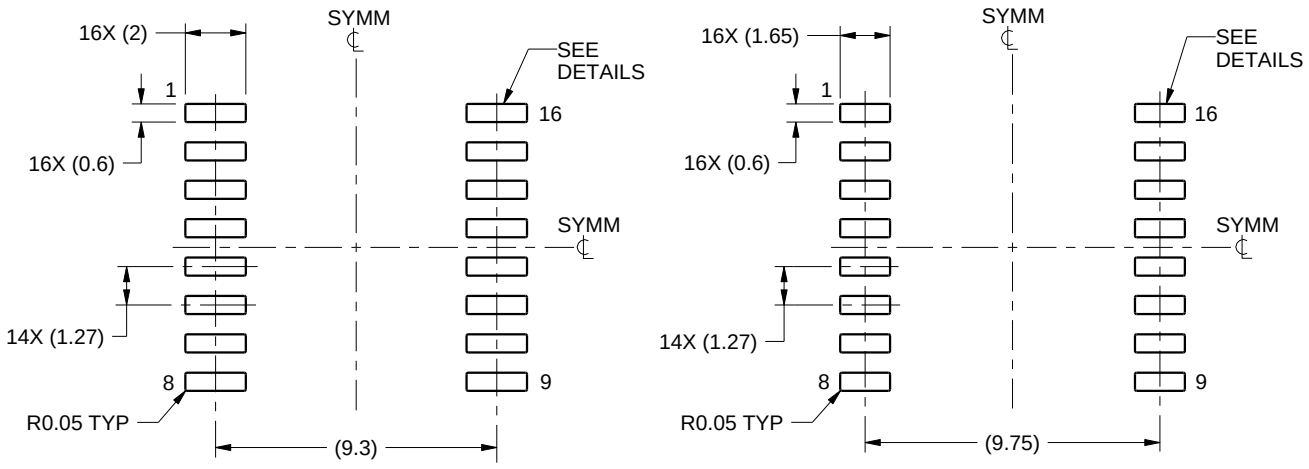
SOIC - 2.65 mm max height

SOIC



NOTES:

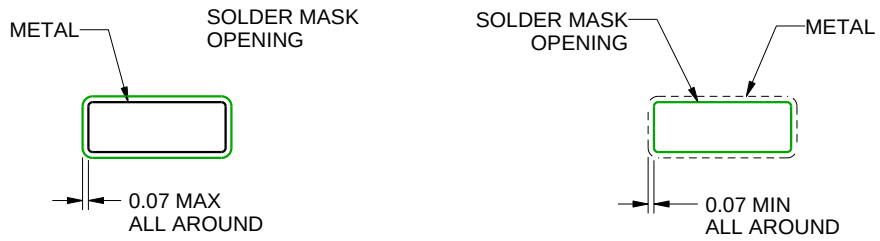
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

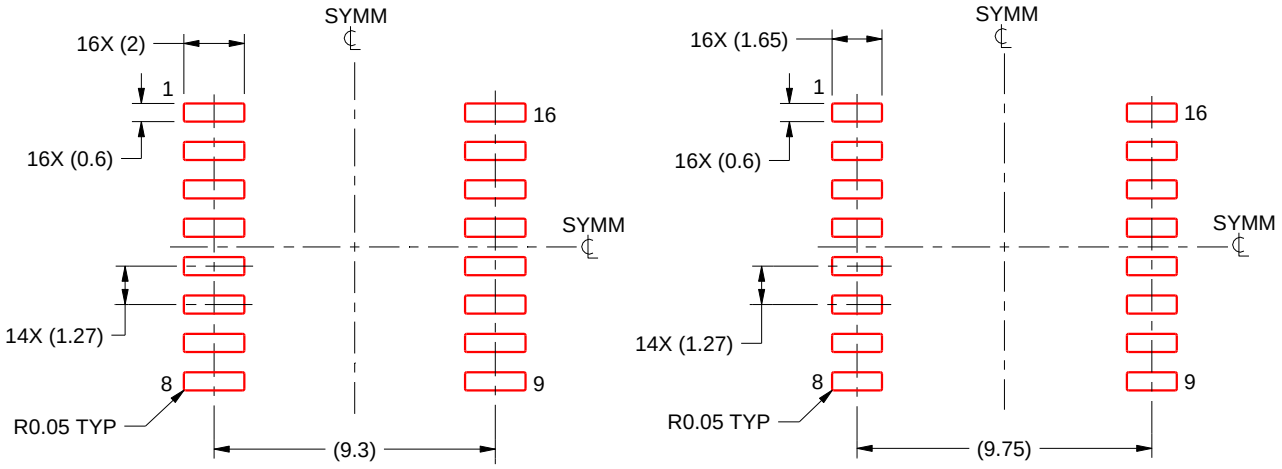
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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