NAU82110
DataSheet

For additional information or questions, please contact: Nuvoton Technology Corporation.
www.nuvoton.com

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1 FEATURE

- Powerful Class-D Amplifier:
  18W Output Power @4Ω, 10% THD+N, 12V Supply
  10W Output Power @8Ω, 10% THD+N, 12V Supply
- 83dB for 217Hz, 79dB for 1kHz, 73dB for 4kHz Power Supply Rejection Ratio (PSRR)
- Low Current Shutdown Mode, less than 10uA
- Click-and-Pop Suppression 30 µVRMS
- I2C Serial Interface
- Gain Selection:
  5 Selectable Gain Settings in Analog mode 0dB / 20dB / 24dB / 32dB / 36dB
  32 Selectable gain settings in I2C mode
- Device Protection:
  Over Current Protection (OCP) (Debugging)
  Over Voltage Protection (OVP)
  Under Voltage Lock Out (UVLO)
  Over Temperature Protection (OTP)
- Speaker Protection:
- Anti-Clip Protection (ACP)
- Filter-less Electro Magnetic Interference (EMI) mitigation
- QFN-20 package
- Package is Halogen-free, RoHS-compliant and TSCA-compliant

Applications

- Automotive Emergency Call (e-Call) Amplifier
- Telematics Systems
- Instrument Cluster Systems

2 GENERAL DESCRIPTION

NAU82110 mono high efficiency filter-free Class-D audio amplifier is capable of driving an 8Ω load with up to 10W output power. The chip features high output power capability, low-current shutdown mode, and click-and-pop suppression. Numerous types of device protection schemes are supported.

NAU82110 is specified for operation from -40℃ ~ +105℃ with QFN-20 package.

3 PART INFORMATION

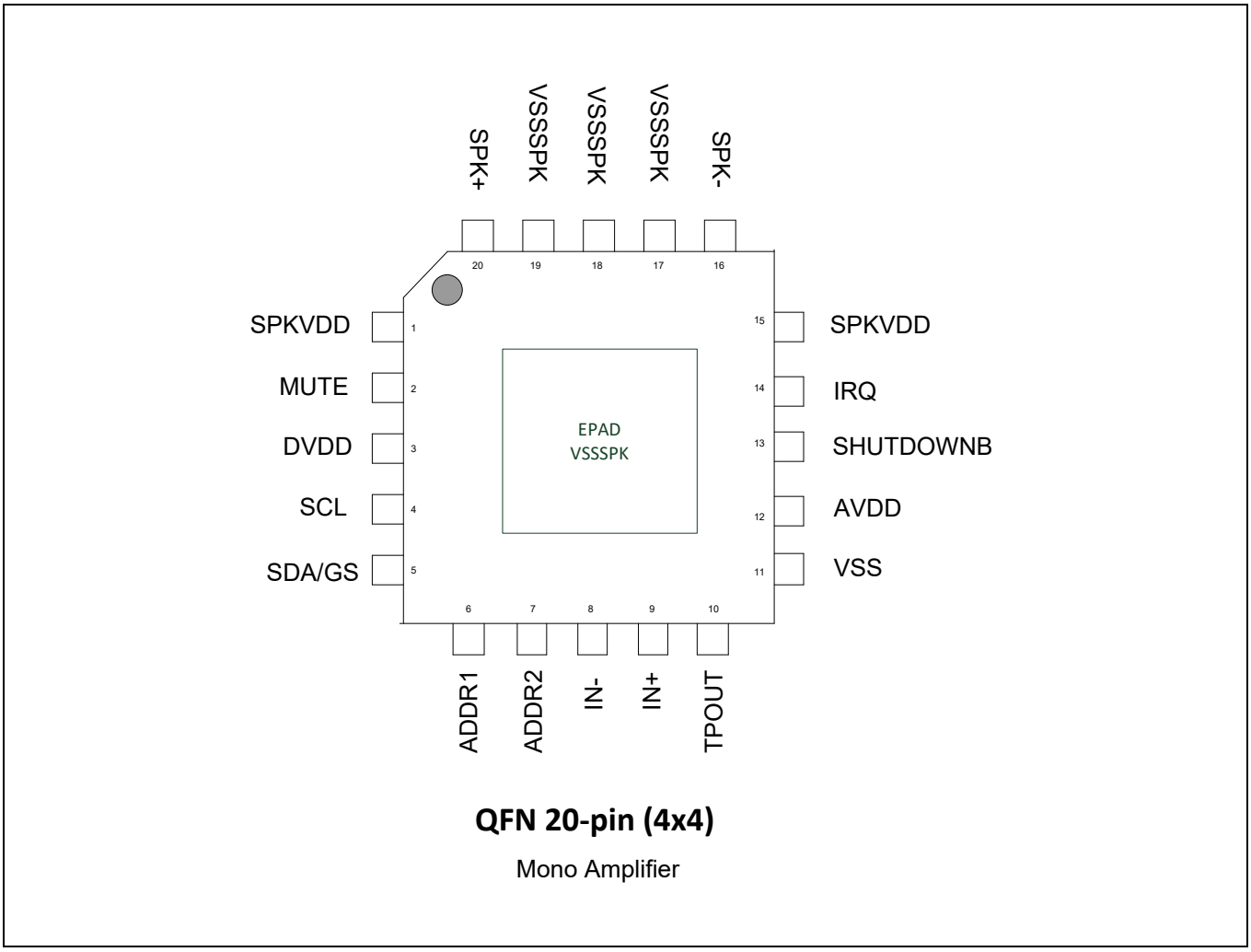


Figure 1 Pin Configuration of QFN 20 pin 4mm x 4mm (TOP VIEW)

Table 1 NAU82110 Pin Description

QFN	Name	Type	Functionality
1	VDDSPK	Supply	Power Supply
2	MUTE	Digital Input	Drive MUTE high to mute inputs
3	DVDD	Digital Supply	Power Supply
4	SCL	Digital Input	Serial Clock for I2C
5	SDA/GS	Digital Input/Output	Serial Data for I2C/Gain Select
6	ADDR1	Digital Input	Mode and I2C address selection
7	ADDR2	Digital Input	Mode and I2C address selection
8	IN+	Analog Input	Positive Input
9	IN-	Analog Input	Negative Input
10	TPOUT	Analog Output	Analog Test Pin
11	VSS	Supply Ground	Supply Ground
12	AVDD	Analog Supply	Power Supply
13	SHUTDOWNB	Digital Input	Chip Enable (High = Enable; Low = PD)
14	IRQ	Digital Output	Interrupt Output
15	VDDSPK	Supply	Power Supply
16	SPK-	Analog Output	Negative BTL Output
17	VSSSPK	Supply Ground	Ground
18	VSSSPK	Supply Ground	Ground
19	VSSSPK	Supply Ground	Ground
20	SPK+	Analog Output	Positive BTL Output
21	EPad	Supply Ground	Thermal Tab (must be connected to VSSSPK)

4 BLOCK DIAGRAM

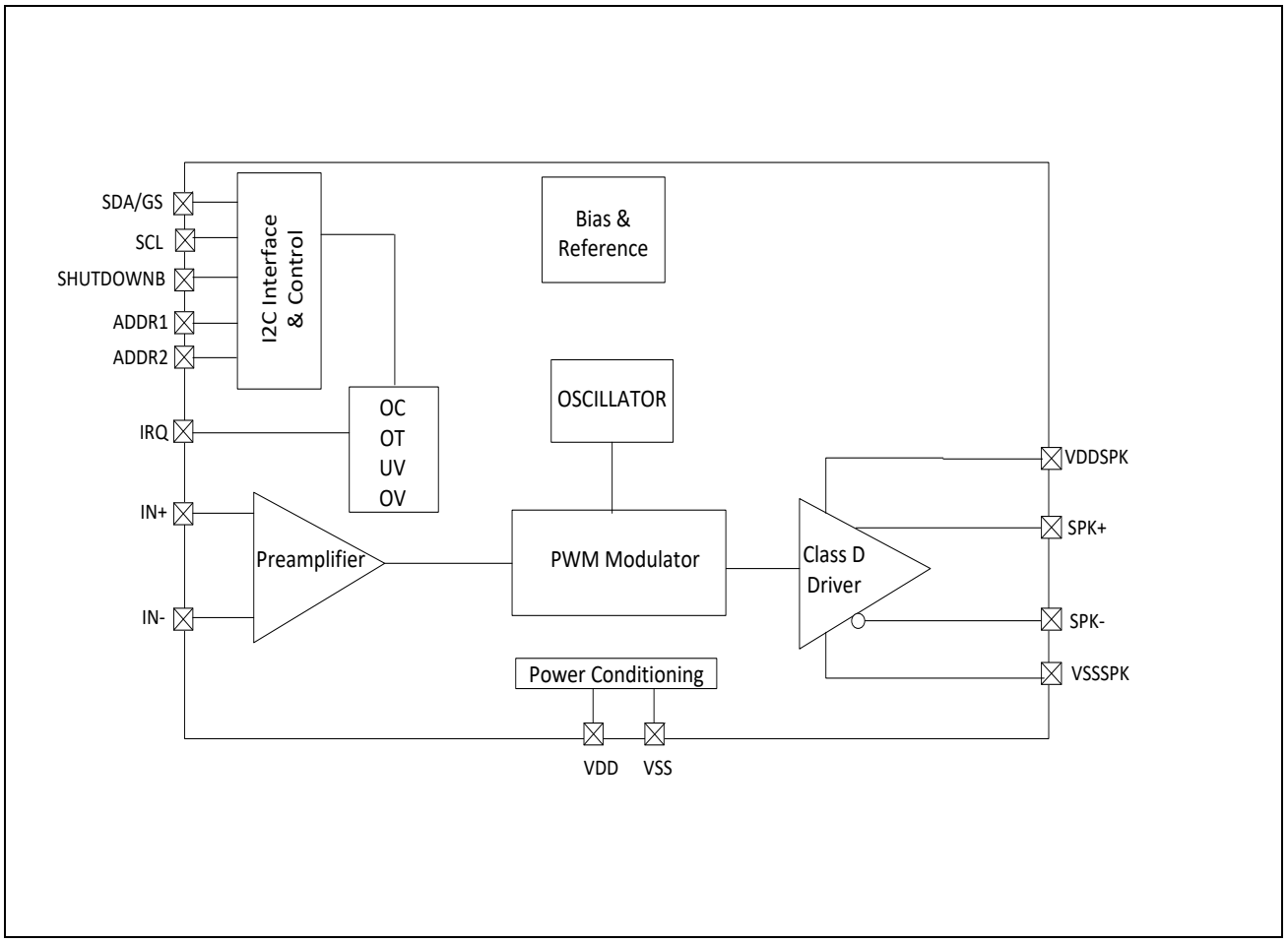


Figure 2 NAU82110 Block Diagram

5 ELECTRICAL CHARACTERISTICS

The tables in this chapter provide the various electrical parameters for the NAU82110 and their values.

5.1 Absolute Maximum Ratings

Condition	Min	Max	Units
Analog supply (AVDD)	-0.3	+5.50	V
Digital supply (DVDD)	-0.3	+5.50	V
Speaker supply range (VDDSPK)	-0.3	+14.1	V
Industrial operating temperature	-40	+105	°C
Storage temperature range	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

5.2 Operating Conditions

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Analog supply range	AVDD	2.70**	3.6	5.50	V
Digital supply range	DVDD	2.70**	3.6	5.50	V
Speaker supply range	VDDSPK	5.5	12	13.6**	V
Ground	VSS,VSSSPK		0		V

Note: ** When analog supply range is below 3V, VDDSPK is 13.6 V, high standby current is expected due to segment control

5.3 Analog Input Parameters

Condition	Min	Typ.	Max.	Unit
IN+ and IN-	GND-0.3	-	AVDD+0.3	V

5.4 Digital Input/Output Parameters

Condition	Min	Typ.	Max.	Unit	Test Conditions
Input Leakage Current SCL, SDA	-1	-	+1	μA	AVDD = DVDD = 5.5V
Input High Voltage VIH	0.7DVDD		5.5	V	
Input low Voltage VIL	VSS		0.3DVDD	V	
VOH (SDA)	0.9DVDD			V	
VOL (SDA)			0.2DVDD	V	IOL = 1 mA
SDA, SCL; pull up resistor value		50K		Ohm	

5.5 Electrical Parameters

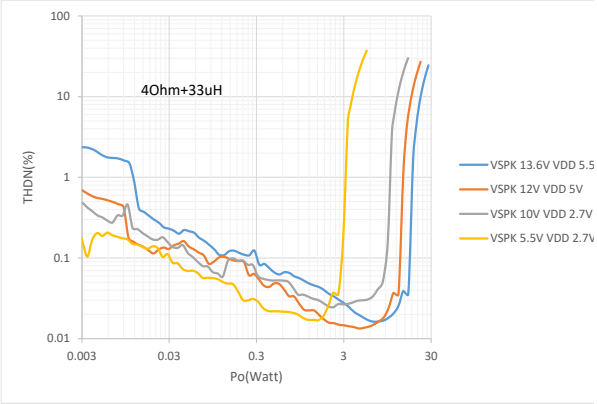
Conditions: SHUTDOWNB = DVDD = 5V, VDDSPK=12V, VSS = 0V, Av = 20dB, Z_L = ∞, BW = 20Hz to 22kHz, T_A = 25 °C

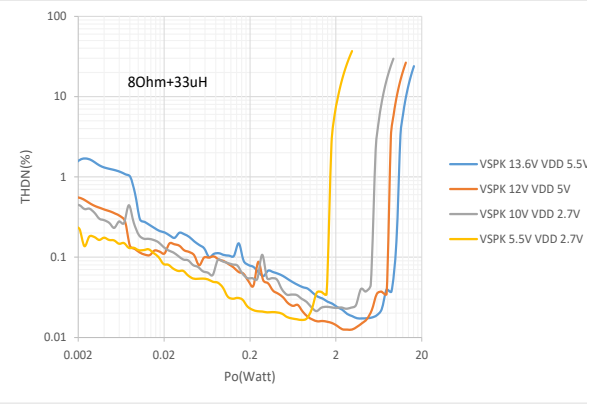
***Note 1** : PSRR = 20 x LOG10(GAIN x ΔAVDD/Δ(SPKP-SPKN)) dB*

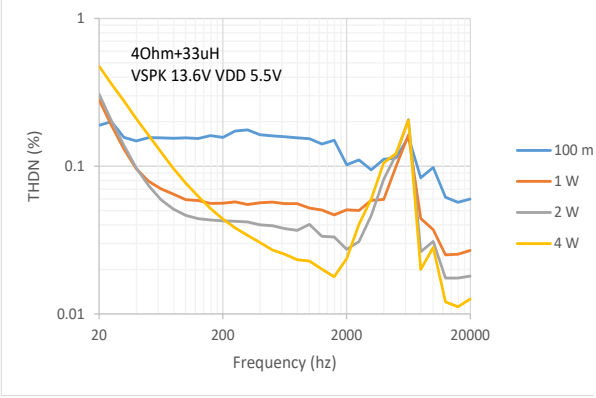
Symbol	Parameter	Conditions	Typical	Limit	Units
Class-D Channel					
P_O	Output Power	RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	8		W
		RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%	10		W
		RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	14		W
		RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%	18		W
THD+N	Total Harmonic Distortion + Noise	R_L = 8 Ω + 33 µH, f=1kHz, P_O = 2 W	0.019		%
e_{OS}	Output Noise	A-Weighted, 20Hz-20kHz, Receiver mode no input signal, gain = 0dB	40		µVrms
		A-Weighted, 20Hz-20kHz, no input signal, gain = 20dB	65		µVrms
SNR	Signal to noise ratio	R_L = 8 Ω + 33 µH, P_O = 8W, A-weighted	103		dB
		R_L = 8 Ω + 33 µH, P_O = 8W, unweighted	100		dB
		R_L = 4 Ω + 33 µH, P_O = 8W, A-weighted	100		dB
		R_L = 4 Ω + 33 µH, P_O = 8W, unweighted	97		dB
PSRR	Power Supply Rejection Ratio	DC, DVDD= 2.9V – 5.5V, GAIN = 20dB	89		dB
		f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} GAIN = 20dB	83		dB
		f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 200mV_{P_P} GAIN =20dB	79		dB
		f_{RIPPLE} = 4kHz, V_{RIPPLE} = 200mV_{P_P} GAIN = 20dB	70		dB
Fres	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, R_L = 8 Ω + 33 µH	+0.8/-0.1		dB
V_{OS}	Output Offset Voltage	Idle Channel, Gain= 0dB	±1	±5	mV
Kpop	Pop and Click Noise	A-weighted, Idle input, toggling amplifier on/off	0.12		mVrms
Rdson-P	Driver P MOS-FET ON-resistance	V_{BAT}= 5.0V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.199		Ohm
Rdson-N	Driver N MOS-FET ON-resistance	V_{BAT}= 5.0V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.149		Ohm
Fsw	Switching Frequency	Average	300		kHz

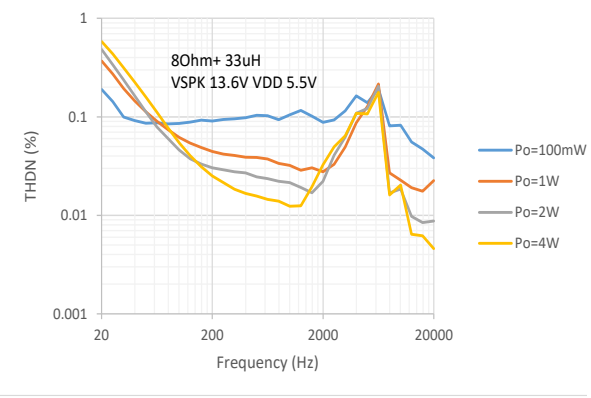
5.6 THD+N Plots

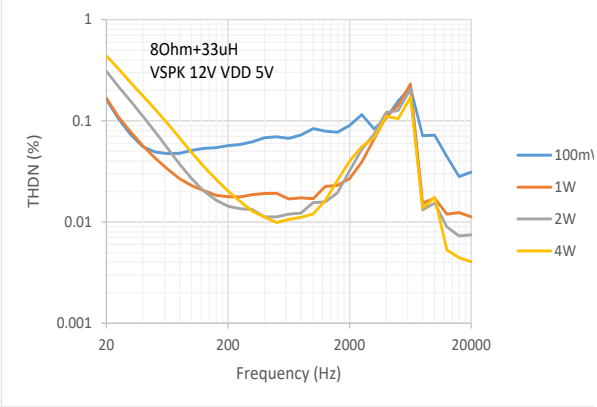
VDD is AVDD=DVDD, VSPK is VDDSPK

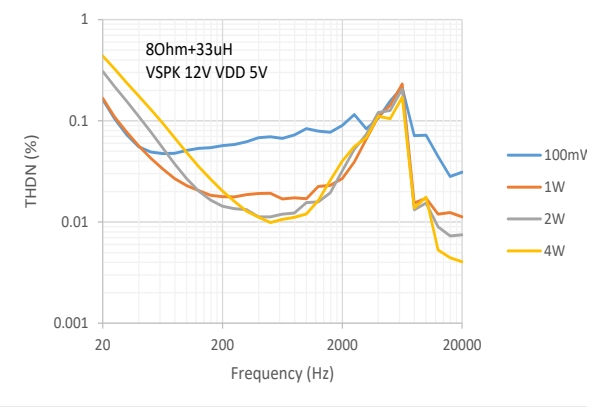


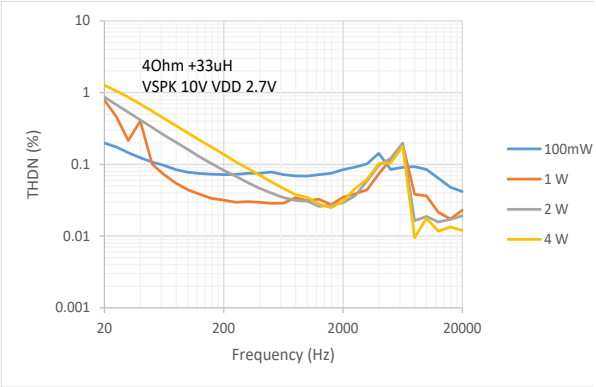


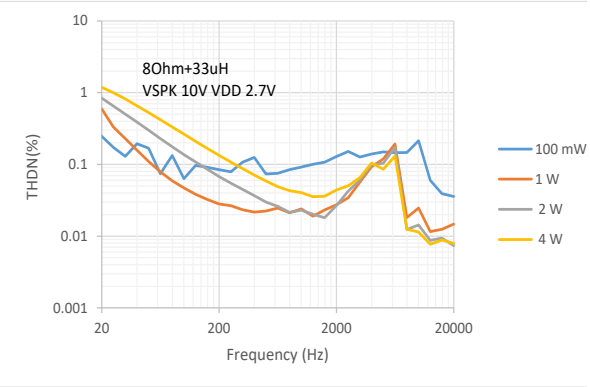


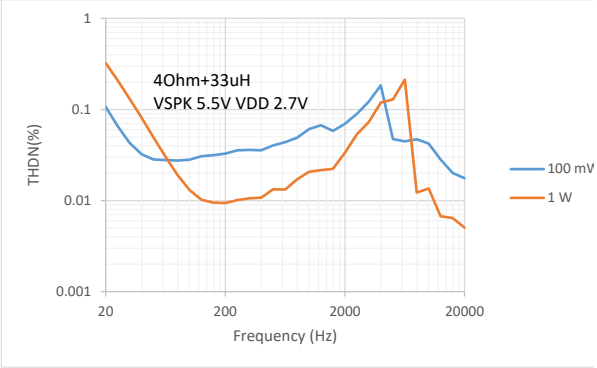


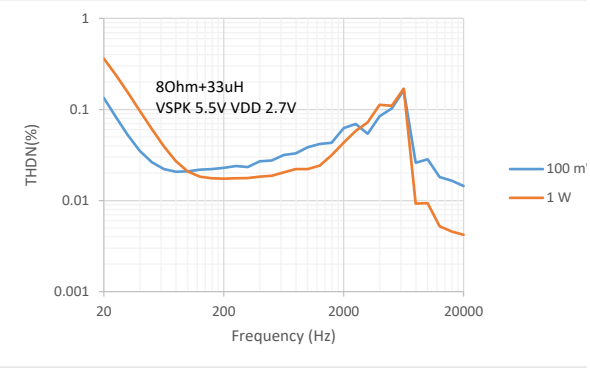




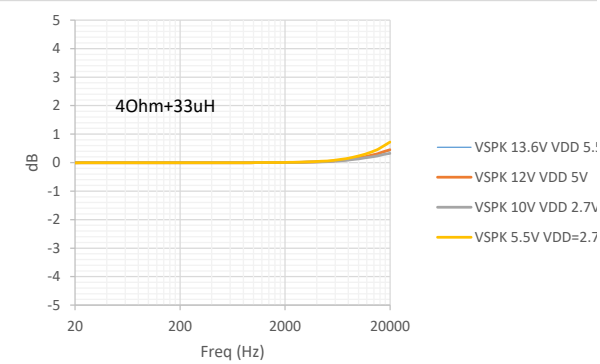

4Ohm +33uH
VSPK 10V VDD 2.7V
THDN (%)
Frequency (Hz)
100mW
1 W
2 W
4 W

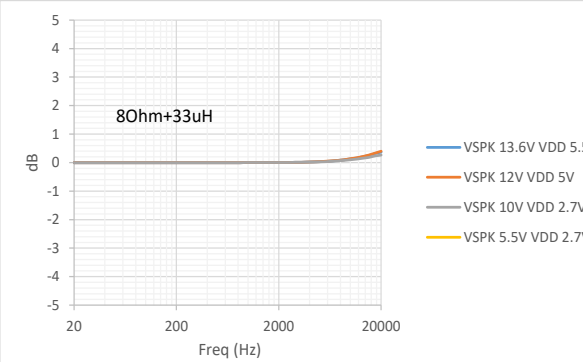

8Ohm+33uH
VSPK 10V VDD 2.7V
THDN(%)
Frequency (Hz)
100 mW
1 W
2 W
4 W


4Ohm+33uH
VSPK 5.5V VDD 2.7V
THDN(%)
Frequency (Hz)
100 mV
1 W

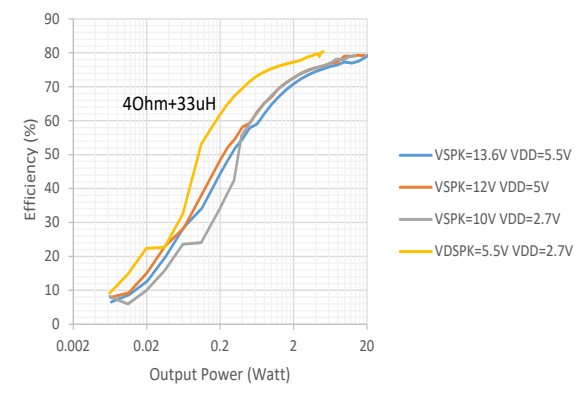

8Ohm+33uH
VSPK 5.5V VDD 2.7V
THDN(%)
Frequency (Hz)
1 W

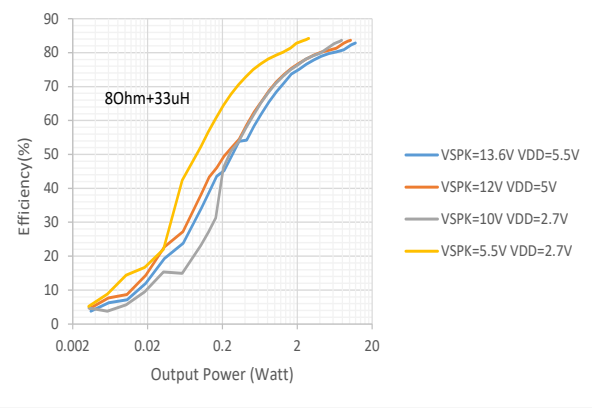
5.7 Frequency Response Plots





5.8 Power Efficiency





6 FUNCTIONAL DESCRIPTION

The NAU82110 offers excellent quantity performance as high efficiency, high output power and low quiescent current. It also provides the following special features.

6.1 Wire-Serial Control and Data Bus (I2C Style Interface)

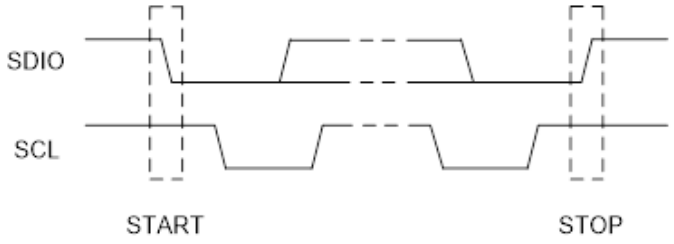
The serial interface provides a 2-wire bidirectional read/write data interface similar to and typically compatible with standard I2C protocol. This protocol defines any device that sends CLK onto the bus as a master, and the receiving device as slave. The NAU82110 can function only as a slave device. An external clock drives the device, and in accordance with the protocol, data is sent to or from the device accordingly. All functions are controlled by means of a register control interface in the device.

6.2 2-Wire Protocol Convention

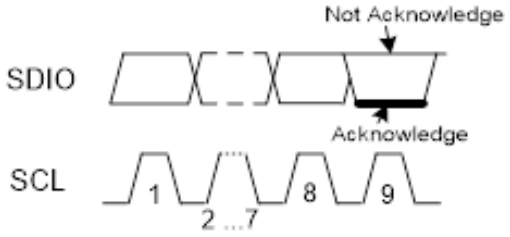
All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition at the end of a read or write operation places the serial interface in standby mode.

An acknowledge (ACK), is a software convention is used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting eight bits to allow for the ACK response. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data.

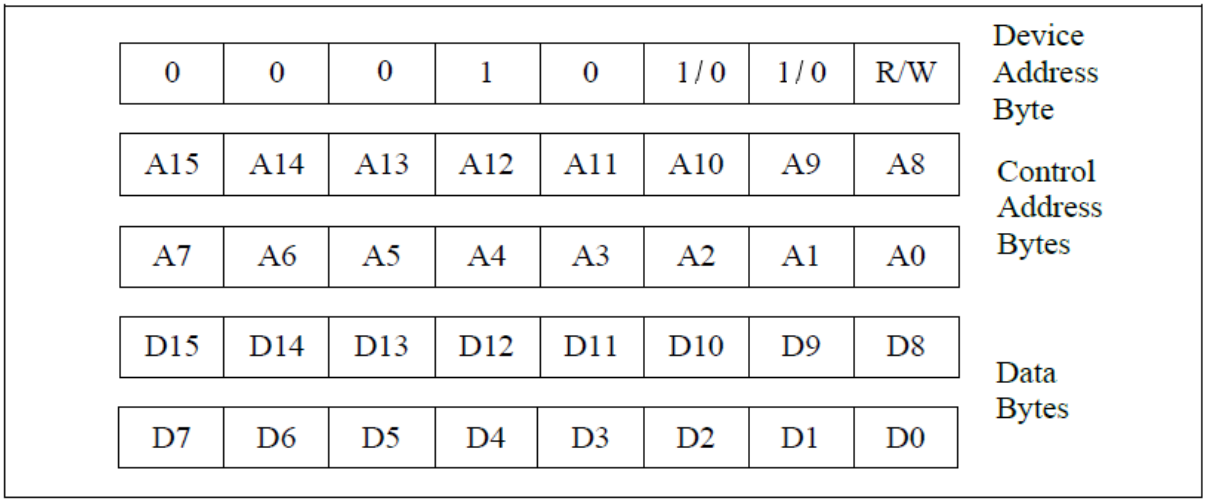
Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W= 1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.



START and STOP Signals



Acknowledge and NOT Acknowledge



Slave Address Byte, Control Address Byte, and Data Byte

Figure 3 I2C Protocol

6.3 2-Wire Write Operation

A Write operation consists of a two-byte instruction followed by a Data Byte. A Write operation requires a START condition, followed by a valid device address byte with R/W= 0, a valid control address byte, data byte, and a STOP condition.

The NAU82110 has a selectable I2C address scheme. See section 6.6.1 for setting the I2C address. If the Device Address matches the set value, the NAU82110 will respond with the expected ACK signaling as it accepts the data being transmitted into it.

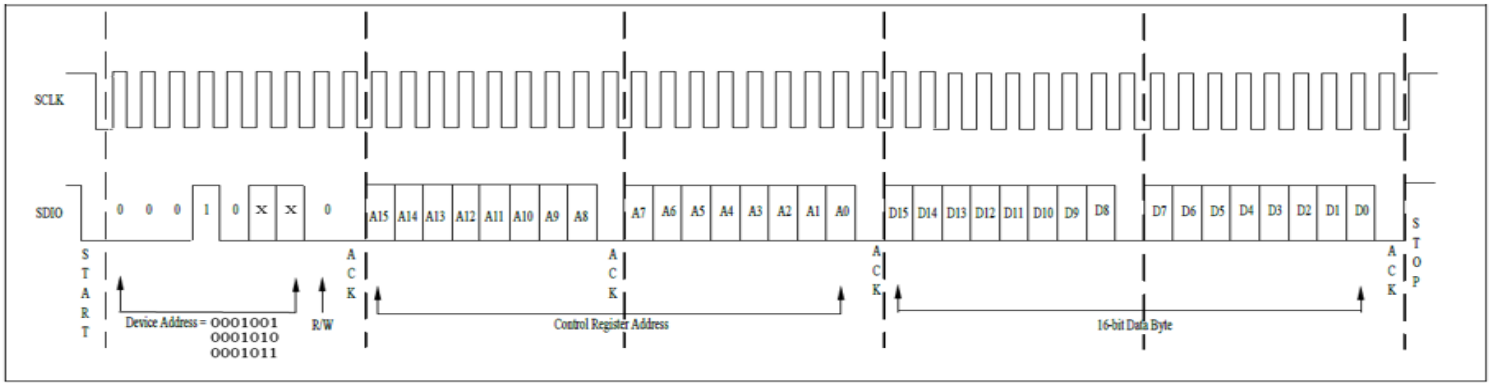


Figure 4 I2C Write Sequence

6.4 2-Wire Single Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of data byte. The bus master initiates the operation issuing the following sequence: a START condition, device

address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

The NAU82110 is programmable with ADDR1 and ADDR2 (Section 6.6.1) as its device address. If the device address matches this value, the NAU82110 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU82110 transmits an ACK, followed by a one-byte value containing the data from the selected control register inside the NAU82110. During this phase, the master generates the ACK signaling with byte transferred from the NAU82110.

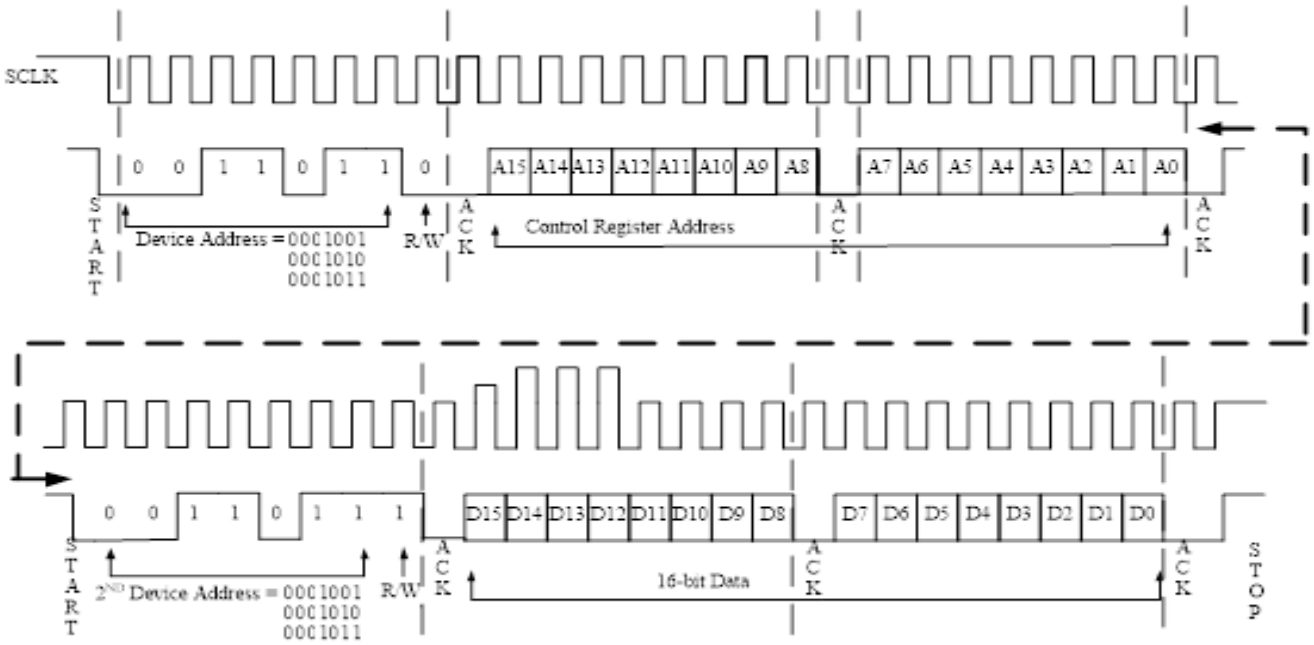
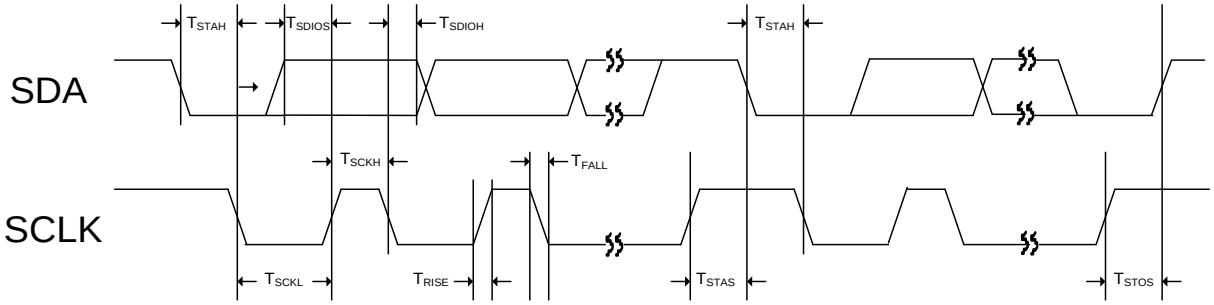


Figure 5 I2C Read Sequence

6.5 2-Wire Timing

The NAU82110 is compatible with serial clock speeds defined as “standard mode” with SCL 0 - 100 kHz, and “fast mode” with SCL 0 - 400 kHz. At these speeds, the total bus line capacitance load is required to be 400 pF or less.

Open collector drivers are required for the serial interface. Therefore, the bus line rise time is determined by the total serial bus capacitance and the DVDD pull-up resistors. The NAU82110 defaults to a weak pull up (typical 50 k ohm) for applications with no external pull up resistor.



Symbol	Description	Min	Typ	Max	Unit
T_{STAH}	SDA falling edge to SCL falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCL rising edge to SDA falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCL rising edge to SDA rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCL High Pulse Width	600	-	-	ns
T_{SCKL}	SCL Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDAS}	SDA to SCL Rising Edge DATA Setup Time	100	-	-	ns
T_{SDAH}	SCL falling Edge to SDA DATA Hold Time	0	-	600	Ns

6.6 Volume Control

The volume control operates in either an analog voltage mode, through the Gain Select pin (GS) or through the I2C interface. The I2C volume control has 32 levels controlled by Reg0x13[4:0]. In analog mode, there are 5 gain settings. To enter the analog mode, connect ADDR1 and ADDR2 to GND. If ADDR1 or ADDR2 are not GND, then an I2C address is selected and the I2C interface is used to set the gain.

6.6.1 I2C mode

ADDR2	ADDR1	SA7 to SA0
0	0	Analog mode(I2C disabled)
0	1	0001001x(I2C mode)
1	0	0001010x(I2C mode)
1	1	0001011x(I2C mode)

SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
0	0	0	1	0	ADDR2	ADDR1	Read/$\overline{\text{Write}}$

The slave address register is shown above. To select the device, address the user sends the slave address (SA7-SA1) plus a write bit (SA0 active low). Data (D0 to D7) can then be sent to the device in the usual 8-bit format. The lower 5 bits of the data bit are used to set the digital volume control according to table below. The upper 3 bits should be set to zero. There are 32 gain settings including a mute pin selection (pin2).

REG0x13 GAIN_INDEX							
D15(MSB)	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0(LSB)
0	0	0	Vol5	Vol4	Vol3	Vol2	Vol1

6.6.2 Standalone mode

In Analog mode SCL, ADDR1 and ADDR2 are tied to VSS, the gain is set using the “GS” Pin, there are 5 Settings available depending on external hardware settings. 36dB, 32dB, 24dB, 20dB and 0dB are all selectable by hardware jumper. See table below.

GS Pin Configuration	**Internal Gain (dB)**
GS tie to DVDD or AVDD	36
GS connect to DVDD or AVDD through 100kΩ ± 5% resistor	32
GS tie to DVDD or AVDD	24
GS connect to VSS through 100kΩ ± 5% resistor	20
GS tie to VSS	0

6.7 Device Protection

The NAU82110 includes the following types of device protection:

Over Current Protection (OCP)
Supply Over Voltage Protection (OVP)
Under Voltage Lock Out (UVLO)
Over Temperature Protection (OTP)

6.7.1 Over Current Protection (OCP)

It is provided in the NAU82110. If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 16.7µsec, the output drivers will be disabled for 100msec. The output drivers will then be enabled again and checked for the short circuit. If the short circuit is still present, the output drivers are disabled after 16.7µsec. This cycle will continue until the short circuit is removed. The short circuit threshold is 3.2A at 12V with all driver segment on.

6.7.2 Supply Over Voltage Protection (OVP)

It provides in the NAU82110. If the VDDSPK supply voltage reaches 14.1V, the output drivers will be set to pull down to ground while the NAU82110 control circuitry continues to operate. If the supply drops below 13.2V, the output drivers are re-enabled.

6.7.3 Under Voltage Lock Out (UVLO)

It provides Supply Under Voltage Protection in the NAU82110. If supply voltages drop below 2.5V, the output drivers will be disabled while the NAU82110 control circuitry continues to operate. This will prevent the battery supply from going too low before the host processor can safely shut down the devices on the system. If the supply goes back up, the drivers will be enabled again at 2.55V. If the supply drops further (below 1.6 V), the internal power-on reset is activated and puts the entire device into the power-down state. Under voltage lockout (UVLO) If AVDD is less than 2.5V (AVDD UVLO = 2.5V) or if VDDSPK is less than 4V (VDDSPK UVLO = 4V).

6.7.4 Over Temperature Protection (OTP)

It provides in the event of thermal overload. When the internal junction temperature of the device reaches 140°C, the NAU82110 will disable the output drivers. When the device cools down and a safe operating temperature of 125°C has been achieved for at least 100 msec, the output drivers will be enabled again.

6.7.5 Power-up and Power-down Control

When the supply voltage ramps up, the internal power on reset circuit gets triggered. At this time all internal circuits will be set to power down state. The device can be enabled by setting the SHUTDOWNB pin high. Upon setting the SHUTDOWNB pin high, the device will go through an internal power up sequence in order to minimize 'pops' on the speaker output. The complete power up sequence will take about **4.6ms**. The device will power down in about **600µs**, when the SHUTDOWNB pin is set low.

It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize the 'pops' when the SHUTDOWNB pin is toggled.

Bypass capacitors are required to remove the AC ripple on the AVDD/DVDD pins. The value of these capacitors depends on the length of the trace. In most cases, 10 µF and 0.1 µF are sufficient to achieve good performance.

6.8 Control & Status Registers

# Hex	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
0	HARDWARE_RST	HW_RST																	**Hardware Reset** (Write any value ***TWICE*** to reset all the config registers.)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
1	SOFTWARE_RST	SW_RESET																	**Software Reset** (Write any value ***TWICE*** to reset all internal states without resetting the config registers.)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
5	IRQ_MASK	EXTIRQ_INT_DIS																	**External IRQ Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		TALARM_INT_DIS																	**TALARM Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		SHUTDOWN_INT_DIS																	**Shutdown Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		LOVDDDETB_INT_DIS																	**Low Voltage Detection Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		OVP_INT_DIS																	**Over Voltage Protection Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		EXTIRQ_MASK																	**External IRQ Mask Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		TALARM_MASK																	**TALARM Mask Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		SHUTDWN_MASK																	**Shutdown Mask Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		LOVDDDETB_MASK																	**Low Voltage Detection Mask Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		OVP_MASK																	**Over Voltage Protection Mask Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	**0x007E**
A	IRQ_CTRL	IRQ_PL																	**IRQ Polarity Logic Select** 0 = Active low (DEFAULT) 1 = Active high
		IRQ_PU																	**IRQ Pull Up Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		IRQ_PD																	**IRQ Pull Down Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		IRQ_CS																	**IRQ Type Select** 0 = CMOS (DEFAULT) 1 = Schmitt trigger
		IRQ_OE																	**IRQ Output Enable Control** 0 = Disable 1 = Enable (DEFAULT)

# Hex	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		IRQ_IE																	**IRQ Input Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		IRQ_PDRV																	**IRQ Driving Strength Select** 00 = 4mA (DEFAULT) 01 = 8mA 10 = 12mA 11 = 16mA
		IRQ_SL																	**IRQ Slew Rate Select** 0 = Low (DEFAULT) 1 = High
		DEFAULT	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	**0x0800**
B	SCL_PAD_CTRL (I2C CLOCK PIN)	SCL_PAD_PU																	**SCL Pull Up Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SCL_PAD_PD																	**SCL Pull Down Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SCL_PAD_CS																	**SCL Type Select** 0 = CMOS (DEFAULT) 1 = Schmitt trigger
		SCL_PAD_PDRV																	**SCL Driving Strength Select** 00 = 4mA (DEFAULT) 01 = 8mA 10 = 12mA 11 = 16mA
		SCL_PAD_SL																	**SCL Slew Rate Select** 0 = Low (DEFAULT) 1 = High
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
C	SD_PAD_CTRL (I2C DATA PIN)	SD_PAD_PU																	**SD Pull Up Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SD_PAD_PD																	**SD Pull Down Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SD_PAD_CS																	**SD Type Select** 0 = CMOS (DEFAULT) 1 = Schmitt trigger
		SD_PAD_PDRV																	**SD Driving Strength Select** 00 = 4mA (DEFAULT) 01 = 8mA 10 = 12mA 11 = 16mA
		SD_PAD_SL																	**SD Slew Rate Select** 0 = Low (DEFAULT) 1 = High
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
10	IRQ STATUS	EXTIRQ_INT																	**External IRQ Interrupt Status**
		TALARM_INT																	**TALARM Interrupt Status**
		SHUTDWN_INT																	**Shutdown Control Interrupt Status**
		LOVDDDETB_INT																	**Low Voltage Detection Interrupt Status**
		OVP_INT																	**Over Voltage Protection Interrupt Status**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
11	IRQ_CLR	EXTIRQ_CLR																	**External IRQ Interrupt Clear Control** 0 = No action (DEFAULT) 1 = Clear interrupt

# Hex	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		SHUTDWN_CLR																	**Shutdown Interrupt Clear Control** 0 = No action (DEFAULT) 1 = Clear interrupt
		TALARM_CLR																	**TALARM Interrupt Clear Control** 0 = No action (DEFAULT) 1 = Clear interrupt
		LOVDDDETB_CLR																	**Low Voltage Interrupt Clear Control** 0 = No action (DEFAULT) 1 = Clear interrupt
		OVP_CLR																	**Over Voltage Protection Interrupt Clear Control** 0 = No action (DEFAULT) 1 = Clear interrupt
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
13	GAIN_INDEX	GAIN INDEX																	**Digital Volume Select** 00000 = -120dB/Mute (Step size is 4dB.) 00001 = -84dB 00010 = -80dB 00011 = -76dB ▼ 10101 = -4dB 10110 = 0dB (DEFAULT) 10111 = 4dB ▼ 11101 = 28dB 11110 = 32dB 11111 = 36dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	**0x0016**
14	GAIN_DIG_L	GAIN_DIG_L																	**Digital Gain Read Register** (For Reg0x13 lower two-byte gain)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
15	GAIN_DIG_H	GAIN_DIG_L																	**Digital Gain Read Register** (For Reg0x13 higher three-byte gain)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
18	MISC	IRQ_ENABLE																	**IRQ Output Enable Control** 0 = Disable (It would pass one of 0x18[10:8] status whichever is specified) 1 = Enable (Default)
		CTRL_PIN_MUX																	**Control Pin Mutiplexing Select** (when MISC[11]=0) 000 = TALARM (DEFAULT) 001 = SHIRTR 010 = LOVDDDETB 011 = OVP 100 = MUTEB 101 = PDOSCB 110 = PWRDOWN1B_D 111 = SHUTDWNDRVRR
		UVLO_EN																	**UVLO Enable Control** 0 = Disable 1 = Enable (Default)

# Hex	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		MONITOR_OSC																	**Monitoring Internal OSC by IRQ Pin Enable Control** (CFG_REG0A[11] is set to 1 automatically if this bit is enabled.) 0 = Disable (Default) 1 = Enable
		SHUTDOWNB_CS																	**SHUTDOWNB Input Select** 0 = CMOS (Default) 1 = Schmitt Trigger
		MUTE_CS																	**MUTE input Select** 0 = CMOS 1 = Schmitt Trigger (Default)
		ADDR_CS																	**ADDR input Select** 00 = CMOS (Default) 11 = Schmitt Trigger
		DEFAULT	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	**0x0824**
40	BDM_DIV_SEL	PWMMODE																	**PWM Mode Select** 0 = (Default)
		BDM_DIV_SEL																	**BDM Select**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
55	MODE	MODE																	**Mode Select** 0 = I2C (Default)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
58	I2C_DEVICE_ID	I2C_DEVICE_ID																	**I2C Device ID**
		SILICON REVISION ID																	**Silicon Revision Bits**
		DEFAULT	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	**0x09F1**
69	MTO	COARSE_LOOP																	**Coarse Trim Select** (To reduce EMI)
		FINE_INC																	**Incremental Fine Trim Select**
		FINE_SLOP																	**OSC Fine Trim Select**
		DEFAULT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	**0x00C0**

7 APPLICATION CIRCUIT

7.1 Typical Application Diagram

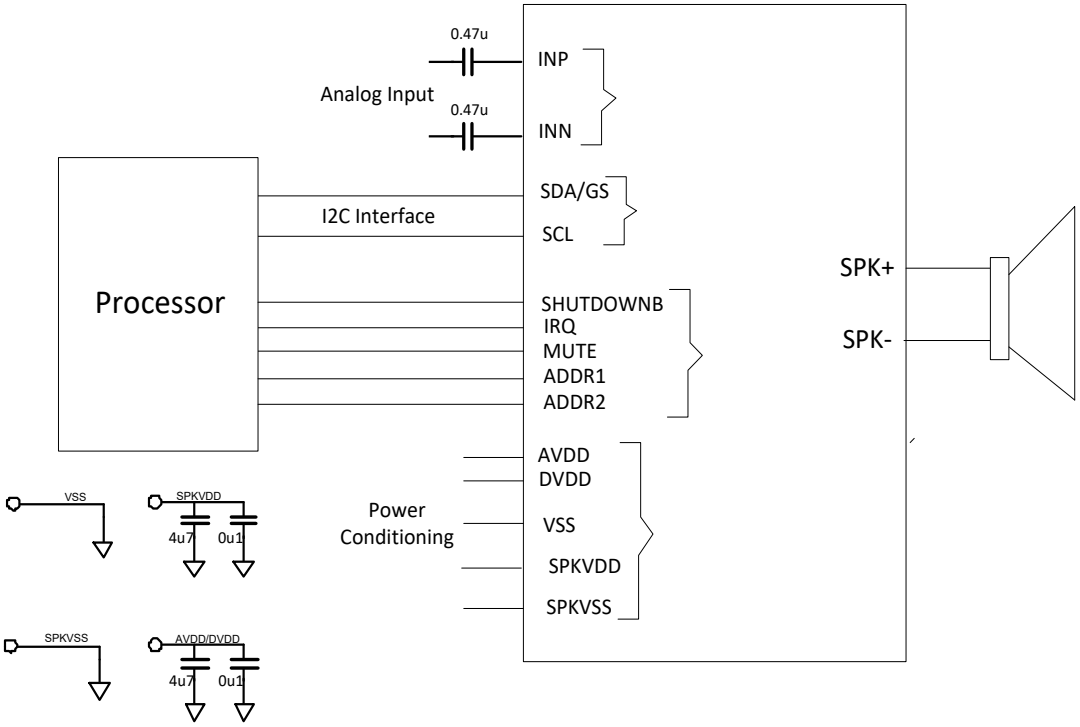


Figure 6 NAU82110 System Diagram by I2C

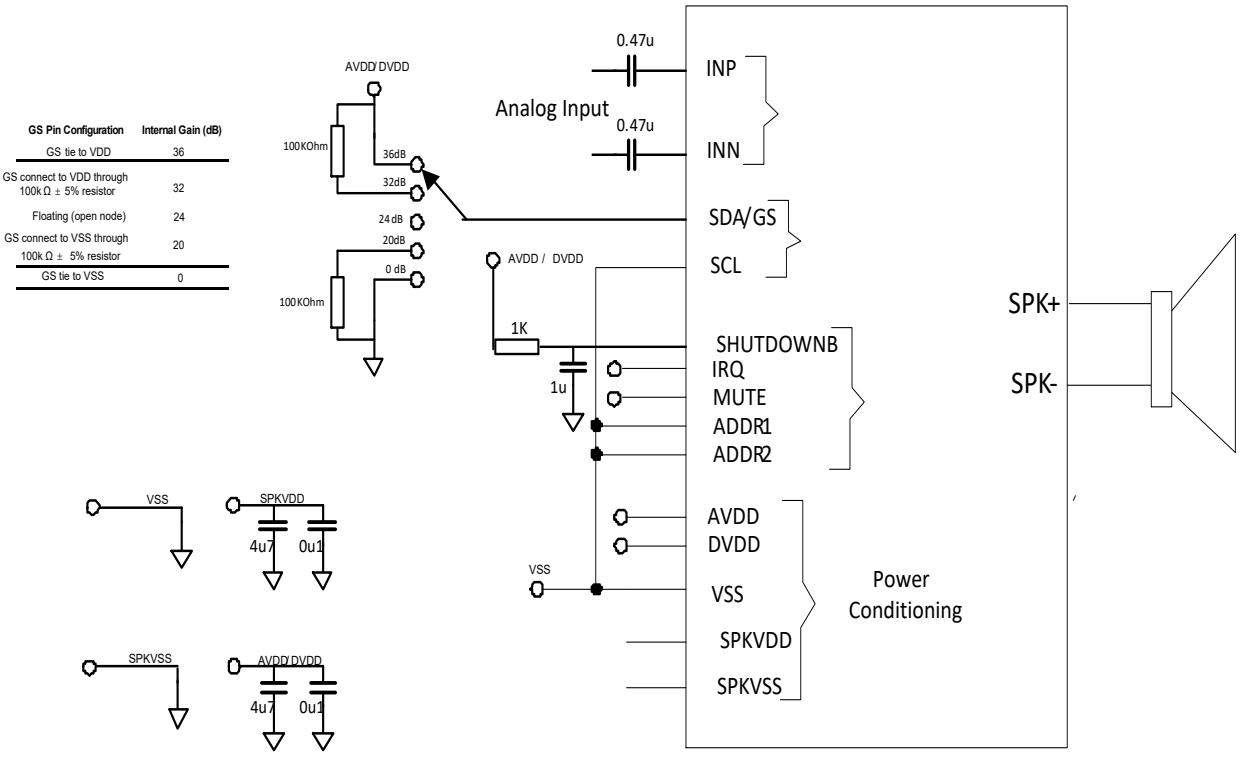


Figure 7 NAU82110 Standalone System Diagram

Note: SHUTDOWNB pin need to add a 1~10uF capacitor and 1KOhm resistor connection with DVDD or AVDD

7.2 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. It is better to use low-resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

7.3 PCB Layout Notes

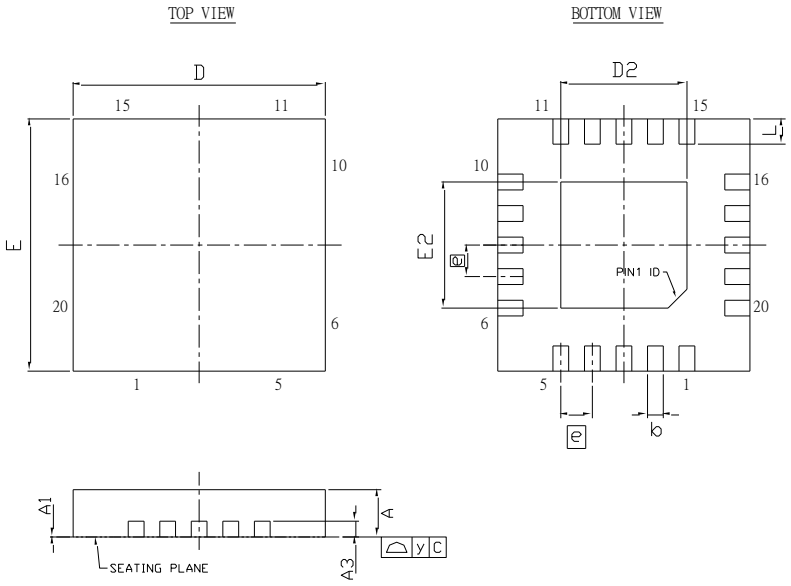
The Class-D Amplifier is a high-power switching circuits that can cause Electro Magnetic Interference (EMI) when poorly connected. Therefore, care must be taken to design the PCB eliminate Electro Magnetic Interference (EMI), reduce IR drops, and maximize heat dissipation.

The following notes are provided to assist product design and enhance product performance:

- Use a VSS plane, preferably on both sides, to shield clocks and reduce EMI.
- Maximize the copper to the VSS pins and have solid connections to the plane.
- Planes on DVDD & AVDD are optional.
- The DVDD & AVDD connection needs to be a solid piece of copper.
- Use thick copper options on the supply layers if cost permits.
- Keep the speaker connections short and thick. Do not use VIAs.
- Use a small speaker connector like a wire terminal block (Phoenix Contact)
- For better heat dissipation, use VIAs to conduct heat to the other side of the PCB.
- Do not use VIA's to connect OUT+ & OUT-. Use a direct top layer copper connection to the pins. Thick copper is preferred.
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane.
- The digital IO lines can be shielded between power planes.

8 PACKAGE DIMENSION

20-lead plastic QFN 20; 4X4mm^2, 0.8mm thickness, 0.5mm lead pitch.



Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note:D2,E2 by die size difference .

NAU82110 20 pin QFN Package Specification

9 ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU82110YG	4mm x 4mm	QFN-20	Green

NAU82110 _ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-20

10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Aug 29, 2024	Initial Release
1.1	Jan 15, 2025	Update Typical Application Diagram Update Pin Diagram Update Register Names

IMPORTANT NOTICE

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