# HI-8598

Galvanically Isolated
Single-Rail ARINC 429 Differential Line Driver

December 2023

## GENERAL DESCRIPTION

The HI-8598 is the world's first galvanically isolated ARINC 429 line driver, available in a compact 18-pin SOIC plastic package. Patented capacitive isolation and power regulation provide 800V galvanic isolation between the analog line driver and the logic interface, making this device ideal for systems that must tolerate different grounds.

Logic inputs feature built-in 4kV ESD input protection (HBM) as well 3.3V logic level compatibility.

37.5 Ohm or 5 Ohm resistors in series with each ARINC output are available to allow the use of external resistors for lightning protection.

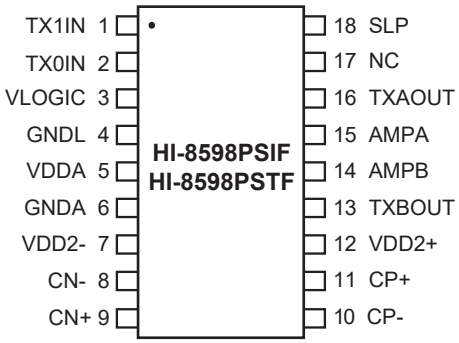
The HI-8598 line driver is intended for use where logic signals must be converted to ARINC 429 levels (such as when using an FPGA or Holt's HI-3220 or HI-35860 ARINC 429 protocol ICs) and where it is important to fully isolate the ARINC 429 data bus from digital circuitry.

The part is available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

## FEATURES

- Airbus ABD0100H specification compliant
- Galvanically isolated ARINC 429 line driver providing 800V isolation between the analog line driver and the logic interface
- All ARINC 429 voltage levels generated on-chip
- Digitally selectable rise and fall times
- 5 Ohm or 37.5 Ohm output resistance
- Industrial and Extended temperature ranges
- Burn-in available

## PIN CONFIGURATION (TOP VIEW)




**18-Pin Plastic SOIC package (Wide Body)**

Table 1. Function Table

| TX1IN | TX0IN | SLP | TXAOUT | TXBOUT | SLOPE |
|---|---|---|---|---|---|
| 0 | 0 | X | 0V | 0V | N/A |
| 0 | 1 | 0 | -5V | 5V | 10µs |
| 0 | 1 | 1 | -5V | 5V | 1.5µs |
| 1 | 0 | 0 | 5V | -5V | 10µs |
| 1 | 0 | 1 | 5V | -5V | 1.5µs |
| 1 | 1 | X | Hi-Z | Hi-Z | N/A |

## BLOCK DIAGRAM

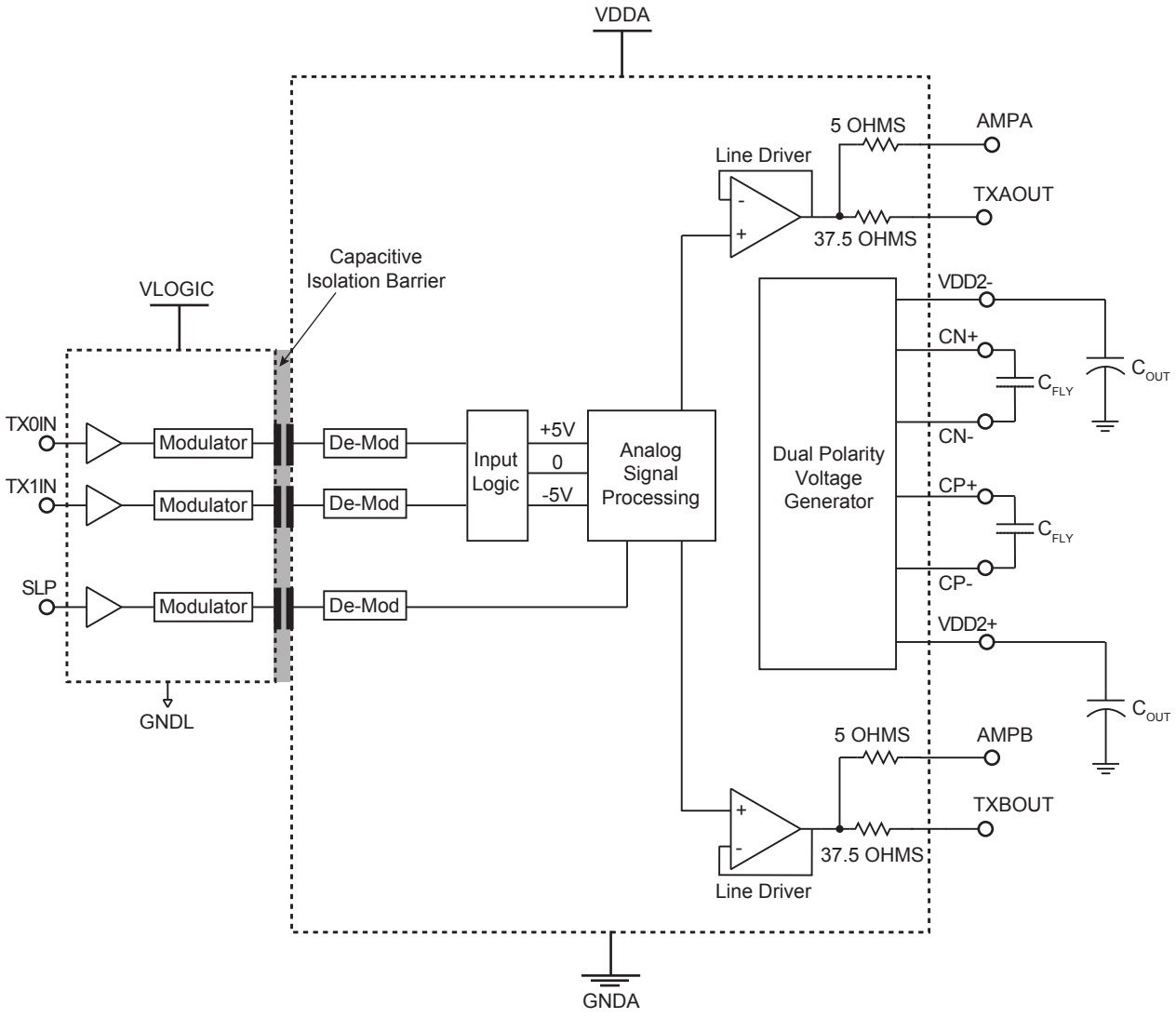



Figure 1. HI-8598 Functional Block Diagram

## PIN DESCRIPTIONS

Table 2. Pin Descriptions

| Pin # | Pin Name | Function | Description |
|---|---|---|---|
| 1 | TX1IN | INPUT | Data input one |
| 2 | TX0IN | INPUT | Data input zero |
| 3 | $V_{LOGIC}$ | POWER | 3.3V power supply for digital logic |
| 4 | GNDL | POWER | Ground for digital logic |
| 5 | $V_{DDA}$ | POWER | 3.3V power supply for analog line driver |
| 6 | GNDA | POWER | Ground for analog line driver |
| 7 | $V_{DD2-}$ | OUTPUT | Voltage doubler negative output (~ −6.0V for 3.3V supply) |
| 8 | CN- | ANALOG | $V_{DD2-}$ flyback capacitor, $C_{FLY}$; negative terminal |
| 9 | CN+ | ANALOG | $V_{DD2-}$ flyback capacitor, $C_{FLY}$; positive terminal |
| 10 | CP- | ANALOG | $V_{DD2+}$ flyback capacitor, $C_{FLY}$; negative terminal |
| 11 | CP+ | ANALOG | $V_{DD2+}$ flyback capacitor, $C_{FLY}$; positive terminal |
| 12 | $V_{DD2+}$ | OUTPUT | Voltage doubler positive output (~ +6.0V for 3.3V supply) |
| 13 | TXBOUT | OUTPUT | ARINC low output with 37.5 Ohms series resistance |
| 14 | AMPB | OUTPUT | ARINC low output with 5 Ohms series resistance |
| 15 | AMPA | OUTPUT | ARINC high output with 5 Ohms series resistance |
| 16 | TXAOUT | OUTPUT | ARINC high output with 37.5 Ohms series resistance |
| 17 | NC | No Connect | Do not connect. |
| 18 | SLP | INPUT | Output slew rate control. High selects ARINC 429 high-speed. Low selects ARINC 429 low-speed. |

## FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the line driver. An integrated inverting / non-inverting voltage doubler generates the rail voltages (± 6.0V) which are then used to produce the ± 5V ARINC 429 output levels. The analog circuitry is fully isolated from the digital logic.

The internal dual polarity charge pump circuit requires four external capacitors, two for each polarity generated by the doubler. CP+ and CP- connect the external charge transfer or "fly" capacitor, $C_{FLY}$, to the positive portion of the doubler, resulting in twice $V_{DDA}$ at the $V_{DD2+}$ pin. An output "hold" capacitor, $C_{OUT}$, is placed between $V_{DD2+}$ and GND. $C_{OUT}$ should be ten times the size of $C_{FLY}$. The inverting or negative portion of the converter works in a similar fashion, with $C_{FLY}$ and $C_{OUT}$ placed between CN+ / CN- and $V_{DD2-}$ / GND respectively.

Currents for slope control are set by on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as Holt's HI-3210 or HI-3220. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an "A" side internal capacitor while the "B" side is enabled to -5V. The charging current is selected by the SLP pin. If the SLP pin is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If SLP is low, the rise and fall times are 10µs.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8598.

The HI-8598 has 37.5 ohms in series with each TXOUT output and 5 ohms in series with each AMP output. The AMP outputs are for applications where external series resistance is required, typically for lightning protection devices. Holt Application Note AN-300 describes suitable lightning protection schemes.

Tri-stateable outputs allow multiple line drivers to be connected to the same ARINC 429 bus. Set TX1IN and TX0IN both to a logic "1" to force the outputs in the high-impedance state.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltages | |
| $V_{DDA}$ | +7.0V |
| $V_{LOGIC}$ | +7.0V |
| Junction Temperature ($T_{JMAX}$) | 175°C |
| Common-mode input voltage | +/- 1,000V |
| Solder Temperature (reflow) | 260°C |
| Storage Temperature | -65°C to +150°C |

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply Voltages | |
| $V_{DDA}$ | +3.0V to +3.6V |
| $V_{LOGIC}$ | +3.0V to +3.6V |
| Temperature Range | |
| Industrial Screening | -40°C to +85°C |
| Hi-Temp Screening | -55°C to +125°C |

*NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.*

# ELECTRICAL CHARACTERISTICS

## Table 3. DC Electrical Characteristics

$V_{DDA}$ = $V_{LOGIC}$ = [+3.0V, +3.6], $T_A$ = Operating Temperature Range (unless otherwise stated)

| Parameters | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Voltage (TX1IN, TX0IN, SLP) | | | | | | |
| High | $V_{IH}$ | | 2.0 | - | - | V |
| Low | $V_{IL}$ | | - | - | $0.3V_{DD}$ | V |
| Common Mode Offset | $V_{DIFF}$ | GNDL w.r.t. GNDA, all pins | -800 | | +800 | V |
| Input Current (TX1IN, TX0IN, SLP) | | (73kΩ Internal Pulldown) | | | | |
| | $I_{IH}$ | $V_{IN}$ = 3.3V | - | 45 | - | µA |
| | $I_{IL}$ | $V_{IN}$ = 0V | - | - | -0.1 | µA |
| ARINC Output Voltage (Differential) | | | | | | |
| one | $V_{DIFF1}$ | no load; TXAOUT - TXBOUT | 9 | 10 | 11 | V |
| zero | $V_{DIFF0}$ | no load; TXAOUT - TXBOUT | -11 | -10 | -9 | V |
| null | $V_{DIFFN}$ | no load; TXAOUT - TXBOUT | -0.5 | 0 | 0.5 | V |
| ARINC Output Voltage (Ref. to GND) | | | | | | |
| one or zero | $V_{DOUT}$ | no load & magnitude at pin | 4.5 | 5.0 | 5.5 | V |
| null | $V_{NOUT}$ | no load | -0.25 | 0 | 0.25 | V |
| Operating Supply Current | | SLP = $V_{LOGIC}$ | | | | |
| No Load (Logic) | $I_{DDNL}$ | TX1IN = TX0IN = $V_{LOGIC}$ = 0V | - | 0.6 | 1.0 | mA |
| No Load (Analog) | $I_{DDNLA}$ | TX1IN = TX0IN = $V_{LOGIC}$ = 0V | - | 40 | 50 | mA |
| Max. Load (Analog) | $I_{DDLA}$ | 100kHz, 400Ω load | - | 65 | - | mA |
| ARINC Outputs Shorted | $I_{DDS}$ | See Note 1 | - | 165 | - | mA |
| Power Dissipation in device[2] | | SLP = $V_{LOGIC}$ | | | | |
| No load (Analog) | $P_{DDNLA}$ | TX1IN = TX0IN = $V_{LOGIC}$ = 0V | - | 132 | 180 | mW |
| Max. Load (AMPA to AMPB) | $P_{DDLA}$ | 100kHz, 400Ω load [3] | - | 264 | - | mW |
| Max. Load (TXAOUT to TXBOUT) | $P_{DDLT}$ | 100kHz, 400Ω load | - | 294 | - | mW |
| ARINC Outputs Shorted (AMP outputs) | $P_{DDSA}$ | See Note 1 | - | 390 | - | mW |
| ARINC Outputs Shorted (TXOUT outputs) | $P_{DDST}$ | See Note 1 | | 550 | - | mW |
| ARINC Output Impedance | $Z_{OUT}$ | | | | | |
| TXOUT pins | | | | 37.5 | | Ohms |
| AMP pins | | | | 5 | | Ohms |
| ARINC Output Tri-State Current | $I_{OZ}$ | TX0IN = TX1IN = $V_{LOGIC}$<br>−5.5V < $V_{OUT}$ < +5.5V | -1.0 | 0 | +1.0 | µA |

**Note 1:** TXAOUT and/or TXBOUT shorted to each other or ground. AMPA and/or AMPB shorted to each other or ground (assumes external resistors are connected to AMPA and AMPB to comply with ARINC 429 37.5 Ohm output resistance requirement).

**Note 2:** Estimate junction temperature using Theta JB or Theta JA values available on Holt's website, www.holtic.com. $T_J \leq T_{JMAX}$.

**Note 3:** In addition, external resistors are connected to AMPA and AMPB to comply with ARINC 429 37.5 Ohm output resistance requirement

## Table 4. Converter Characteristics

$V_{DDA}$ = $V_{LOGIC}$ = [+3.0V, +3.6], $T_A$ = Operating Temperature Range (unless otherwise stated)

| Parameters | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Start-up transient ($V_{DD2+}$, $V_{DD2-}$) | $t_{START}$ | | - | - | 10 | ms |
| Operating Switching Frequency | $f_{sw}$ | | - | 650 | - | kHz |
| Worst case maximum voltage doubler output | $V_{DD2+(max)}$ | $V_{DDA}$ = 3.6V. T = −55°C. Open load. | | | 6.6 | V |
| **DC/DC convertor capacitor recommendations.**<br>**For optimum performance use typical (not min.) values. For EMC compliance, see AN-135.** | | | | | | |
| Ratio of bulk storage to fly-back capacitors | $C_{OUT}$ / $C_{FLY}$ | | 2.2 | 10 | | |
| Fly-back capacitor<br>(Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.). | $C_{FLY}$<br>$C_{FLY(ESR)}$ | $C_{OUT}$ / $C_{FLY}$ >= 10<br>[0.5, 1.0]Mhz | 1.0 | 4.7 | -<br>500 | µF<br>mΩ |
| Bulk storage capacitor<br>(Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.). | $C_{OUT}$<br>$C_{OUT(ESR)}$ | $C_{OUT}$ / $C_{FLY}$ >= 10<br>[0.5, 1.0]Mhz | 2.2 | 47 | -<br>300 | µF<br>mΩ |
| By-pass capacitor<br>(Recommend ceramic cap, 10V min.). | $C_{SUPPLY}$ | $C_{SUPPLY}$ >= $C_{OUT}$ (connect from $V_{DDA}$ to GND) | | | | |

## Table 5. AC Electrical Characteristics

$V_{DDA}$ = $V_{LOGIC}$ = [+3.0V, +3.6], $T_A$ = Operating Temperature Range (unless otherwise stated)

| Parameters | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Line Driver Propogation Delay | | defined in Figure 2, no load | | | | |
| Output high to low | $t_{phlx}$ | | - | 500 | - | ns |
| Output low to high | $t_{plhx}$ | | - | 500 | - | ns |
| Line Driver Transition Times | | | | | | |
| High Speed | | SLP = $V_{LOGIC}$ | | | | |
| Output high to low | $t_{fx}$ | | 1.0 | 1.5 | 2.0 | µs |
| Output low to high | $t_{rx}$ | | 1.0 | 1.5 | 2.0 | µs |
| Low Speed | | SLP = GNDL | | | | |
| Output high to low | $t_{fx}$ | | 5.0 | 10.0 | 15.0 | µs |
| Output low to high | $t_{rx}$ | | 5.0 | 10.0 | 15.0 | µs |
| Input Capacitance (Logic)[1] | $C_{IN}$ | | - | - | 10 | pF |
| Output Capacitance (Tri-state)[1] | $C_{OUT}$ | TX0IN = TX1IN = $V_{LOGIC}$ | - | - | 10 | pF |

Note 1: Guaranteed but not tested

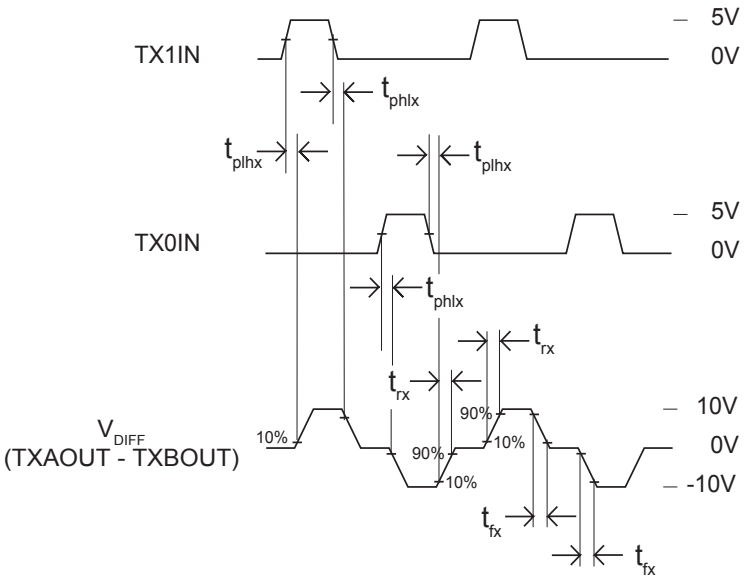



Figure 2. Line Driver Timing

## ORDERING INFORMATION

**HI - 8598Px x x (Plastic)**

| PART NUMBER | LEAD FINISH |
|---|---|
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|---|---|---|---|
| I | -40°C to +85°C | I | No |
| T | -55°C to +125°C | T | No |
| M | -55°C to +125°C | M | Yes |

| PART NUMBER | PACKAGE DESCRIPTION |
|---|---|
| 8598PS | 18 PIN PLASTIC SMALL OUTLINE - WB SOIC (18HW) |

## REVISION HISTORY

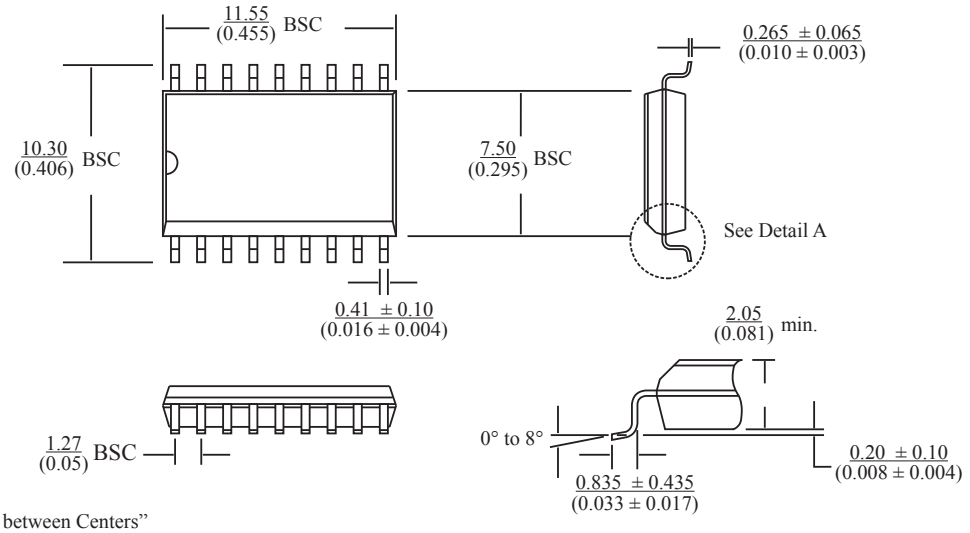
| Revision | Date | Description of Change |
|---|---|---|
| DS8598, Rev. New | 09/01/2021 | Initial Release. |
| Rev. A | 12/01/2023 | Clarify Input Current values on TX1IN, TX0IN and SLP pins. |

## PACKAGE DIMENSIONS

### 18-PIN PLASTIC SMALL OUTLINE (SOIC) - WB
(Wide Body)

*millimeters (inches)*

Package Type: 18HW




BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)