

# SNx4HCT240 Octal Buffers and Line Drivers With 3-State Outputs

## 1 Features

- Operating voltage range of 4.5V to 5.5V
- High-current outputs drive up to 15 LSTTL loads
- Low power consumption, 80 $\mu$ A max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ mA output drive at 5V
- Low input current of 1 $\mu$ A max
- Inputs are TTL-voltage compatible
- 3-state outputs drive bus lines or buffer memory address registers

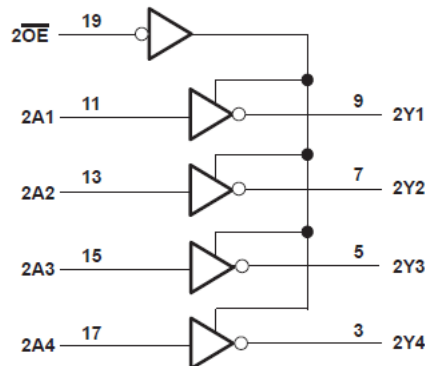
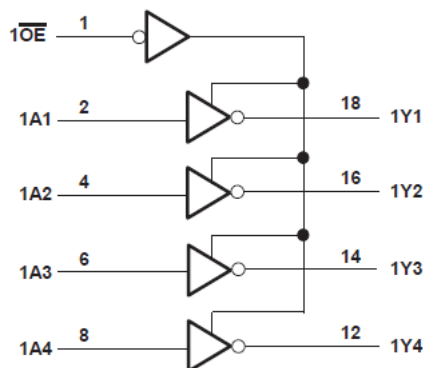
## 2 Description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT240 devices are organized as two 4-bit buffers/drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

### Device Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|-------------|------------------------|-----------------------------|--------------------------|
| SN74HCT240  | DGS (VSSOP, 20)        | 5.1mm × 4.9mm               | 5.1mm × 3mm              |
|             | DW (SOIC, 20)          | 12.80mm × 10.3mm            | 12.80mm × 7.50mm         |
|             | PDIP (20)              | 24.33mm × 9.4mm             | 24.33mm × 6.35mm         |
|             | NS (SOP, 20)           | 12.6mm × 7.8mm              | 12.6mm × 5.3mm           |
|             | PW (TSSOP, 20)         | 6.50mm × 6.4mm              | 6.50mm × 4.40mm          |
| SN54HCT240  | J (CDIP, 20)           | 24.2mm × 7.62mm             | 24.2 mm × 6.92mm         |
|             | FK (LCCC, 20)          | 8.9mm × 8.9mm               | 8.9mm × 8.9mm            |

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



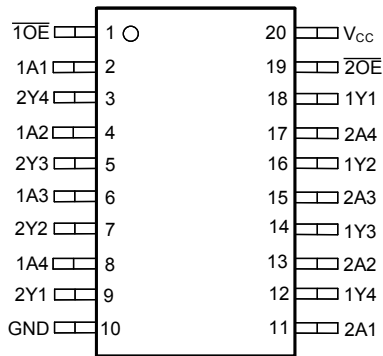
Functional Block Diagram



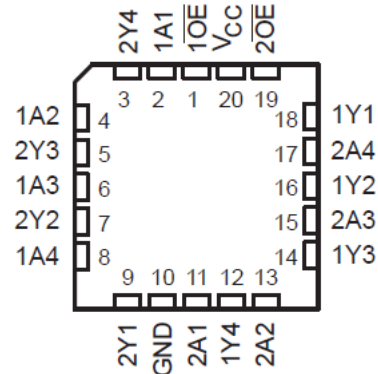
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### 3 Pin Configuration and Functions



**J, DGS, DW, N, NS, or PW package**  
**20-Pin CDIP, SOIC, PDIP, NS, or TSSOP**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**

| NAME <sup>(1)</sup> | PIN | TYPE | DESCRIPTION     |
|---------------------|-----|------|-----------------|
| 1OE                 | 1   | I    | Output enable 1 |
| 1A1                 | 2   | I    | 1A1 input       |
| 2Y4                 | 3   | O    | 2Y4 output      |
| 1A2                 | 4   | I    | 1A2 input       |
| 2Y3                 | 5   | O    | 2Y3 output      |
| 1A3                 | 6   | I    | 1A3 input       |
| 2Y2                 | 7   | O    | 2Y2 output      |
| 1A4                 | 8   | I    | 1A4 input       |
| 2Y1                 | 9   | O    | 2Y1 output      |
| GND                 | 10  | —    | Ground pin      |
| 2A1                 | 11  | I    | 2A1 input       |
| 1Y4                 | 12  | O    | 1Y4 output      |
| 2A2                 | 13  | I    | 2A2 input       |
| 1Y3                 | 14  | O    | 1Y3 output      |
| 2A3                 | 15  | I    | 2A3 input       |
| 1Y2                 | 16  | O    | 1Y2 output      |
| 2A4                 | 17  | I    | 2A4 input       |
| 1Y1                 | 18  | O    | 1Y1 output      |
| 2OE                 | 19  | I    | Output enable 2 |
| VCC                 | 20  | —    | Power pin       |

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   | MIN  | MAX | UNIT |
|------------------|---|--|-----|------|
| V <sub>CC</sub>  | Supply voltage range                              | -0.5   | 7   | V    |
| I <sub>IK</sub>  | Input clamp current <sup>(2)</sup>                | V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> | ±20 | mA   |
| I <sub>OK</sub>  | Output clamp current <sup>(2)</sup>               | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> | ±20 | mA   |
| I <sub>O</sub>   | Continuous output current                         | V <sub>O</sub> = 0 to V <sub>CC</sub>                  | ±35 | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |  | ±70 | mA   |
| T <sub>J</sub>   | Junction temperature                              |  | 150 | °C   |
| T <sub>stg</sub> | Storage temperature range                         | -65  | 150 | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                 | SN54HCT240                       |     |                 | SN74HCT240 |     |                 | UNIT |
|-----------------|---------------------------------|----------------------------------|-----|-----------------|------------|-----|-----------------|------|
|                 |                                 | MIN                              | NOM | MAX             | MIN        | NOM | MAX             |      |
| V <sub>CC</sub> | Supply voltage                  | 4.5                              | 5   | 5.5             | 4.5        | 5   | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage        | V <sub>CC</sub> = 4.5 V to 5.5 V |     | 2               | 2          |     |                 | V    |
| V <sub>IL</sub> | Low-level input voltage         | V <sub>CC</sub> = 4.5 V to 5.5 V |     |                 |            | 0.8 |                 | V    |
| V <sub>I</sub>  | Input voltage                   | 0                                |     | V <sub>CC</sub> | 0          |     | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                  | 0                                |     | V <sub>CC</sub> | 0          |     | V <sub>CC</sub> | V    |
| Δt/Δv           | Input transition rise/fall time |                                  |     | 500             |            |     | 500             | ns   |
| T <sub>A</sub>  | Operating free-air temperature  | -55                              |     | 125             | -40        |     | 85              | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 4.3 Thermal Information

| THERMAL METRIC        |   | DGS (VSSOP) | DW (SOIC) | N (PDIP) | NS (SOP) | PW (TSSOP) | UNIT |
|-----------------------|---|-------------|-----------|----------|----------|------------|------|
|                       |   | 20 PINS     | 20 PINS   | 20 PINS  | 20 PINS  | 20 PINS    |      |
| R <sub>θJA</sub>      | Junction-to-ambient thermal resistance <sup>(1)</sup> | 130.6       | 109.1     | 84.6     | 113.4    | 131.8      | °C/W |
| R <sub>θJC(top)</sub> | Junction-to-case (top) thermal resistance             | 68.7        | 76        | 72.5     | 78.6     | 72.2       | °C/W |
| R <sub>θJB</sub>      | Junction-to-board thermal resistance                  | 85.4        | 77.6      | 65.3     | 78.4     | 82.8       | °C/W |
| ψ <sub>JT</sub>       | Junction-to-top characterization parameter            | 10.5        | 51.5      | 55.3     | 47.1     | 21.5       | °C/W |
| ψ <sub>JB</sub>       | Junction-to-board characterization parameter          | 85.0        | 77.1      | 65.2     | 78.1     | 82.4       | °C/W |
| R <sub>θJC(bot)</sub> | Junction-to-case (bottom) thermal resistance          | N/A         | N/A       | N/A      | N/A      | N/A        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

#### 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS  |                          | V <sub>CC</sub> | T <sub>A</sub> = 25°C |       |      | SN54HCT240 |       | SN74HCT240 |     | UNIT |
|---------------------------------|--|--------------------------|-----------------|-----------------------|-------|------|------------|-------|------------|-----|------|
|                                 |  |                          |                 | MIN                   | TYP   | MAX  | MIN        | MAX   | MIN        | MAX |      |
| V <sub>OH</sub>                 | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>  | I <sub>OH</sub> = -20 μA | 4.5 V           | 4.4                   | 4.499 |      | 4.4        |       | 4.4        | V   |      |
|                                 |  | I <sub>OH</sub> = -6 mA  |                 | 3.98                  | 4.3   |      | 3.7        | 3.84  |            |     |      |
| V <sub>OL</sub>                 | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>  | I <sub>OL</sub> = 20 μA  | 4.5 V           |                       | 0.001 | 0.1  |            | 0.1   | 0.1        | V   |      |
|                                 |  | I <sub>OL</sub> = 6 mA   |                 |                       | 0.17  | 0.26 |            | 0.4   | 0.33       |     |      |
| I <sub>I</sub>                  | V <sub>I</sub> = V <sub>CC</sub> or 0  |                          | 5.5 V           |                       | ±0.1  | ±100 |            | ±1000 | ±1000      | nA  |      |
| I <sub>OZ</sub>                 | V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> |                          | 5.5 V           |                       | ±0.01 | ±0.5 |            | ±10   | ±5         | μA  |      |
| I <sub>CC</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0                                  |                          | 5.5 V           |                       |       | 8    |            | 160   | 80         | μA  |      |
| ΔI <sub>CC</sub> <sup>(1)</sup> | One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>                          |                          | 5.5 V           |                       | 1.4   | 2.4  |            | 3     | 2.9        | mA  |      |
| C <sub>i</sub>                  |  |                          | 4.5 V to 5.5 V  |                       | 3     | 10   |            | 10    | 10         | pF  |      |

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

#### 4.5 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Figure 5-1](#))

| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT240 |     | SN74HCT240 |     | UNIT |
|------------------|-----------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                  |                 |             |                 | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub>  | A               | Y           | 4.5 V           |                       | 13  | 25  |            | 37  |            | 32  | ns   |
|                  |                 |             | 5.5 V           |                       | 12  | 23  |            | 33  |            | 29  |      |
| t <sub>en</sub>  | $\overline{OE}$ | Y           | 4.5 V           |                       | 21  | 35  |            | 53  |            | 44  | ns   |
|                  |                 |             | 5.5 V           |                       | 19  | 32  |            | 48  |            | 40  |      |
| t <sub>dis</sub> | $\overline{OE}$ | Y           | 4.5 V           |                       | 19  | 35  |            | 53  |            | 44  | ns   |
|                  |                 |             | 5.5 V           |                       | 18  | 32  |            | 48  |            | 40  |      |
| t <sub>t</sub>   |                 | Y           | 4.5 V           |                       | 8   | 12  |            | 18  |            | 15  | ns   |
|                  |                 |             | 5.5 V           |                       | 7   | 11  |            | 16  |            | 14  |      |

#### 4.6 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 150 pF (unless otherwise noted) (see [Figure 5-1](#))

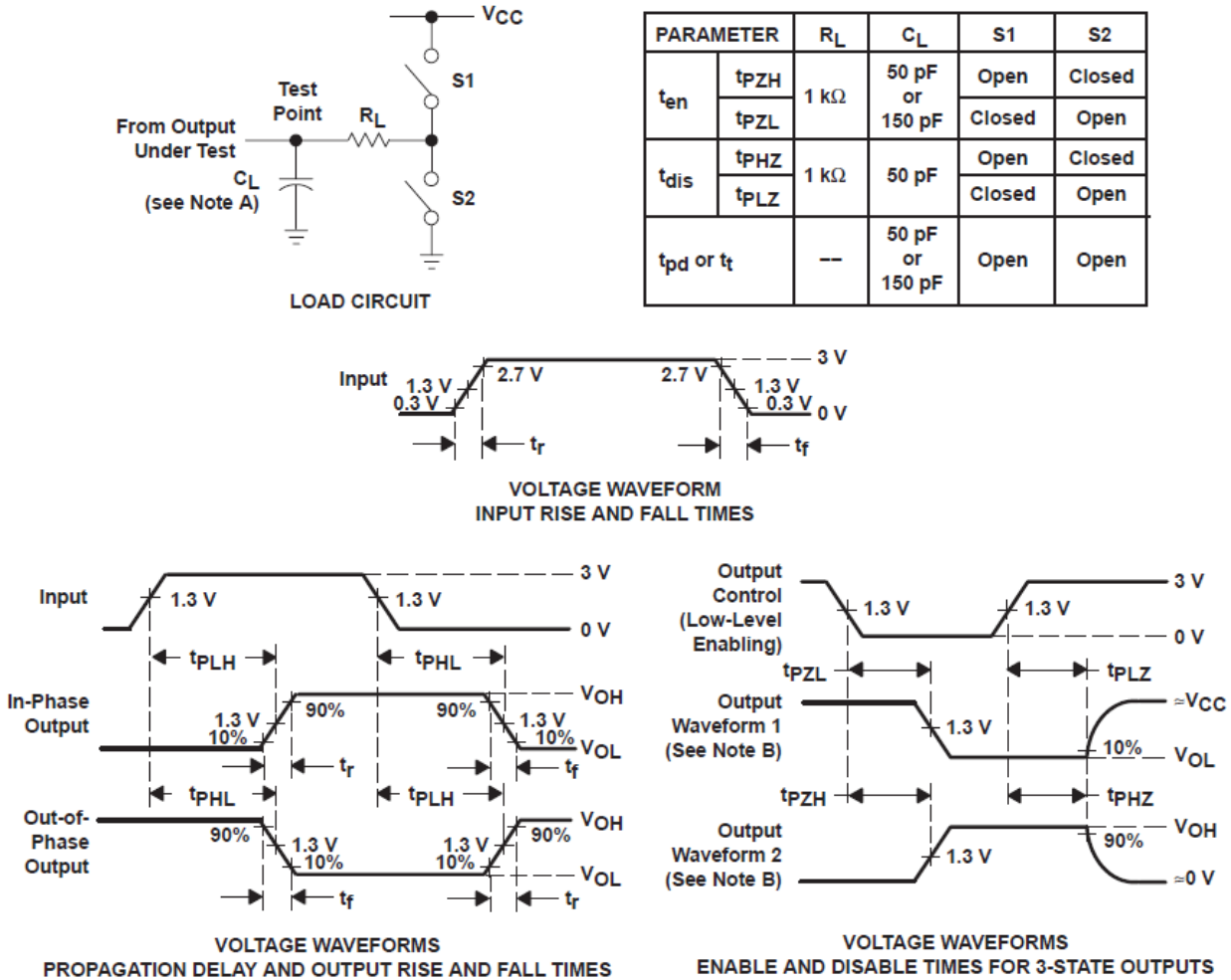
| PARAMETER       | FROM (INPUT)    | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT240 |     | SN74HCT240 |     | UNIT |
|-----------------|-----------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                 |                 |             |                 | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub> | A               | Y           | 4.5 V           |                       | 20  | 42  |            | 63  |            | 53  | ns   |
|                 |                 |             | 5.5 V           |                       | 19  | 38  |            | 56  |            | 48  |      |
| t <sub>en</sub> | $\overline{OE}$ | Y           | 4.5 V           |                       | 25  | 52  |            | 79  |            | 65  | ns   |
|                 |                 |             | 5.5 V           |                       | 22  | 47  |            | 71  |            | 59  |      |
| t <sub>t</sub>  |                 | Y           | 4.5 V           |                       | 17  | 42  |            | 63  |            | 53  | ns   |
|                 |                 |             | 5.5 V           |                       | 14  | 38  |            | 57  |            | 48  |      |

#### 4.7 Operating Characteristics

T<sub>A</sub> = 25°C

| PARAMETER       | TEST CONDITIONS               | TYP | UNIT |
|-----------------|-------------------------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance | 40  | pF   |

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

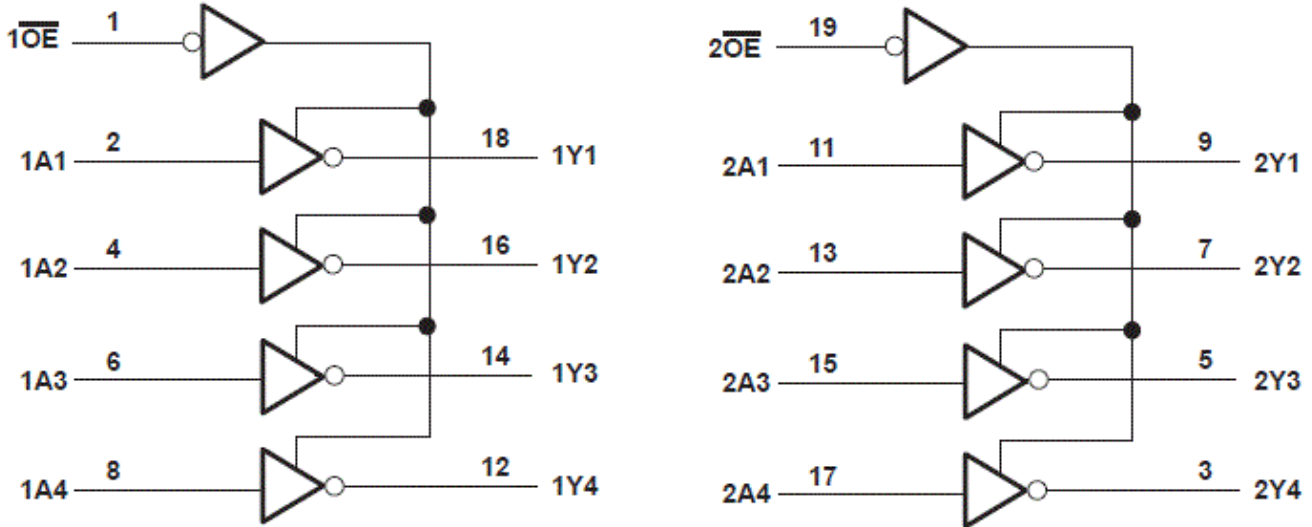
**Figure 5-1. Load Circuit and Voltage Waveforms**

## 6 Detailed Description

### 6.1 Overview

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT240 devices are organized as two 4-bit buffers/drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

### 6.2 Functional Block Diagram



### 6.3 Device Functional Modes

**Table 6-1. Function Table (Each Buffer/Driver)**

| INPUTS |   | OUTPUT |
|--------|---|--------|
| OE     | A | Y      |
| L      | H | L      |
| L      | L | H      |
| H      | X | Z      |

## 7 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1 $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1 $\mu$ F and 1 $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.



## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (May 2022) to Revision H (August 2024)  | Page |
|---|------|
| • Added DGS package to <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, and <i>Thermal Information</i> table..... | 1    |
| • Added <i>Pin Functions</i> table.....   | 3    |
| • Added <i>Application and Implementation</i> section.....  | 8    |

| Changes from Revision F (February 2022) to Revision G (May 2022)   | Page |
|--|------|
| • Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6, NS was 60 is now 113.4, PW was 83 is now 131.8..... | 4    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)        | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------|-------------------------|
| 85505012A        | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 85505012A<br>SNJ54HCT<br>240FK | <a href="#">Samples</a> |
| 8550501RA        | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 8550501RA<br>SNJ54HCT240J      | <a href="#">Samples</a> |
| JM38510/65753BRA | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65753BRA           | <a href="#">Samples</a> |
| M38510/65753BRA  | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65753BRA           | <a href="#">Samples</a> |
| SN54HCT240J      | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54HCT240J                    | <a href="#">Samples</a> |
| SN74HCT240DGSR   | ACTIVE        | VSSOP        | DGS             | 20   | 5000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | HT240                          | <a href="#">Samples</a> |
| SN74HCT240DW     | OBSOLETE      | SOIC         | DW              | 20   |             | TBD              | Call TI                              | Call TI              | -40 to 85    | HCT240                         |                         |
| SN74HCT240DWR    | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT240                         | <a href="#">Samples</a> |
| SN74HCT240DWRE4  | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT240                         | <a href="#">Samples</a> |
| SN74HCT240N      | ACTIVE        | PDIP         | N               | 20   | 20          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74HCT240N                    | <a href="#">Samples</a> |
| SN74HCT240NSR    | ACTIVE        | SO           | NS              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT240                         | <a href="#">Samples</a> |
| SN74HCT240PW     | OBSOLETE      | TSSOP        | PW              | 20   |             | TBD              | Call TI                              | Call TI              | -40 to 85    | HT240                          |                         |
| SN74HCT240PWR    | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT240                          | <a href="#">Samples</a> |
| SN74HCT240PWT    | OBSOLETE      | TSSOP        | PW              | 20   |             | TBD              | Call TI                              | Call TI              | -40 to 85    | HT240                          |                         |
| SNJ54HCT240FK    | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 85505012A<br>SNJ54HCT<br>240FK | <a href="#">Samples</a> |
| SNJ54HCT240J     | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 8550501RA<br>SNJ54HCT240J      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HCT240, SN74HCT240 :**

● Catalog : [SN74HCT240](#)

● Military : [SN54HCT240](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

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