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SEMICONDUCTOR™

January 2000
Revised June 2005

74VCX162373

Low Voltage 16-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

General Description

The VCX162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The VCX162373 is also designed with 26Ω resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceivers/transmitters.

The 74VCX162373 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX162373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- t_{PD} (I_n to O_n)
  - 3.3 ns for 3.0V to 3.6V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static drive (I_{OH}/I_{OL})
  - ±12 mA @ 3.0V V_{CC}
- Uses proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Note 1: To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Ordering Number	Package Number	Package Description
74VCX162373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol
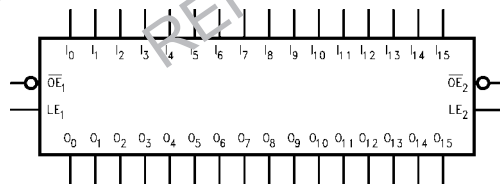
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

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Connection Diagram

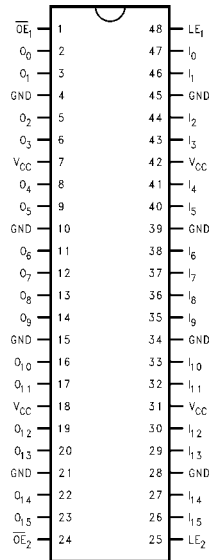|			
$\overline{OE}_1$	1	48	LE_1
O_0	2	47	I_0
O_1	3	46	I_1
GND	4	45	GND
O_2	5	44	I_2
O_3	6	43	I_3
V_{CC}	7	42	V_{CC}
O_4	8	41	I_4
O_5	9	40	I_5
GND	10	39	GND
O_6	11	38	I_6
O_7	12	37	I_7
O_8	13	36	I_8
O_9	14	35	I_9
GND	15	34	GND
O_{10}	16	33	I_{10}
O_{11}	17	32	I_{11}
V_{CC}	18	31	V_{CC}
O_{12}	19	30	I_{12}
O_{13}	20	29	I_{13}
GND	21	28	GND
O_{14}	22	27	I_{14}
O_{15}	23	26	I_{15}
$\overline{OE}_2$	24	25	LE_2

Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

| Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance
O_0 = Previous O_0 before HIGH-to-LOW of Latch Enable

Functional Description

The 74VCX162373 contains sixteen D-type latches with 3-STATE outputs. The device is byte operable with each byte functioning identically but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on LE_n. The 3-STATE outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram
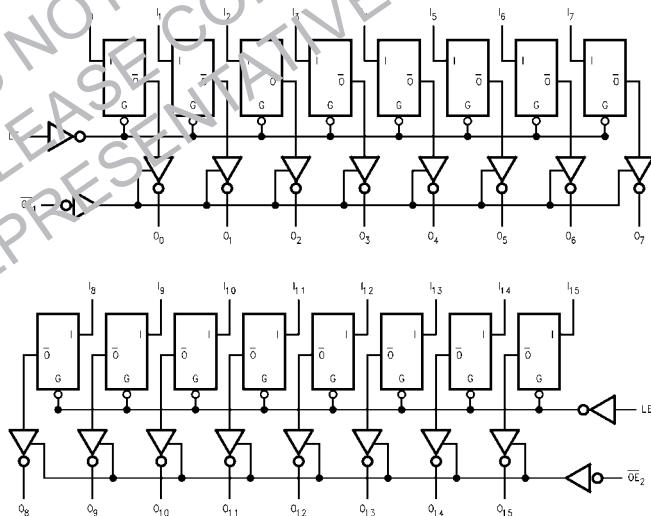
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_CC)	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	−0.5V to +4.6V
Outputs Active (Note 3)	−0.5V to V_CC +0.5V
DC Input Diode Current (I_IK) V_I < 0V	−50 mA
DC Output Diode Current (I_OK)	
V_O < 0V	−50 mA
V_O > V_CC	+50 mA
DC Output Source/Sink Current	
(I_OH/I_OL)	±50 mA
DC V_CC or GND Current per	
Supply Pin (I_CC or GND)	±100 mA
Storage Temperature Range (T_STG)	−65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	−0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_CC
Output in "OFF" State	0.0V to 3.6V
Output Current in I_OH/I_OL	
V_CC = 3.0V to 3.6V	± nA
V_CC = 2.3V to 2.7V	±8
V_CC = 1.65V to 2.3V	±3
V_CC = 1.4V to 1.6V	mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
V_IN = 0.8V to 2.0V, V_CC = 3.0	10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_OL Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_CC (V)	Min	Max	Units
V_IH	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_CC		
			1.4 - 1.6	0.65 x V_CC		
V_IL	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_CC	
			1.4 - 1.6		0.35 x V_CC	
V_OH	HIGH Level Output Voltage	I_OH = −100 μA	2.7 - 3.6	V_CC - 0.2		V
		I_OH = −6 mA	2.7	2.2		
		I_OH = −8 mA	3.0	2.4		
		I_OH = −12 mA	3.0	2.2		
		I_OH = −100 μA	2.3 - 2.7	V_CC - 0.2		V
		I_OH = −4 mA	2.3	2.0		
		I_OH = −6 mA	2.3	1.8		
		I_OH = −8 mA	2.3	1.7		
		I_OH = −100 μA	1.65 - 2.3	V_CC - 0.2		
		I_OH = −3 mA	1.65	1.25		
		I_OH = −100 μA	1.4 - 1.6	V_CC - 0.2		
		I_OH = −1 mA	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	Min	Max	Units
V_OL	LOW Level Output Voltage	I_OL = 100 μA	2.7 - 3.6		0.2	
		I_OL = 6 mA	2.7		0.4	
		I_OL = 8 mA	3.0		0.55	
		I_OL = 12 mA	3.0		0.8	
		I_OL = 100 μA	2.3 - 2.7		0.2	V
		I_OL = 6 mA	2.3		0.4	
		I_OL = 8 mA	2.3			
		I_OL = 100 μA	1.65 - 2.3		0.2	
		I_OL = 3 mA	1.65			
		I_OL = 100 μA	1.4 - 1.6			
		I_OL = 1 mA	1.		0.35	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	1.4 - 3.		5.0	μA
I_OZ	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V, V_I = V_IH or V_IL	1.4 - 3.6		±10.0	μA
I_OFF	Power-OFF Leakage Current	0 ≤ (V_I, V_O) ≤ 3.6V	0		10.0	μA
I_CC	Quiescent Supply Current	V_I = V_CC or GND	1. 3.6		20.0	μA
		V_CC ≤ (V_I, V_O) ≤ 3.6V (Note 5)	1.4 - 3.6		±20.0	μA
ΔI_CC	Increase in I_CC per Input	V_IH = V_CC −0.6V	.7 - 3.6		750	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Figure Number
t_PHL t_PLH	Propagation Delay LE to O_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.6	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.9		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t_PHL t_PLH	Propagation Delay I_n to O_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.3	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.5		
			1.8 ± 0.15	1.5	9.0		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	18.0		Figures 7, 8
t_PZL t_PZH	Output Enable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.9	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	5.4		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t_PLZ t_PHZ	Output Disable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	4.0	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.4		
			1.8 ± 0.15	1.5	7.9		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	15.8		Figures 7, 9, 10
t_S	Setup Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	3.0			Figures 6, 7
t_H	Hold Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	1.0		ns	Figures 1, 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	2.0			Figures 6, 7

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$ = −40°C to +85°C Min	T$_A$ = −40°C to +85°C Max	Units	Figure Number
t$_W$	Pulse Width	C$_L$ = 30 pF, R$_L$ = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 5
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		C$_L$ = 15 pF, R$_L$ = 2kΩ	1.5 ± 0.1	4.0			Figures 5, 7
t$_{OSHL}$ t$_{OSLH}$	Output to Output Skew (Note 7)	C$_L$ = 30 pF, R$_L$ = 500Ω	3.3 ± 0.3		0.5		
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C$_L$ = 15 pF, R$_L$ = 2kΩ	1.5 ± 0.1		1.5		

Note 6: For C$_L$ = 50pF, add approximately 300 ps to the AC maximum specification.

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t$_{OSHL}$) or LOW-to-HIGH (t$_{OSLH}$).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$ = +25°C Typical	Units
V$_{OLP}$	Quiet Output Dynamic Peak V$_{OL}$	C$_L$ = 30 pF, V$_{IH}$ = V$_{CC}$, V$_{IL}$ = 0V	1.8	0.15	V
			2.5	0.25	
			3.3	0.35	
V$_{OLV}$	Quiet Output Dynamic Valley V$_{OL}$	C$_L$ = 30 pF, V$_{IH}$ = V$_{CC}$, V$_{IL}$ = 0V	1.8	−0.15	V
			2.5	−0.25	
			3.3	−0.35	
V$_{OHV}$	Quiet Output Dynamic Valley	C$_L$ = 30 pF, V$_{IH}$ = V$_{CC}$, V$_{IL}$ = 0V	1.8	1.55	V
			2.5	2.05	
			3.3	2.65	

Capacitance

Symbol	Parameter	Conditions	T$_A$ = +25°C Typical	Units
C$_{IN}$	Input Capacitance	V$_{CC}$ = 1.8V, 2.5V or 3.3V, V$_I$ = 0V or V$_{CC}$	6	pF
C$_{OUT}$	Output Capacitance	V$_I$ = 0V or V$_{CC}$, V$_{CC}$ = 1.8V, 2.5V or 3.3V	7	pF
	Power Dissipation Capacitance	V$_I$ = 0V or V$_{CC}$, f = 10 MHz, V$_{CC}$ = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V_{CC} 3.3V $\pm$ 0.3V to 1.8V $\pm$ 0.15V)
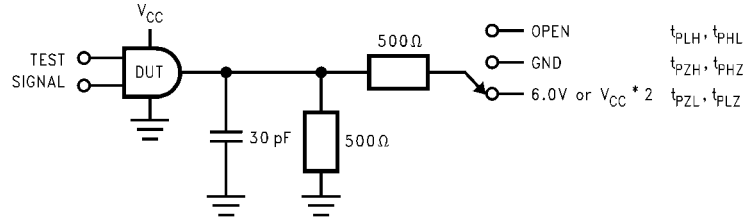
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 $\pm$ 0.3V; V_{CC} x 2 at V_{CC} = 2.5 $\pm$ 0.2V; 1.8V $\pm$ 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit
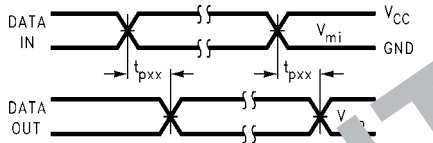
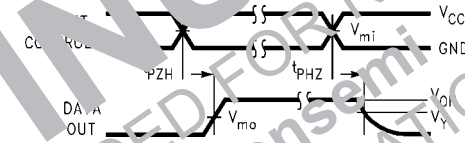**FIGURE 2. Waveform for Inverting and Non-Inverting Functions**

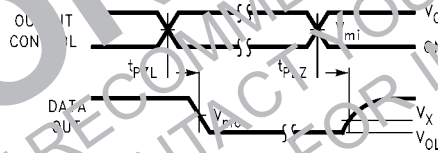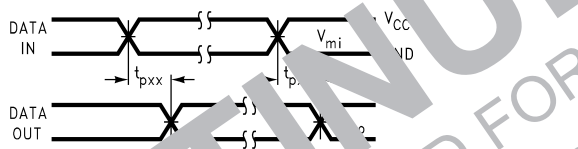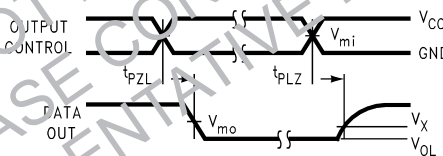**FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic**

FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic
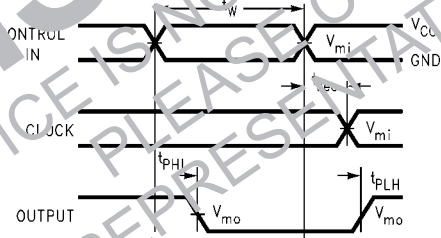
FIGURE 5. Propagation Delay, Pulse Width and t_{REC} Waveforms
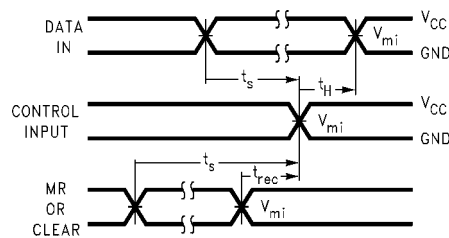
FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} +0.3V	V_{OL} +0.15V	V_{OL} +0.15V
V_Y	V_{OH} −0.3V	V_{OH} −0.15V	V_{OH} −0.15V

AC Loading and Waveforms (V$_{CC}$ 1.5V $\pm$ 0.1V)
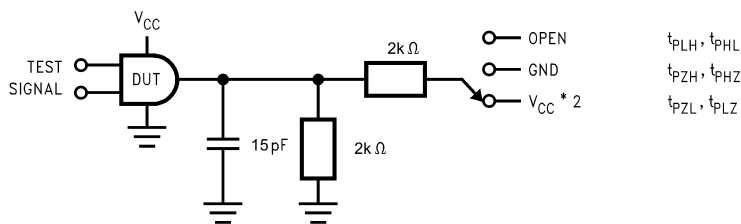
TEST	SWITCH
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	V$_{CC}$ x 2 at V$_{CC}$ = 1.5V $\pm$ 0.1V
t$_{PZH}$, t$_{PHZ}$	GND

FIGURE 7. AC Test Circuit

FIGURE 8. Waveform for Inverting and Non-Inverting Functions
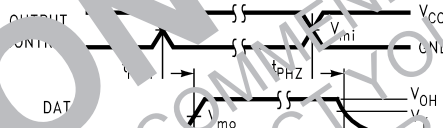
FIGURE 9. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

FIGURE 10. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

Symbol	V$_{CC}$
	1.5V $\pm$ 0.1V
V$_{mi}$	V$_{CC}$/2
V$_{mo}$	V$_{CC}$/2
V$_X$	V$_{OL}$ +0.1V
V$_Y$	V$_{OH}$ −0.1V

Physical Dimensions inches (millimeters) unless otherwise noted

MTD48REVC
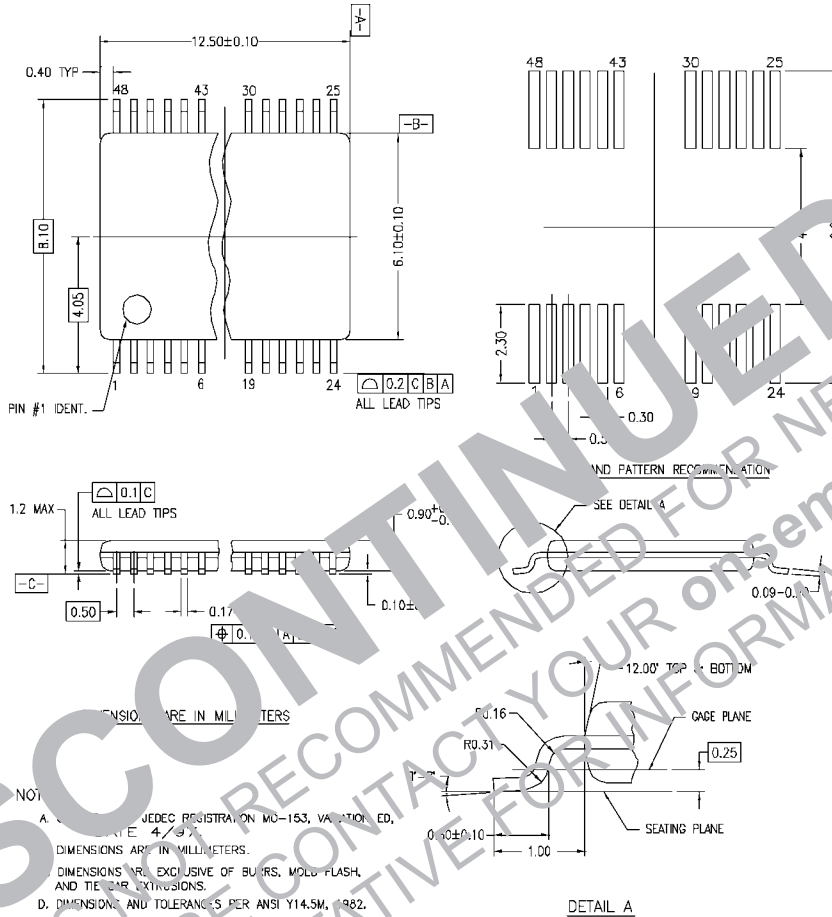
**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48**

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