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Approval Sheet

(產品承認書)

產品名稱	(Product)	WiFi Low Power Module
解決方案	(Solution)	Nordic nRF7002 QFN Package
產品型號	(Model No.)	**AN7002Q – P**
產品料號	(Part No.)	see *3.1 Order code*

Index

1. Overall introduction

Raytac's AN7002Q is a low power WiFi 6 module designed based on Nordic nRF7002 companion solution and it supports dual-band 2.4 GHz and 5 GHz band operation. The antenna ports are single-ended 50 Ω and it supports 20 MHz wide channels, 1x1 Single-Input Single-Output (SISO) operation and can deliver a PHY data rate of 86 Mbps (MCS7). AN7002Q series is a wireless module that adds low-power Wi-Fi 6 capabilities to another System on Chip (SoC), Microprocessor Unit (MPU), or Microcontroller Unit (MCU) host. AN7002Q is compatible with IEEE 802.11ax (also known as Wi-Fi 6) and with earlier standards IEEE 802.11 a/b/g/n/ac and which has been designed for IoT applications, and is ideal for adding modern Wi-Fi 6 capabilities to existing Bluetooth® Low Energy, Thread®, or Zigbee® systems.

It connects to the host SoC or MCU through a Serial Peripheral Interface (SPI) or Quad Serial Peripheral Interface (QSPI) serial interface (which can optionally be encrypted) and supports coexistence with other radio protocols through a dedicated 3-wire or 4-wire coexistence interface.

It supports Station and Wi-Fi Direct operation modes as well as Software Enabled Access Point (Soft AP) (Wi-Fi 4 operation only) and simultaneous station + soft AP/Wi-Fi Direct/station modes.

1.1. Features

1. Wi-Fi® 6 companion IC with integrated RF.
2. Supports IEEE 802.11 ax and earlier standards (IEEE 802.11 a/b/g/n/ac)
3. Supports Target Wake Time (TWT), Orthogonal Frequency Division Multiple Access (OFDMA), Basic Service Set (BSS) Coloring
4. Supports Wi-Fi CERTIFIED 6™, Wi-Fi CERTIFIED™, Wi-Fi Enhanced Open™
5. Supports WPA3™, WPA2™, WPA™ - Personal and Enterprise, Protected Management Frames
6. Supports WMM®, WMM - Power Save, Wi-Fi Agile Multiband™, Wi-Fi Direct®
7. Dual-band 2.4 GHz and 5 GHz operation in 1x1 (SISO) operation.
8. 3-wire or 4-wire coexistence interface and compatible with Raytac MDBT53 series module.

1.2. Application

- Internet of Things (IoT)
- Smart Home application
- Gateways and Border Routers
- Industrial IoT sensors and controllers
- Sports and Fitness sensor and monitor devices
- Wireless payment enabled devices
- Health monitor devices
- Wi-Fi locationing based on SSID scanning

1.3. General parameters

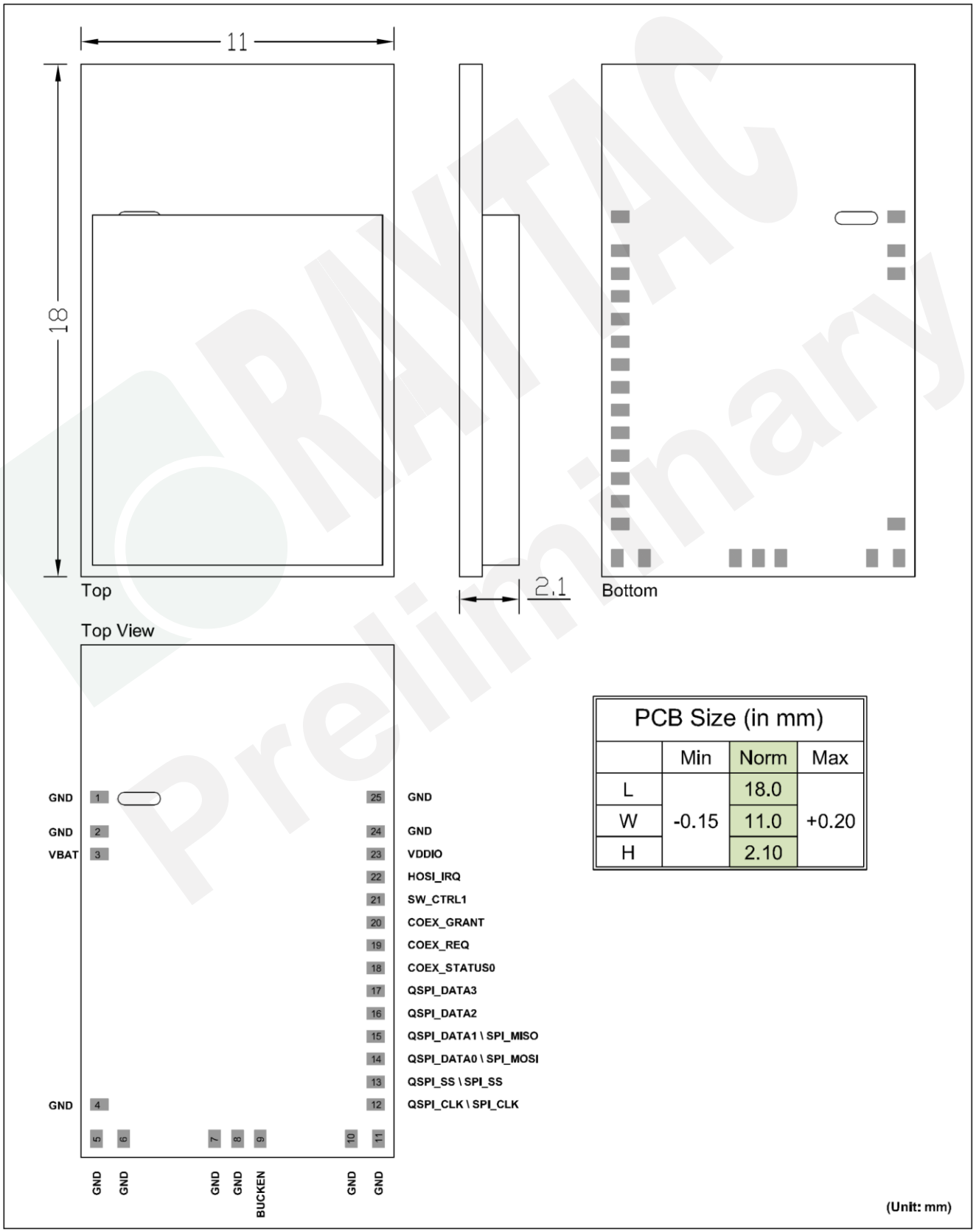
Model name	AN7002Q-P	
Dimension (L x W x H)	18 x 11 x 2.2mm	
Weight (g)	AN7002Q-P:0.79 (±0.02g)	
Interface	SPI or QSPI	
Supply voltage	2.9V to 4.5V	
Operating temperature	-40 to +85°C	
Support antenna	1 x 1 (SISO)	
RF channels	2.4G	Ch1-Ch14*
	5G	Ch36/40/44/48/52/56/60/64 Ch100/104/108/112/116/120/124/128/132/136/140 Ch149/153/157/161/165/169/173
IEEE WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax	

***Channel 14 Japan only with 11b modulation.**

2. Product dimension

2.1. PCB dimensions & pin indication

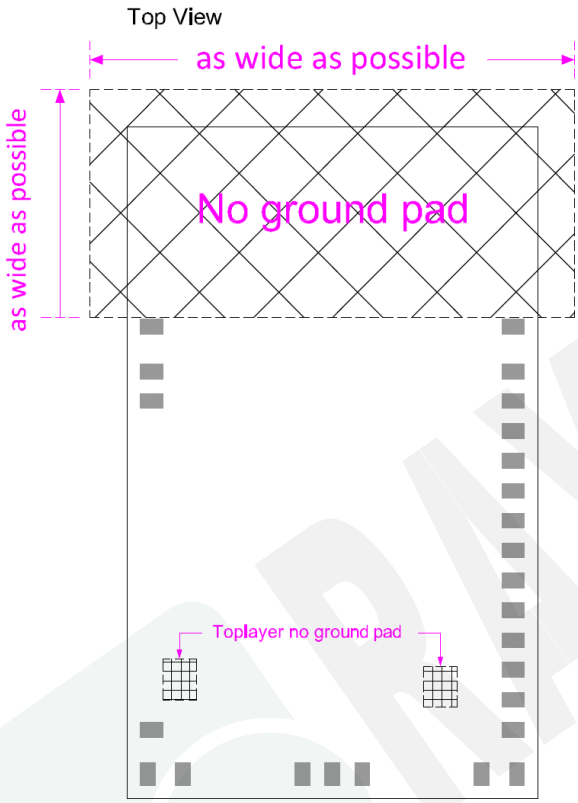
- **AN7002Q-P**

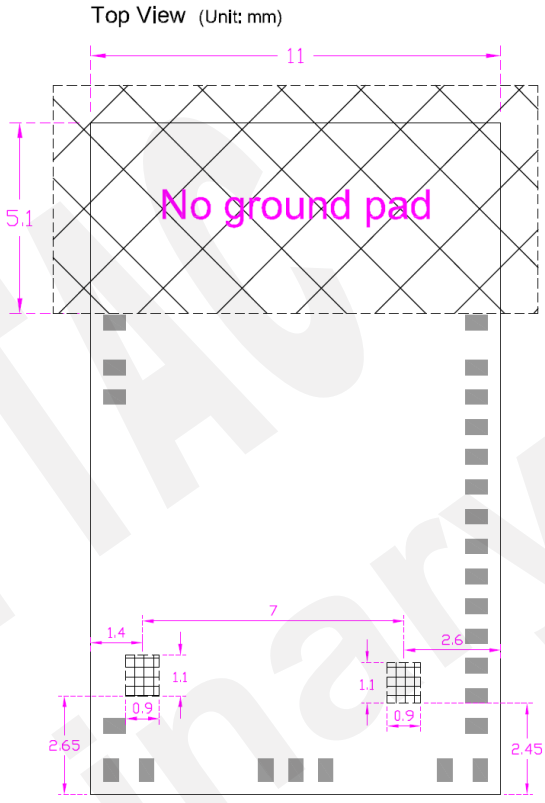


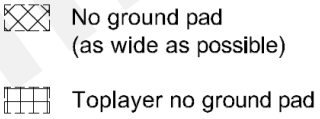
PCB Size (in mm)			
	Min	Norm	Max
L	-0.15	18.0	+0.20
W		11.0	
H		2.10	

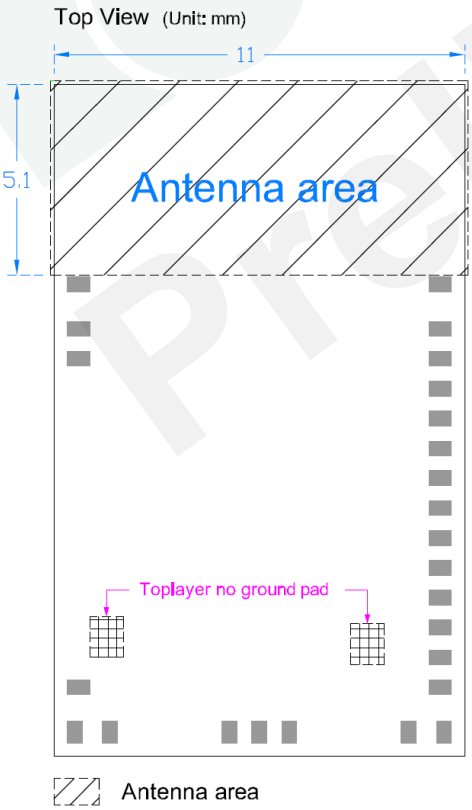
2.2. Recommended layout of solder pad

Graphs are all in Top View, Unit in mm.

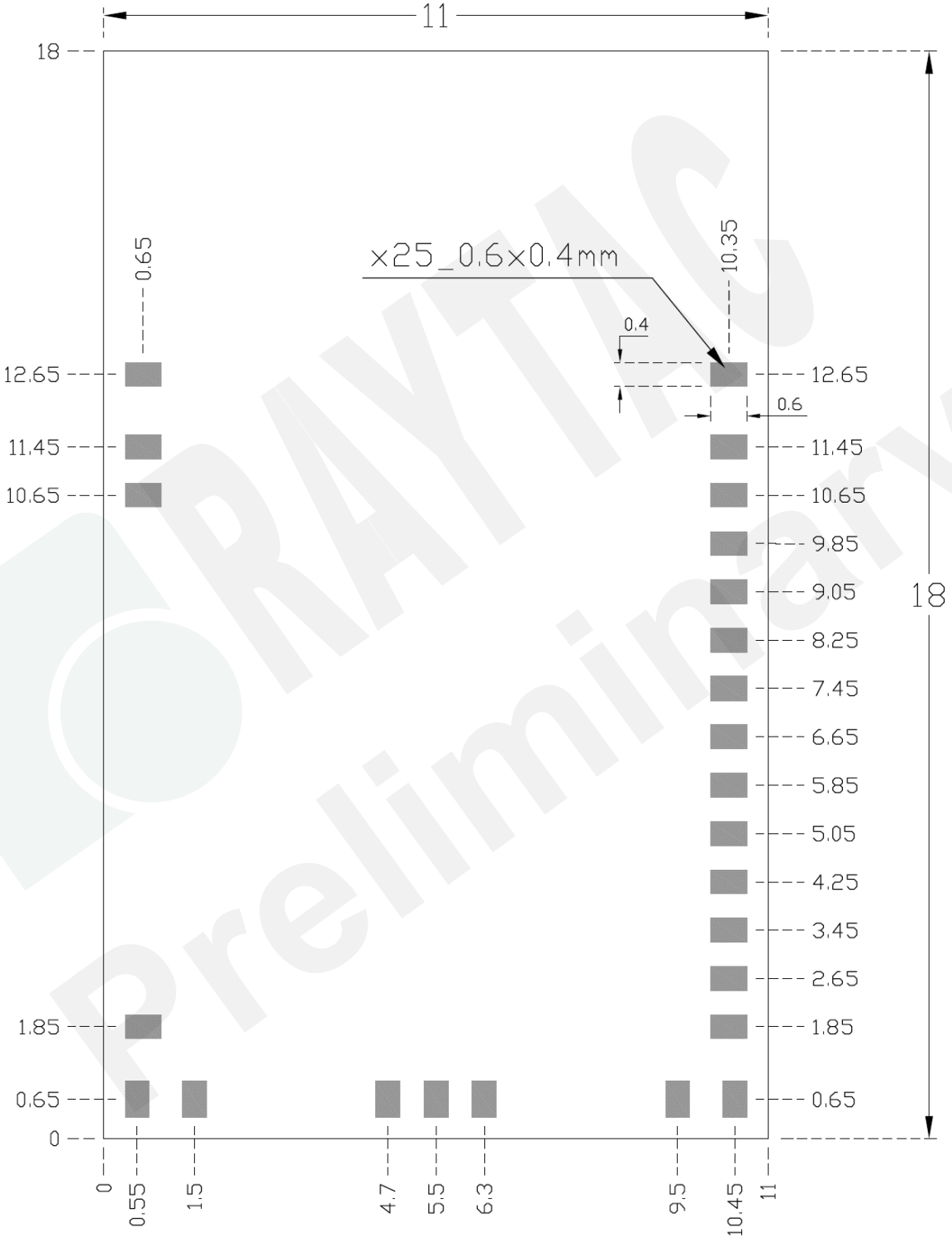








Top View (Unit: mm)



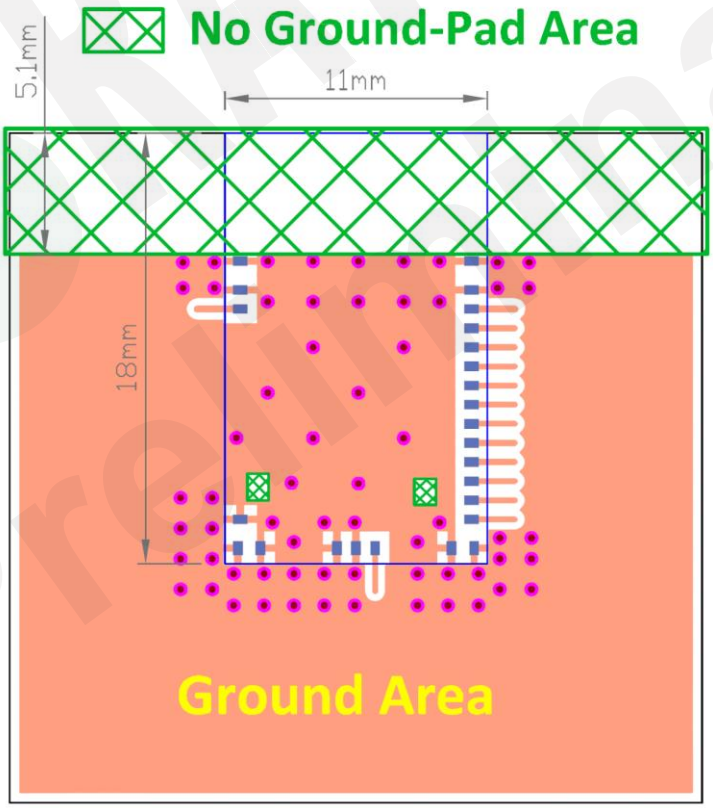
2.3. RF layout suggestion (aka keep-out area)

Make sure to keep the “No Ground Pad” as wider as you can regardless of the size of your PCB.

No Ground Pad should be included in the corresponding position of the antenna in **EACH LAYER**.

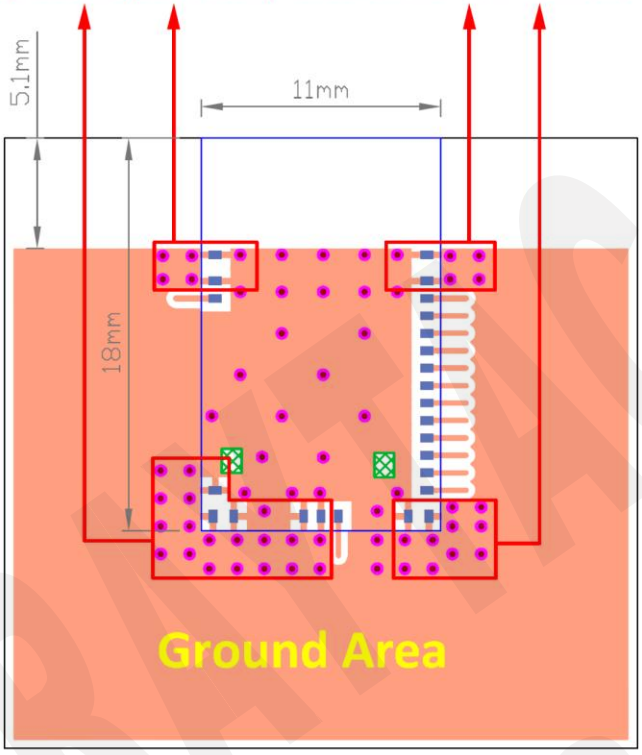
Place the module towards the edge of PCB to have better performance than placing it on the center.

Welcome to send us your layout in PDF for review at service@raytac.com or your contact at Raytac with title “Layout reviewing – Raytac Model No. – YOUR company’s name”.



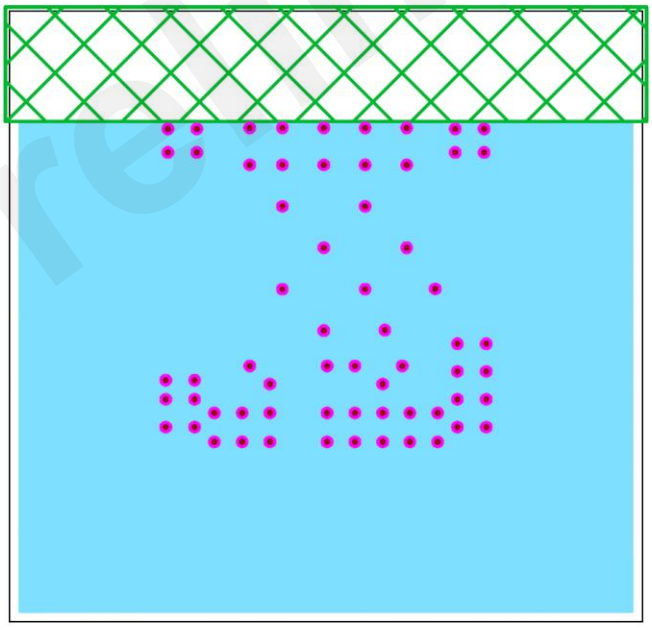
Top View

Please add via holes in GROUND area as many as possible, especially around the four corners.



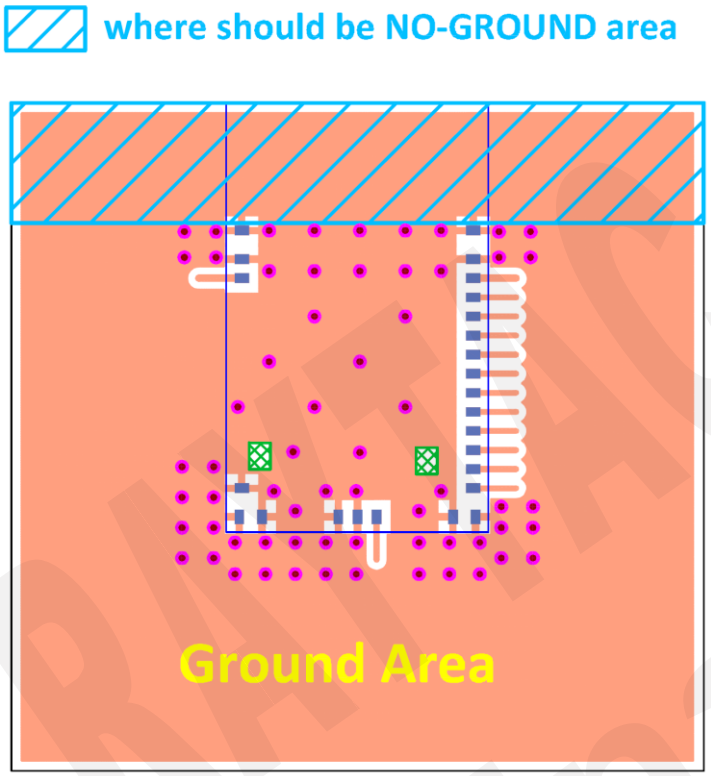
Top View

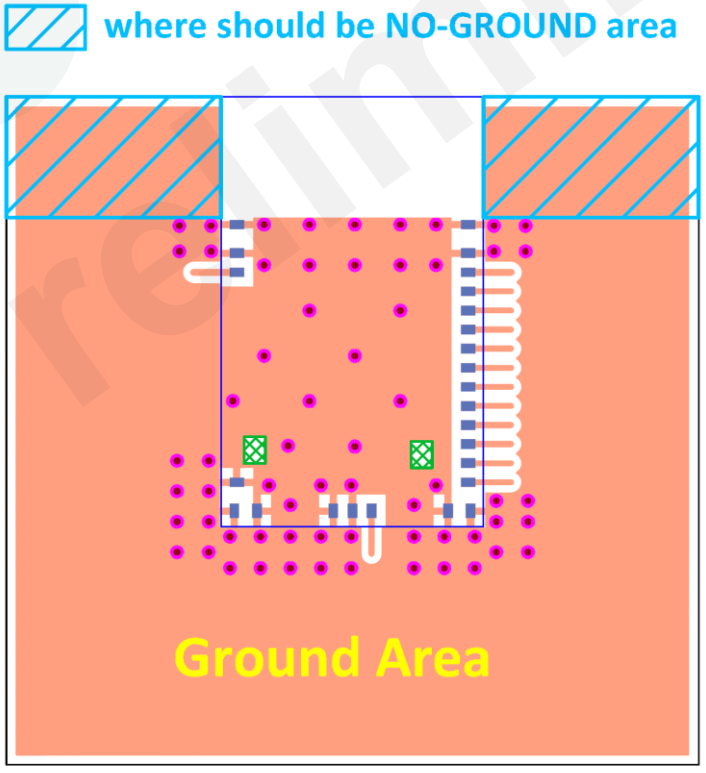
No Ground-Pad Area



Perpective View

Examples of “**NOT RECOMMENDED**” layout





2.4. Pin assignment

Pin No.	Name	Pin Function	Description
(1)(2)	**GND**	Power	Ground
(3)	**VBAT**	Power	
(4)(5)(6)(7)(8)	**GND**	Power	Ground
(9)	**BUCKEN**	Digital I/O	PWR IP enable pin
(10)(11)	**GND**	Power	Ground
(12)	**QSPI_CLK**	Digital I/O	QSIP Clock
	SPI_CLK	Digital I/O	SIP Clock
(13)	**QSPI_SS**	Digital I/O	QSIP Slave select
	SPI_SS	Digital I/O	SIP Slave select
(14)	**QSPI_DATD0**	Digital I/O	QSIP data
	SPI_MOSI	Digital I/O	SIP data
(15)	**QSPI_DATD1**	Digital I/O	QSIP data
	SPI_MISO	Digital I/O	SIP data
(16)	**QSPI_DATD2**	Digital I/O	QSIP data
(17)	**QSPI_DATD3**	Debug	QSIP data
(18)	**COEX_STATUS0**	Digital I/O	Coex interface
(19)	**COEX_REQ**	Reset	Coex interface
(20)	**COEX_GRANT**	Digital I/O	Coex interface
(21)	**SW_CTRL1**	Digital I/O	External switch control (4 wire coex interface)
(22)	**HOSI_IRQ**	Digital I/O	Host processor interrupt request
(23)	**VDDIO**	GND	I/O Power level
(24)(25)	**GND**	Power	Ground

3. Shipment packaging information

Model	Antenna	Photo
AN7002Q-P	PCB antenna	

3.1. Order code

Each model has two options of packaging. Please use following part no. when placing order to us.

Model	Tray	Tape & Reel
AN7002Q-P	W5-500A1-001	W5-500A1-001R

4. Specification

Any technical spec shall refer to Nordic's official documents as final reference. Contents below are from "nRF7002 Product Specification v1.1", please click to download full spec.

4.1. Absolute maximum ratings

	Min.	Max.	Unit
Supply voltages			
VBAT	-0.3	4.5	V
IOVDD	-0.3	3.6	V
I/O pin voltage			
$V_{I/O}$, IOVDD ≤3.3 V	-0.3	IOVDD + 0.3	V
$V_{I/O}$, IOVDD >3.3 V	-0.3	3.6	V
BUCKEN	-0.3	VBAT + 0.3	V
Radio			
RF input level		-10	dBm
Environmental QFN package			
Storage temperature	-40	125	°C
Moisture Sensitivity Level (MSL)		2	
ESD Human Body Model (HBM)		750	V
ESD Charged Device Model (CDM)		1000	V
Environmental WLCSP package			
Storage temperature	-40	125	°C
Moisture Sensitivity Level (MSL)		1	
ESD Human Body Model (HBM)		750	V
ESD Charged Device Model (CDM)		500	V

4.2. Recommended operating conditions

Symbol	Parameter	Min.	Nom.	Max.	Units
VBAT	VDD supply voltage	2.9	3.6	4.5	V
IOVDD	VDD supply voltage for IO pins	1.62	1.8	3.6	V
OTPVDD	VDD supply voltage for OTP memory (read mode)	1.62	1.8	1.98	V
OTPVDD	VDD supply voltage for OTP memory (write mode)	2.25	2.5	2.75	V
TA	Operating temperature	-40	25	85	°C

4.3. Electrical specifications

4.3.1. General characteristics

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$f_{OP,2.4GHz}$	Operating frequencies 2.4 GHz	2401		2495	MHz	
$f_{OP,5GHz}$	Operating frequencies 5 GHz	5170		5330	MHz	U-NII-1/U-NII-2A sub-bands
		5490		5730		U-NII-2C sub-band
		5735		5895		U-NII-3/U-NII-4 sub-bands
$f_{MOD,MIN}$	Minimum modulation rate		1DSSS			2.4 GHz
			6 Mbps			5 GHz
$f_{MOD,MAX}$	Maximum modulation rate		MCS7			
f_{TOL}	Crystal frequency tolerance at 25°C[1]			20	ppm	
$f_{STA,TEMP}$	Crystal frequency stability over temperature and aging			13	ppm	
C_{L_XO}	XO load capacitance		8		pF	
ESR_{XO}	Equivalent Series Resistance			100	ohm	
$t_{SHUTDOWN→ACTIVE}$	Startup time from shutdown state		400		ms	Depends on patch size and interface speed
$t_{SLEEP→ACTIVE}$	Startup time from sleep state		6.7		ms	

4.3.2. Current consumption

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$I_{RX,2.4GHz}$	Receive current listen (2.4 GHz)		60		mA	
$I_{RX,5GHz}$	Receive current listen (5 GHz)		56		mA	
$I_{2.4GHz,DTIM1}$	Average current consumption (2.4GHz,DTIM=1, beacon duration 3.8 ms)		3.47		mA	
$I_{2.4GHz,DTIM3}$	Average current consumption (2.4GHz,DTIM=3, beacon duration 3.8 ms)		1.12		mA	
$I_{2.4GHz,DTIM10}$	Average current consumption (2.4GHz,DTIM=10, beacon duration 3.8 ms)		0.34		mA	
$I_{5GHz,DTIM1}$	Average current consumption (5GHz,DTIM=1, beacon duration 0.7 ms)		1.70		mA	
$I_{5GHz,DTIM3}$	Average current consumption (5GHz,DTIM=3, beacon duration 0.7 ms)		0.56		mA	
$I_{5GHz,DTIM10}$	Average current consumption (5GHz,DTIM=10, beacon duration 0.7 ms)		0.19		mA	
$I_{2.4GHz,TWT,1\ min}$	Average current consumption (2.4GHz, TWT, target wake interval 1 min)[2]		29.5		uA	
$I_{2.4GHz,TWT,1\ hour}$	Average current consumption (2.4GHz, TWT, target wake interval 1 hour)[2]		18.4		uA	
$I_{2.4GHz,TWT,1\ day}$	Average current consumption (2.4GHz, TWT, target wake interval 1 day)[2]		18.2		uA	
$I_{5GHz,TWT,1\ min}$	Average current consumption (5GHz, TWT, target wake interval 1 min)[2]		28.9		uA	
$I_{5GHz,TWT,1\ hour}$	Average current consumption (5GHz, TWT, target wake interval 1 hour)[2]		18.2		uA	
$I_{5GHz,TWT,1\ day}$	Average current consumption (5GHz, TWT, target wake interval 1 day)[2]		18.0		uA	
I_{OFF}	Shutdown current		1.7		µA	
I_{SLEEP}	Sleep current (with RTC)		15		µA	
I_{SCAN}	Average current consumption during scan operation		60		mA	The exact current depends on the number of APs detected during scan. The value quoted aligns with ~100 APs.

4.3.3. Receiver characteristics

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$P_{SENS,2.4GHz,1DSSS}$	Sensitivity 2.4GHz (1 Mbps DSSS)		-98.6		dBm	
$P_{SENS,2.4GHz,11CCK}$	Sensitivity 2.4GHz (11 Mbps CCK)		-90.4		dBm	
$P_{SENS,2.4GHz,6MBPS}$	Sensitivity 2.4GHz (6 Mbps)		-91.6		dBm	
$P_{SENS,2.4GHz,54MBPS}$	Sensitivity 2.4GHz (54 Mbps)		-75.4		dBm	
$P_{SENS,2.4GHz,HT-MCS0}$	Sensitivity 2.4GHz (HT-MCS0)		-90.0		dBm	
$P_{SENS,2.4GHz,HT-MCS7}$	Sensitivity 2.4GHz (HT-MCS7)		-71.5		dBm	
$P_{SENS,5GHz,VHT-MCS0}$	Sensitivity 5.0GHz (VHT-MCS0)		-89.3		dBm	
$P_{SENS,5GHz,VHT-MCS7}$	Sensitivity 5.0GHz (VHT-MCS7)		-71.0		dBm	
$P_{SENS,5GHz,HE-MCS0}$	Sensitivity 5.0GHz (HE-MCS0)		-89.3		dBm	
$P_{SENS,5GHz,HE-MCS7}$	Sensitivity 5.0GHz (HE-MCS7)		-70.6		dBm	

4.3.4. Transmit current consumption

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$I_{TX,1DSSS,2.4GHz}$	Transmit current (2.4 GHz, 1DSSS, max output power)		252		mA	
$I_{TX,MSC0,2.4GHz}$	Transmit current (2.4 GHz, MSC0, max output power)		187		mA	
$I_{TX,MCS7,2.4GHz}$	Transmit current (2.4 GHz, MCS7, max output power)		191		mA	
$I_{TX,MSC0,5GHz}$	Transmit current (5 GHz, MSC0, max output power)		260		mA	
$I_{TX,MCS7,5GHz}$	Transmit current (5 GHz, MCS7, max output power)		260		mA	

4.3.5. Transmitter characteristics

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$P_{TXMAX,2.4GHz,DSSS/CCK}$	Maximum transmit power 2.4 GHz (DSSS/CCK)		20		dBm	
$P_{TXMAX,2.4GHz,MCS0}$	Maximum transmit power 2.4 GHz (6 Mbps/HT-MCS0/HE-MCS0)		15		dBm	
$P_{TXMAX,2.4GHz,MCS7}$	Maximum transmit power 2.4 GHz (54 Mbps/HT-MCS7/HE-MCS7)		15		dBm	
$P_{TXMAX,5GHz,MCS0}$	Maximum transmit power 5 GHz (6 Mbps/HT-MCS0/VHT-MCS0/HE-MCS0)		13		dBm	
$P_{TXMAX,5GHz,MCS7}$	Maximum transmit power 5 GHz (54 Mbps/HT-MCS7/VHT-MCS7/HE-MCS7)		13		dBm	

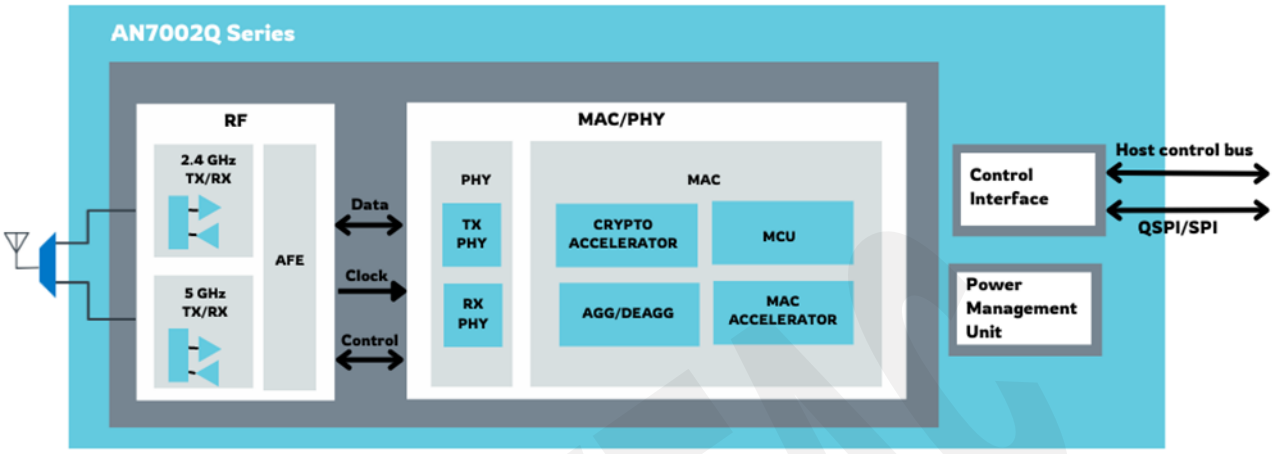
4.3.6. Transmitter power variation over temperature

Frequency band	-40C<TA<=-20C	-20C<TA<=0C	0C<TA<=60C	60C<TA<=85C
2.4GHz	0dB	0dB	0dB	-1dB
5GHz	-2dB	-1dB	0dB	-2dB

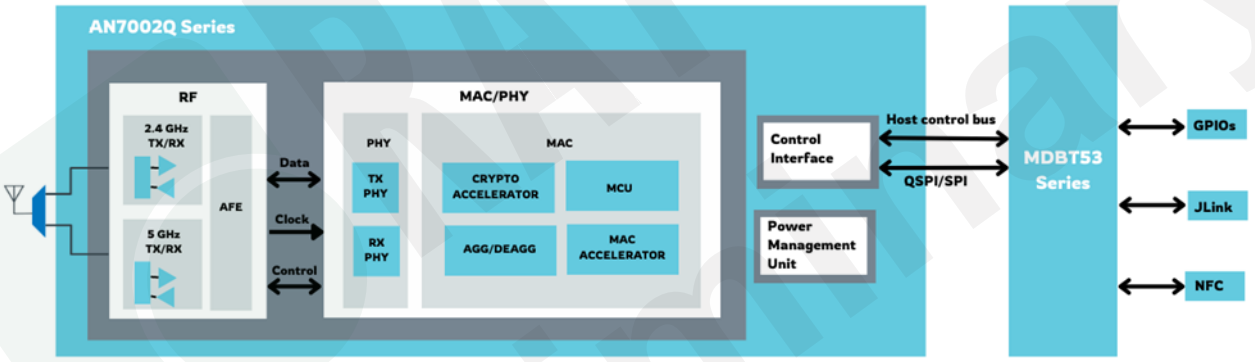
4.3.7. Transmitter power variation over supply voltage

Frequency band	2.9V<VBAT<=3.1V	3.1V<VBAT<=3.4V	3.4V<VBAT<=4.5V
2.4GHz	-1dB	0dB	0dB
5GHz	-2dB	-1dB	0dB

5. Block diagram



AN7002Q module

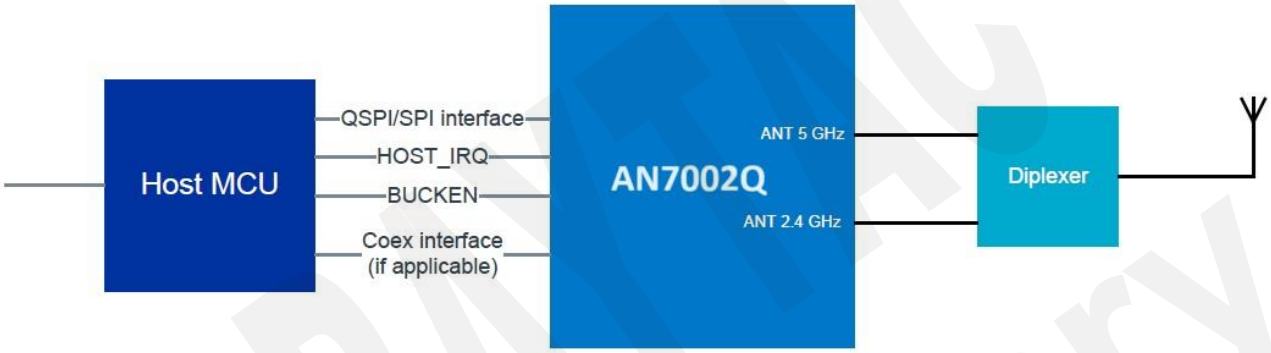


AN7002Q module is a companion alongside MDBT53 module

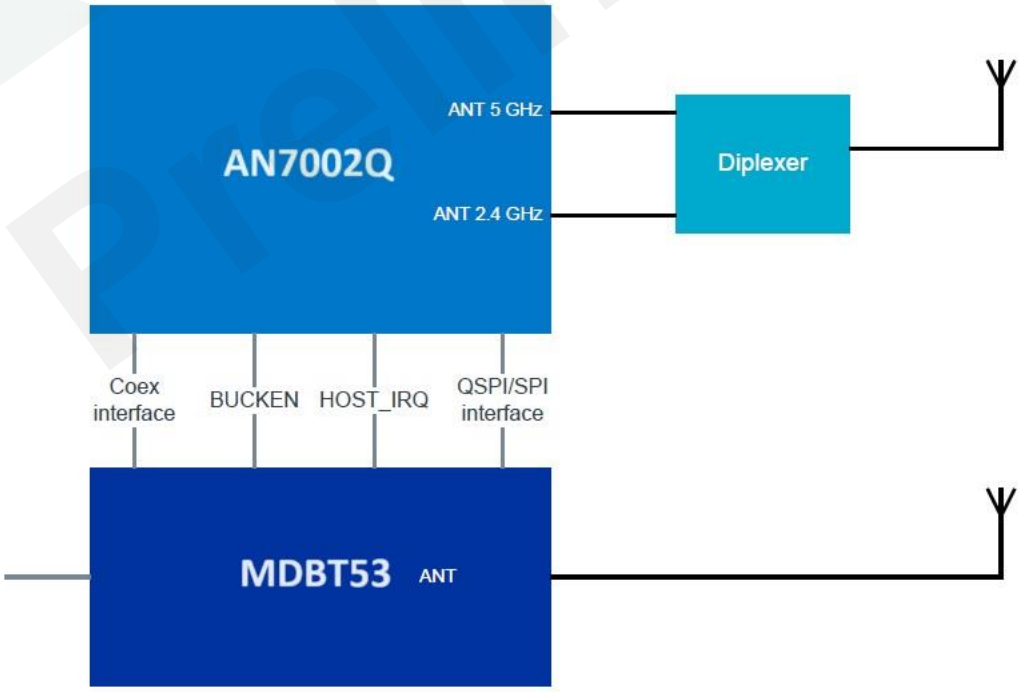
6. Host connection

AN7002Q is a wireless companion device that is connected to a host MCU or application processor. It is connected to the host through a QSPI (6-wire) or SPI (4-wire) for data and a 3-wire or 4-wire coexistence control interface for hosts that include a Bluetooth LE/IEEE 802.15.4 radio. In addition, two lines (HOST_IRQ and BUCKEN) are required. The user application executes on the host MCU.

The following figure shows a system with AN7002Q and a host MCU.



AN7002Q is designed to support radio coexistence and can be used together with another nRF Series device. The following figure shows AN7002Q together with Raytac MDBT53 series to achieve a combined Bluetooth LE and Wi-Fi solution. nRF5340 functions as a host and common interface to the wireless system.



7. Power and clock management

The power and clock management system in AN7002Q is optimized for ultra-low power applications to ensure maximum power efficiency.

7.1. Power states

AN7002Q has three power states: Shutdown, Sleep, and Active.

- **Shutdown**

A fully inactive state where no state information is retained except for the contents of the *One Time Programmable (OTP) memory*. AN7002Q will only respond to a BUCKEN assertion (input to *Power Management Unit (PMU)*).

The following conditions occur during Shutdown state:

- PMU: Off
- Analog circuits: All circuits off
- Baseband logic and scratch RAMs: Off
- Retention RAMs: Off
- *SPI/QSPI: Off*

- **Sleep**

A low-power state where state information is retained and transitioning to Active state can occur rapidly. The device may be in the Sleep state during both pre-association (device idle waiting for host command) and post-association period as part of the Wi-Fi Power Save mode (that is, maintain association with an Access Point but without data traffic). In this state, the device is clocked through the internal 32 kHz RC oscillator (Real-time Clock (RTC)), and can be awakened through the host interface or the internal sleep timer expiry.

The following conditions occur during Sleep state:

- PMU: Low-power mode (Pulse-Frequency Modulation (PFM))
- Analog circuits: RTC active, register state retained. All other circuits are powered down.
- Baseband logic and scratch RAMs: Off
- Retention RAMs: Off
- SPI/QSPI: On

- **Active**

In the Active state, the device will be in one of the Active sub-states: Transmit, Receive, or Idle. The high frequency crystal oscillator derived clocks are active and the appropriate RF section components are enabled as required. The Idle sub-state is a short term transitory state used when Receive is not required, but Sleep cannot be exploited (for example, upon early termination of an RX packet).

The following conditions occur during Active state:

- PMU: High-power mode *(Pulse-Width Modulation (PWM))*
- Analog circuits: All circuits powered (including crystal oscillator). The circuits are enabled according to Active sub-state (TX, RX, or IDLE)
- Baseband logic and scratch RAMs: On
- Retention RAMs: Active
- SPI/QSPI: On

7.2. Power state operation

Apart from transitions in or out of Shutdown state through the BUCKEN pin, all transitions between Sleep and Active states are automatic and do not rely on any control pin assertion or de-assertion.

Shutdown state is achieved by de-assertion on the BUCKEN pin. Asserting BUCKEN will result in the Active (IDLE sub-state) state being entered. The host will initiate the boot sequence through SPI/QSPI, culminating in the Sleep state being entered. This is the lowest power non-Shutdown state that can be achieved. Transitions from Active to Sleep are fully controlled by AN7002Q. Transitions from Sleep to Active are determined by both the host and AN7002Q. In a pre-association condition, Sleep is entered opportunistically whenever there is no activity initiated from the host (for example, a scan request). In a post-association condition, Sleep opportunities are determined by the negotiated Power Save mode of the Access Point. No host interactions are required to enter Sleep, while the host invokes a transition from Sleep to Active as part of any SPI/QSPI command transaction.

1. Switch the Power Management Unit (PMU) to high power mode (PWM).
2. Apply power to the digital logic, RAMs, and analog circuits.
3. Start the 40 MHz crystal oscillator and allow to settle.
4. Start the baseband PLL and allow to settle.

5. Boot all processor cores.
6. Execute baseband initializations.
7. Execute RF initializations and calibrations.

The initial steps consume equal duration whether originating in Shutdown or Sleep, while the baseband and RF initializations are dependent on the originating state. In particular:
Full baseband initializations are required from Shutdown (including transferring the Factory Information Configuration Registers (FICR) information from OTP memory into retention RAM), while in Sleep some of the state is retained in retention RAMs.

- Full baseband initializations are required from Shutdown (including transferring the Factory Information Configuration Registers (FICR) information from OTP memory into retention RAM), while in Sleep some of the state is retained in retention RAMs.
- Complete RF calibrations are required from Shutdown, including across channels to support scanning. From Sleep, only minimal initialization or calibration on the operating channel is required.

See Electrical specification on page 34 for timing information.

7.3. Clock accuracy considerations

The crystal oscillator is active during normal operation, and is the clock reference for the RF synthesizer, the Analog-to-Digital Converter (ADC)/Digital-to-Analog Converter (DAC) sample clocks, and the baseband logic. The RTC is active during sleep state, and is used to run the wakeup timer used as part of Wi-Fi Power Save. The crystal oscillator is inactive during sleep.
The IEEE 802.11 specification defines the accuracy of the Wi-Fi carrier frequency to be within ± 20 ppm (in 5 GHz), which in turn defines the required accuracy of the external crystal. There is provision to trim the crystal oscillator through a value programmed into the OTP memory on the AN7002Q device (or any other available non-volatile memory). This trimming will compensate for the combined frequency offset resulting from the crystal itself as well as any crystal oscillator variation at room temperature. The crystal and crystal oscillator will both exhibit frequency drift across temperature, and the crystal will also be subject to aging. The combination of these temperature and aging effects, along with the trimming accuracy, will consume the majority of the ± 20 ppm allowance, assuming a crystal with ± 10 ppm stability over temperature. The crystal tolerance (that is, accuracy at room temperature) is less important since this will be trimmed out by the crystal oscillator trim function (up to ± 20 ppm). The crystal oscillator/crystal is typically trimmed by transmitting

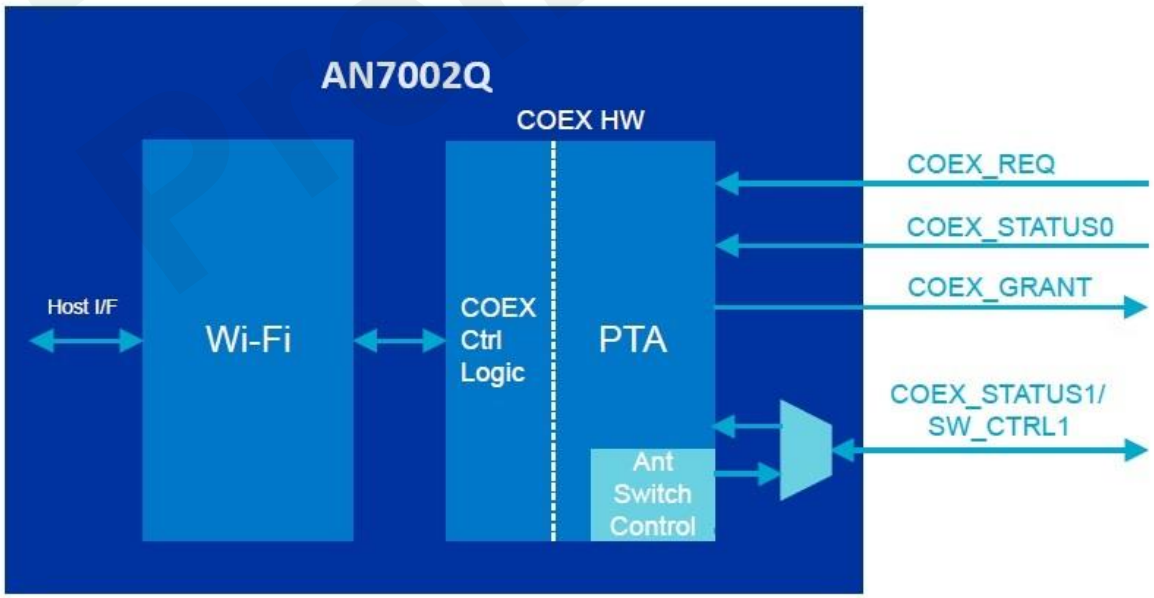
Wi-Fi packets through the antenna connector and using a Vector Signal Analyzer (VSA) to measure the frequency offset. Alternatively, a generic spectrum analyser can be used to measure the frequency offset on a transmitted Carrier Wave (CW).
The RTC is automatically calibrated against the trimmed 40 MHz crystal oscillator reference at runtime, and as such nothing needs to be done on the production line. During sleep, the RTC clocked wakeup timer is used to time wakeup intervals (since the last Delivery Traffic Indication Message (DTIM) beacon in regular Wi-Fi Power Save), and as such any residual inaccuracy is not accumulated.

8. Coexistence

AN7002Q Series devices have a highly configurable coexistence hardware to help mitigate interference between WLAN and Bluetooth LE/IEEE 802.15.4 devices (Thread, Zigbee).
A Packet Traffic Arbitration (PTA) module, connected to the CH logic function, facilitates the mitigation of various interference scenarios through a highly-programmable fabric. The coexistence hardware enables the output signal that support interface configurations 4-wire.
The primary schemes supported are:

- Separate Antenna mode – The PTA makes priority decisions, granting TX/RX requests from Bluetooth LE/IEEE 802.15.4. Each interface is permanently connected to its own antenna.

The following figure shows the architecture of the coexistence hardware with details about the PTA control lines.



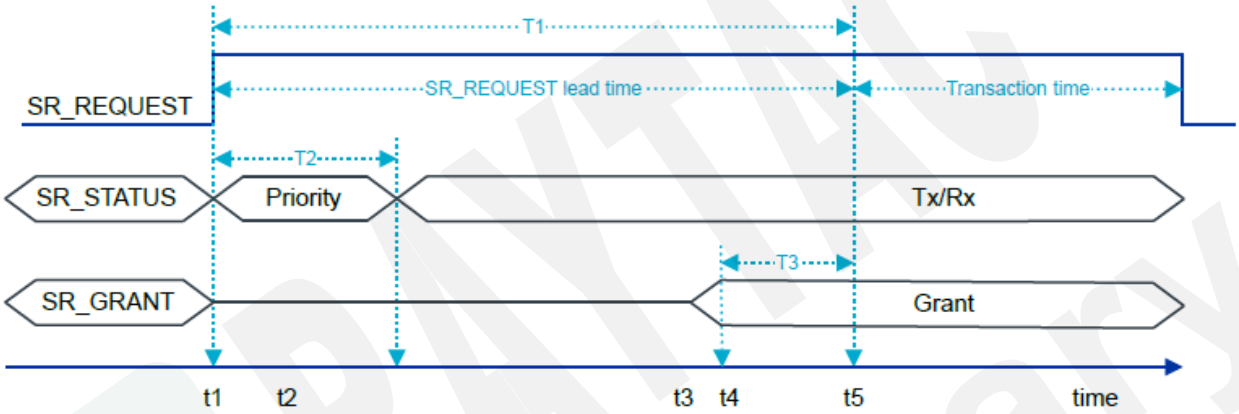
Signal name	I/O	Requirement	Bluetooth LE/ IEEE 802.15.4 signal (3-wire/4-wire)	Description
COEX_REQ	Input	Mandatory for 3-wire and 4-wire	SR_REQUEST	Bluetooth LE/IEEE 802.15.4 device requesting a TX/ RX transaction
COEX_STATUS0	Input	Mandatory for 3-wire and 4-wire	SR_STATUS	Indicates if the Bluetooth LE/ IEEE 802.15.4 transaction is TX or RX. If the device supports a Priority signal, Priority is muxed with TX/RX on this signal based on the timing diagrams.
COEX_GRANT	Output	Mandatory for 3-wire and 4-wire	SR_GRANT	Indicates that the Bluetooth LE/IEEE 802.15.4 device is granted access for this transaction.
COEX_STATUS1/ SW_CTRL1	Input/ Output	Optional for 3-wire	SR_PTI/ RF_SW_CTRL1	In 4-wire mode, this carries the Bluetooth LE/ IEEE 802.15.4 1 bit priority signal. In 3-wire Shared Antenna mode, this can be optionally used as a second antenna switch control signal.

8.1. Bluetooth LE/IEEE 802.15.4 timing

This section provides Bluetooth LE/IEEE 802.15.4 timing diagrams and parameters

3-wire with multiplexed priority

The following diagram shows external Bluetooth LE/IEEE 802.15.4 timing parameters when SR_STATUS
carries both priority and TX/RX information in a time multiplexed manner.



Parameter	Description
T1: SR_REQUEST lead time period	The time SR_REQUEST is asserted before actual transactions.
T2: SR_STATUS	The time when SR_STATUS is sampled to get SR_PTI information.
T3: SR_GRANT	The time before PTA should post SR_GRANT so that it is stable to be considered by the Bluetooth LE/IEEE 802.15.4 device.

The Bluetooth LE/IEEE 802.15.4 timing parameters are used to derive PTA timing parameters. The following table describes the relationship between PTA timing parameters and Bluetooth LE/IEEE 802.15.4 timing parameters.

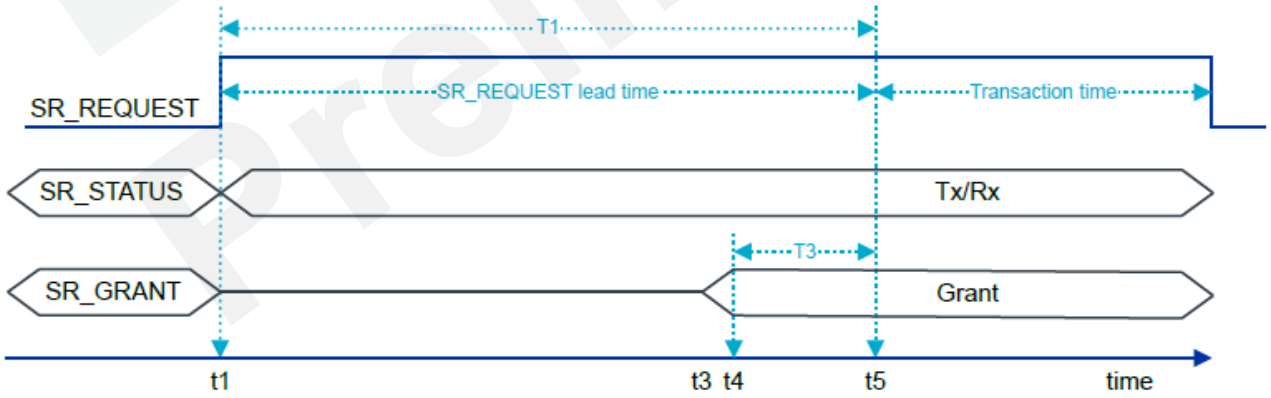
PTA timing parameter	Relation with Bluetooth LE/IEEE 802.15.4 timing parameter
Bluetooth LE/IEEE 802.15.4 device status priority sampling time (t2)	t1 < t2 < (t1+T2)
PTA arbitration decision time (t3)	(t1+T2) < t3 < (T1-T3)

Time instance	Description
t1	The time instance when SR_REQUEST is asserted.
t2	The time instance when SR_STATUS is sampled to get SR_PTI information. This can be any time during T2.
t3	The time instance when PTA takes an arbitration decision and posts SR_GRANT to the Bluetooth LE/IEEE 802.15.4 device. This is chosen a couple of microseconds before the start of the *SR grant lead time period*. This ensures that SR_GRANT is asserted as close to *SR grant lead time period* and is stable by the time the Bluetooth LE/IEEE 802.15.4 device uses this information to continue or abort the transaction.
t4	The time instance when the *SR grant lead time period* starts. This is the time when SR_GRANT must be stable to be considered by the Bluetooth LE/IEEE 802.15.4 device.
t5	The time instance when the actual transaction of the Bluetooth LE/IEEE 802.15.4 device starts. This is the time when the signaling period ends and the transaction period starts. Bluetooth LE/IEEE 802.15.4 Tx and Rx information is provided by changing the SR_STATUS signal level appropriately. PTA should track SR_STATUS if SR_REQUEST is high and update the information SR_TX_RX.

3-wire without multiplexed priority

If SR_STATUS carries only one parameter information (3-wire, no priority mode), then the default

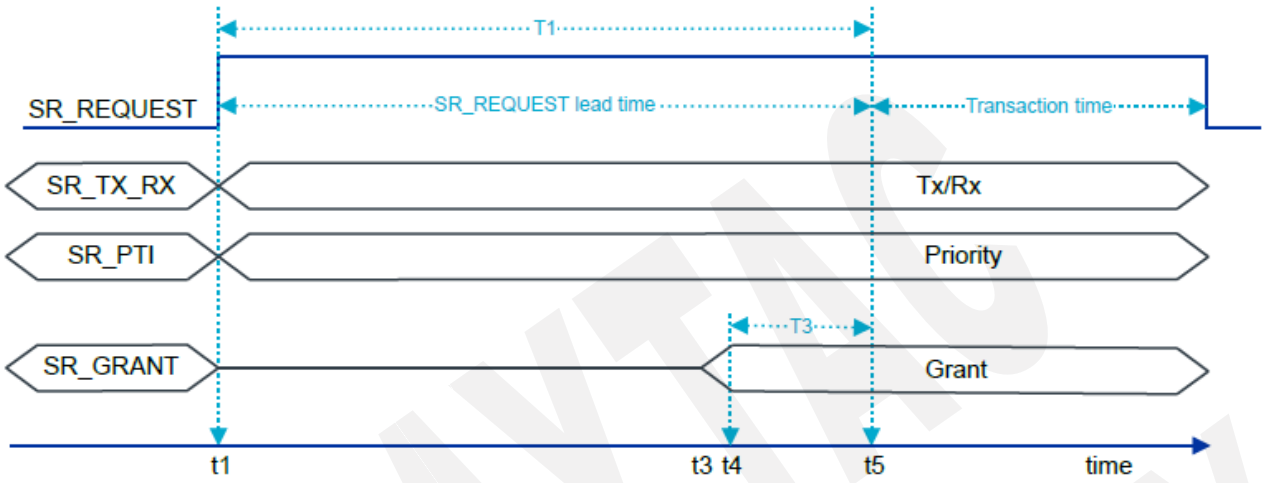
information that it carries is SR_TX_RX. In this case, SR_STATUS is set to TX or RX when SR_REQUEST is HIGH. The following diagram shows SR_STATUS only carrying TX/RX information. The signals are represented as a bus even though they are single bit ports to indicate transitions happening on the ports.



During the transaction, the Bluetooth LE/IEEE 802.15.4 device changes SR_STATUS appropriately to indicate TX and RX information. PTA continuously tracks SR_STATUS while SR_REQUEST is high and updates SR_TX_RX status internally for corresponding COEX behavior.

4-wire timing

In the following diagram, Bluetooth LE/IEEE 802.15.4 priority is explicitly signaled on the BT_COEX_STATUS1 pin.



9. OTP memory programming

AN7002Q includes a 128 x 32-bit OTP memory. This memory is partitioned into two regions, a factory
programmed region and a customer programmed region, each containing 64 x 32-bit locations.
The factory programmed region contains information related to production and trim values. The customer
programmed region contains:

- Encryption key used to protect the QSPI traffic (4 words)
- MAC addresses for VIF0 and VIF1 (4 words)
- Module level calibration coefficient (1 word)
- OTP memory protection control (4 words)
- Default register control (1 word)
- Reserved (24 words)
- User data region (26 words)

QSPI encryption is optional. This is enabled at runtime through a QSPI command. If this feature is not required, the OTP memory locations can remain unprogrammed. For security reasons, the encryption key cannot be read once programmed.

The MAC address fields in the OTP memory are accessed by firmware when powering up the device and presented to the host through an SPI/QSPI-based event as part of the boot phase. The host driver is responsible for configuring the MAC addresses as part of device configuration. As such, the MAC addresses stored in OTP memory can be overwritten by the host. Using this mechanism, the MAC addresses in the OTP memory can remain unprogrammed if an alternate host side storage is used.

The only module level calibration coefficient is the crystal oscillator trim. This is required to minimize the frequency offset resulting from the external 40 MHz crystal. See Device Commissioning and Characterization for information related to calibration.

Although the OTP memory is one time programmable, any bit still in a 1 state can be reprogrammed into a 0 state. To avoid deliberate or inadvertent modification of the OTP memory data, a protection mechanism is provided. The protection registers initially need to be programmed to 0x50FA50FA in order to activate programming of the remaining locations.

Once OTP memory programming is complete, the protection registers should be programmed to 0x00000000, at which point the OTP memory can never be modified.
In addition to the logical protection mechanism described above, a programming voltage needs to be applied to the OTPVDD pin in order to enable programming. The programming voltage is 2.5 V, while for reads it is 1.8 V. To coordinate the OTPVDD supply voltage with read and write operations, it is recommended to drive this supply from the POWERIOVDD output pin on AN7002Q. This also ensures there will be no leakage associated with the OTP memory across sleep cycles, where the digital supply rail is removed.

The OTP memory is indirectly mapped, and as such read and writes are achieved using address, data, and mode registers. The OTP memory programming utility implements this programming, along with appropriate control of the OTPVDD supply through the POWERIOVDD output.

10. FICR - factory information configuration registers

The Factory Information Configuration Registers (FICR) are stored in the OTP memory.
FICR has two regions:

• A factory-programmed region that contains device information and has the INFO group registers.

• A customer-programmable region that contains empty registers for the customer to write data to. It
has the QSPI, MAC, and CALIB group registers.

Access to the customer-programmable region is controlled using the PROTECTION register.
The PROTECTION scenarios are:

• When PROTECTION is unprogrammed, neither read not write is enabled.

• When PROTECTION is programmed to 0x50FA50FA, full read and write access is enabled.

• When PROTECTION is programmed to 0x00000000, access protection is applied and readout of
QSPI.KEY is prevented.

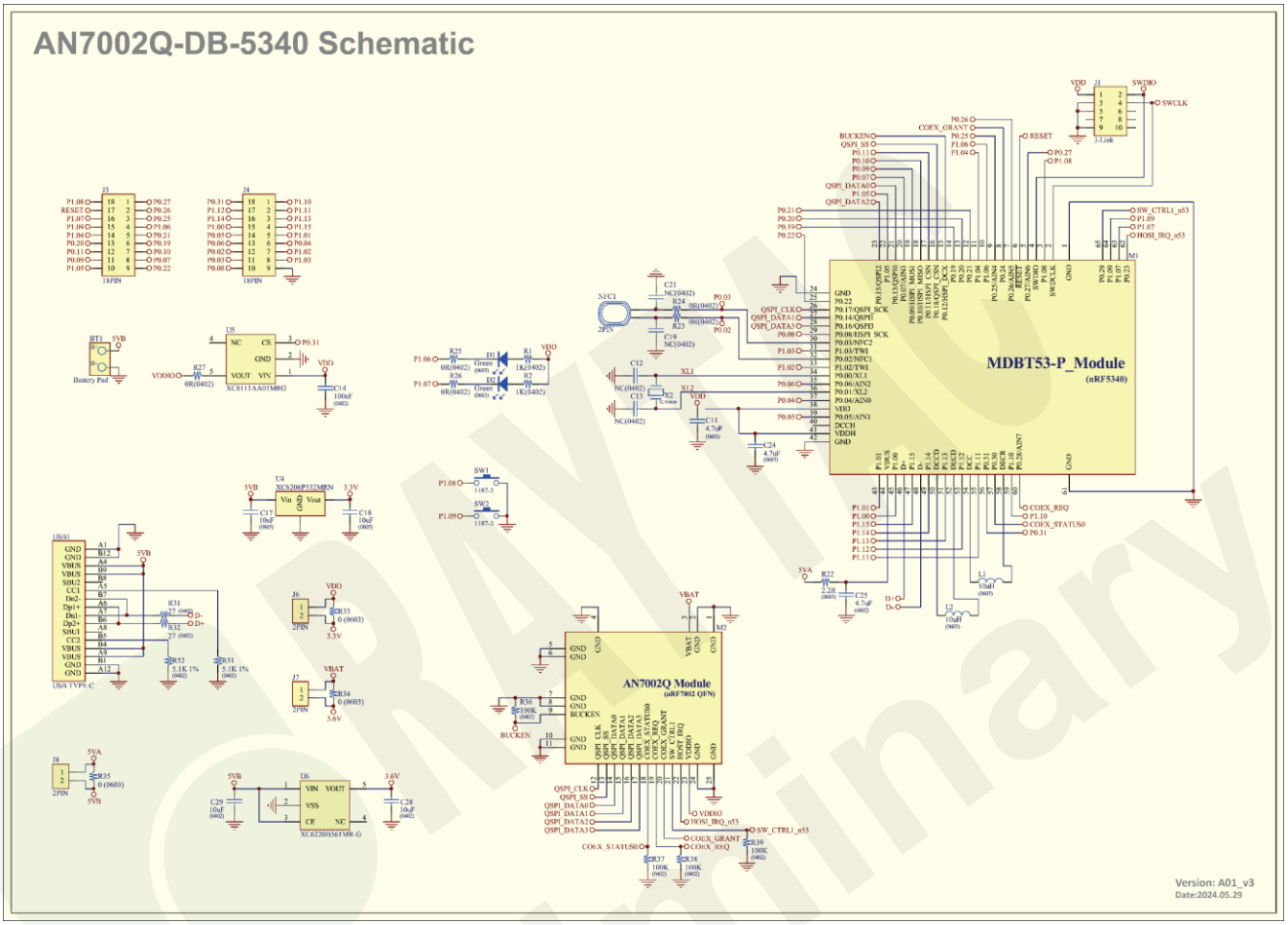
The following table shows the access protection for the different register groups.

Register group	0xFFFFFFFF	0x50FA50FA	0x00000000
QSPI.KEY	-	R/W	-
MAC.ADDRESS	-	R/W	R
CALIB	-	R/W	R

Please click to download full spec from "nRF7002 Product Specification v1.1".

11. Reference circuit

AN7002Q module compatible with MDBT5340 module



12. Notes and cautions

Module is not designed to last for a lifetime. Like general products, it is expected to be worn out after continuous usage through the years. To assure that product will perform better and last longer, please make sure you:

- Follow the guidelines of this document while designing circuit/end-product. Any discrepancy of core Bluetooth technology and technical specification of IC should refer to definition of Bluetooth Organization and Nordic Semiconductor as final reference.

- Do not supply voltage that is not within range of specification.

- Eliminate static electricity at any cost when working with the module as it may cause damage. It is highly recommended adding anti-ESD components to circuit design to prevent damage from real-life ESD events. Anti-ESD methods can be also applied in mechanical design.

- Do not expose modules under direct sunlight for long duration. Modules should be kept away from humid and salty air conditions, and any corrosive gasses or substances. Store it within -40℃ to +125℃ before and after installation.

- Avoid any physical shock, intense stress to the module or its surface.

- Do not wash the module. No-Clean Paste is used in production. Washing it will oxidize the metal shield and have chemistry reaction with No-Clean Paste. Functions of the module are not guaranteed if it has been washed.

The module is not suitable for life support device or system and not allowed to be used in destructive device or systems in any direct or indirect ways. The customer agrees to indemnify Raytac for any losses when applying modules in applications such as the ones described above.

13. Useful links

- Nordic Infocenter: https://infocenter.nordicsemi.com/index.jsp
  All the necessary technical files and software development kits of Nordic's chip are on this website.

- Nordic DevZone: https://devzone.nordicsemi.com/questions/
  A highly recommended website for firmware developer. Interact, discuss and consult with other fellow developers and Nordic's employees to get answers to your questions. The site also includes tutorials in detail to help you get started.

- Official Page of nRF7002 : https://www.nordicsemi.com/Products/nRF7002
  A brief introduction to nRF7002 and download links for Nordic's developing software and SoftDevices.

Full list of Raytac's WiFi modules

AN7002Q series (QFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna
AN7002Q	nRF7002	AN7002Q	1	Chip Antenna
		AN7002Q-P	1	PCB Antenna
		AN7002Q-U	1	u.FL Connector

Full list of Raytac's Bluetooth modules

- **AN54L15 series (QFN package IC) ~ coming soon**

- **AN54H20 series ~ coming soon**

- **AS1262 series (QFN package IC) ~ coming soon**

- **MDBT53 series (WLCSP package IC)**

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT53	nRF5340	MDBT53-1M	1	Chip Antenna	512 kb	1 MB
MDBT53-P	nRF5340	MDBT53-P1M	1	PCB Antenna	512 kb	1 MB
MDBT53-U	nRF5340	MDBT53-U1M	1	u.FL Connector	512 kb	1 MB

- **MDBT53V series (WLCSP package IC)**

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT53V	nRF5340	MDBT53V-1M	1	Chip Antenna	512 kb	1 MB
MDBT53V-P	nRF5340	MDBT53V-P1M	1	PCB Antenna	512 kb	1 MB

MDBT50 series (QFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT50	nRF52820	MDBT50-256R	1	Chip Antenna	32 kb	256 kb
	nRF52833	MDBT50-512K	1		128 kb	512 kb
MDBT50-P	nRF52820	MDBT50-P256R	1	PCB Antenna	32 kb	256 kb
	nRF52833	MDBT50-P512K	1		128 kb	512 kb

MDBT50Q series (aQFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT50Q	nRF52840	MDBT50Q-1MEN	3	Chip Antenna	256 kb	1 MB
	nRF52840	MDBT50Q-1MV2	2			
	nRF52833	MDBT50Q-512K	1		128 kb	512 kb
MDBT50Q-P	nRF52840	MDBT50Q-P1MEN	3	PCB Antenna	256 kb	1 MB
	nRF52840	MDBT50Q-P1MV2	2			
	nRF52833	MDBT50Q-P512K	1		128 kb	512 kb
MDBT50Q-U	nRF52840	MDBT50Q-U1MEN	3	u.FL Connector	256 kb	1 MB
	nRF52840	MDBT50Q-U1MV2	2			
	nRF52833	MDBT50Q-U512K	1		128 kb	512 kb
Dongle	nRF52840	MDBT50Q-RX	1, 2	PCB Antenna	256 kb	1 MB
		MDBT50Q-CX-40	1			
	nRF52833	MDBT50Q-CX-33	1		128 kb	512 kb

MDBT42T series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42T	nRF52805	MDBT42T-192K	1	Chip Antenna	24 kb	192 K
MDBT42T-P		MDBT42T-P192K		PCB Antenna		

MDBT42TV series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42TV	nRF52805	MDBT42TV-192K	1	Chip Antenna	24 kb	192 K
MDBT42TV-P		MDBT42TV-P192K		PCB Antenna		

MDBT42 series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42	nRF52832	MDBT42-512KV2	2	Chip Antenna	64 kb	512 K
MDBT42-P		MDBT42-P512KV2		PCB Antenna		

MDBT42V series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42V	nRF52832	MDBT42V-512KV2	2	Chip Antenna	64 kb	512 K
MDBT42V-P		MDBT42V-P512KV2		PCB Antenna		

MDBT42Q series (QFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42Q	nRF52832	MDBT42Q-512KEN	3	Chip Antenna	64 kb	512 K
	nRF52832	MDBT42Q-512KV2	2			
	nRF52810	MDBT42Q-192KV2	2		24 kb	192 K
	nRF52811	MDBT42Q-192KL	1			
MDBT42Q-P	nRF52832	MDBT42Q-P512KEN	3	PCB Antenna	64 kb	512 K
	nRF52832	MDBT42Q-P512KV2	2			
	nRF52810	MDBT42Q-P192KV2	2		24 kb	192 K
	nRF52811	MDBT42Q-P192KL	1			
MDBT42Q-U	nRF52832	MDBT42Q-U512KEN	3	u.FL Connector	64 kb	512 K
	nRF52832	MDBT42Q-U512KV2	2			

MDBT40 series

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT40	nRF51822	MDBT40-256V3	3	Chip Antenna	16 kb	256 K
		MDBT40-256RV3			32 kb	256 K
MDBT40-P	nRF51822	MDBT40-P256V3	3	PCB Antenna	16 kb	256 K
		MDBT40-P256RV3			32 kb	256 K

Release note

- 2024/07/29 Version 0.1: Preliminary.