ARM Cortex®-M0

32-BIT MICROCONTROLLER

NM18440 Series Product Brief

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1 GENERAL DESCRIPTION

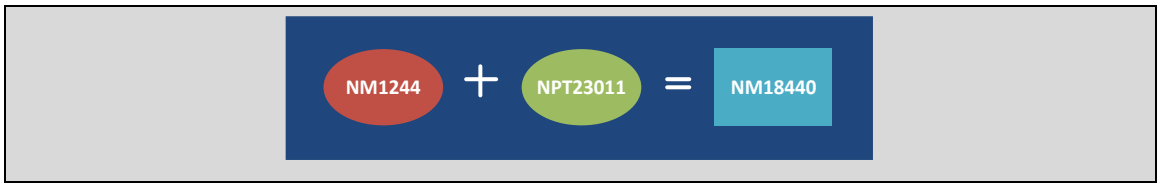
The NM18440 series 32-bit microcontroller(MCU) is embedded with ARM® Cortex™-M0 core and three phase half-bridge power MOSFET and IGBT drivers with independent high and low side referenced output channels for motor driver applications which require high performance, high integration, and low cost. The Cortex™-M0 is the ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NM1244 series can run up to 48(60) MHz and operate at 2.2V(3.3V) ~ 5.5V, -40℃ ~ 105℃, and thus can support a variety of industrial control applications which need high CPU performance. The NM1244 offers 64 Kbytes embedded program Flash, size configurable Data Flash (shared with program flash), 7.5 Kbytes Flash for the ISP, 1.5 Kbytes SPROM for security, and 8Kbytes SRAM. Plentiful system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, DAC, OP, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM18440 to reduce component count, board space and system cost.

The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 200 volts. It's also built-in the temperature sense output signal for MCU detection & one comparator for over current protection

Additionally, the NM18440 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

NM18440 is the combination of MCU NM1244 and Gate Driver NPT23011. User may refer to the TRM of NM1244 and the datasheet of NPT23011 for the detailed specification. The NM1244 BSP is also for NM18440 software developing.



2 FEATURES

- Recommended operation Supply Voltage VIN Range from 12 to 18V
- Gate Driver
  - Programmable enable/disable gate driver by MCU I/O of PA.6
  - Floating channel designed for bootstrap operation up to +200V
  - Gate driver supply range from 12 to 18V
  - Integrated one LDO
    - 5V, 35mA, LDO Output for MCU power supply(Note1)
  - VIN/VBS under-voltage lock-out
  - Cross conduction prevention
  - High side output in phase with HIN
- MCU Core
  - ARM® Cortex™-M0 core running up to 48/60 MHz by internal RC oscillator
  - One 24-bit system tick timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Memory
  - 64 Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 7.5 KB Flash memory for loader (LDROM)
  - Three 0.5 KB Flash memory for security protection (SPROM0, 1, 2)
  - 8 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - 48(60) MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 29 general-purpose I/O (GPIO) pins
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting

- Supports high driver and high sink I/O mode
- GPIO built-in Pull-up/Pull-low resistor for selection

- Timer
  - Provides four channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - Provides four operation modes: One-shot, Periodic, Toggle and Continuous
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Supports event counter function
  - Supports Toggle Output mode
  - Supports wake-up from Idle or Power-down mode
- Continuous Capture
  - Timer0, Timer1, Timer2 and Systick provided with continuous capture function to capture at most 4 edges continuously on one signal
- ECAP (Enhanced Input Capture)
  - One units of 24-bit input capture counter
  - Capture surce:
    - I/O inputs: ECAP ports(ECAP0, ECAP1 and ECAP2)
    - ACMP Trigger
- GDMA (General Direct Memory Access)
  - Two channels
  - Memory to/from memory or APB device
  - Memory to/from USCI TX/RX buffer which supports the hardware trigger
  - Supports “4-data burst” mode to boost performance
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM(Enhanced PWM Generator)
  - Support a built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot PWM function
  - Supports Edge-aligned and Center-aligned PWM type

- Support Asymmetric mode
- Programmable dead-zone insertion between complementary channels
- Each output has independent polarity setting control
- Hardware fault brake and software brake protections
- Supports rising, falling, central, period, and fault break interrupts
- Supports duty/period trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change
- Supports comparator event trigger PWM to force PWM output low for current period
- Provides interrupt accumulation function
- Gate driver PWM output by MCU PWM control

MCU PWM Control		Gate Driver PWM Output	
PWM0/2/4	**PWM1/3/5**	**UHO/VHO/WHO**	**ULO/VLO/WLO**
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
H	H	OFF	OFF

- BPWM (Basic PWM Generator)
  - One 16-bit PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter) and one dead-zone generator
  - Two independent outputs or one complementary paired outputs.
  - PWM Interrupt request synchronized with PWM period
  - Edge-aligned type or Center-aligned type option
  - Synchronous mode for BPWM and EPWM
- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - USCI1 Supports to be configured as UART, SPI or I²C individually
  - USCI2 Supports to be configured as UART and I²C individually
  - Supports programmable baud-rate generator
  - Supports GDMA trasfer
- 12-bit ADC (Analog-to-Digital Converter)
  - 12-bit ADC with 800ns conversion time
  - Supports 2 S/H (sample/hold)
  - Up to 17-ch single-end input from I/O and one internal input from band-gap.
  - Each input channel has own data register
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger

- Supports temperature sensor for measurement chip temperature
- Supports independent and simultaneous conversion modes

- OP Amplifier
  - Rail-to-rail OPA x 1
- DAC
  - Built-in two of 12-bit DAC,
  - Be the reference voltage for ACMP, ADC or output to pins.
- Analog Comparator
  - One analog comparators with 4 reference voltage source
    - Built-in 12-bit DAC0 and DAC1 for comparator reference voltage
    - Band-gap voltage
    - External voltage from port pin
  - Supports Hysteresis function 0/20/90/150mV at V_{DD} = 5V
  - Interrupt when compared result changed
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
  - Support 3 group of independent dividend, divisor, quotient and remainder registers for three times of calculation capacity
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: ESD HBM pass 2 kV; ESD 2 kV
- Packages:
  - 48-pin LQFP, 7mm x 7mm
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Note:

1. Higher LDO output current causes the higher IC temperature.

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Selection Guide

3.1.1 NM18440 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48/60 MHZ	BOD	PWM	Analog Comp.	OPA	DAC (12-Bit)	ADC (12-Bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI												
							UART*	I²C	SPI										
NM18440D	64	8	7.5	√	29	3	2	2	1	1	1	6	1	1	2	17x 12bit	1	√	LQFP 48 (7x7mm)

Table 3.1-1 NM18440 Base Series Selection Guide

3.2 Pin Configuration

3.2.1 NM18440D LQFP48(7mm x 7mm) Pin Diagram

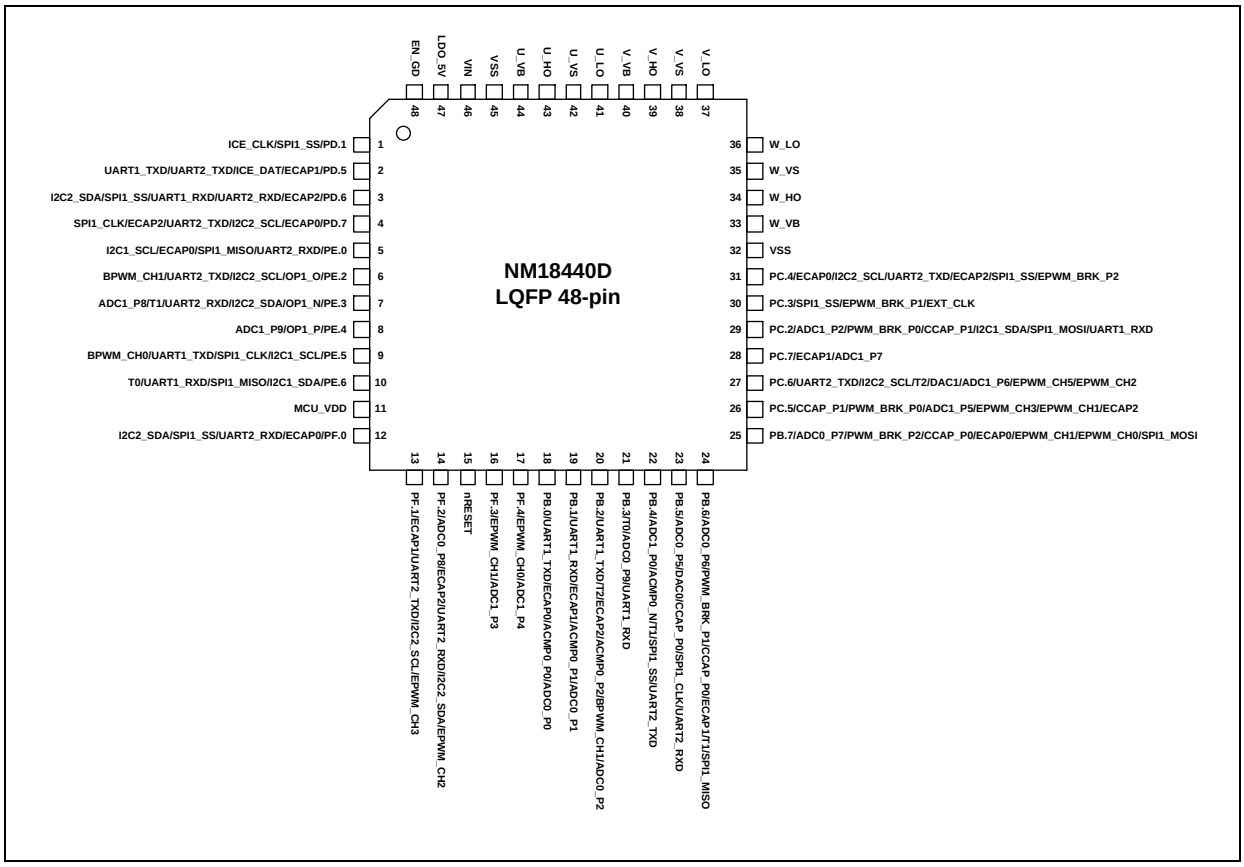


Figure 3.2-1 NM18440D LQFP48 pin Diagram

3.3 Pin Description

3.3.1 NM18440D Series LQFP48 Pin Description

NM1244Y48 QFN48 7x7	NPT23011 SOP 20	NM18440D LQFP48 7x7	Pin Name	Pin Type	Description
34	-	1	PD.1	I/O	General purpose digital I/O pin.
			ICE_CLK	I	Serial wired debugger clock pin.
			SPI1_SS	I/O	SPI1 slave select pin.
37	-	2	PD.5	I/O	General purpose digital I/O pin.
			ICE_DAT	I/O	Serial wired debugger data pin.
			ECAP1	I	Enhanced Input Capture input pin.
			UART1_TXD	O	Data transmitter output pin for UART.
			UART2_TXD	I/O	Data transmitter output pin for UART.
38	-	3	PD.6	I/O	General purpose digital I/O pin.
			I2C2_SDA	I/O	I2C2 data input/output pin.
			SPI1_SS	I/O	SPI1 slave select pin.
			ECAP2	I	Enhanced Input Capture input pin.
			UART1_RXD	I	Data receiver input pin for UART.
			UART2_RXD	I/O	Data receiver input pin for UART.
39	-	4	PD.7	I/O	General purpose digital I/O pin.
			ECAP0	I	Enhanced Input Capture input pin.
			I2C2_SCL	I/O	I2C2 clock pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.
40	-	5	PE.0	I/O	General purpose digital I/O pin.
			I2C1_SCL	I/O	I2C1 clock pin.
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
			ECAP0	I	Enhanced Input Capture input pin.
42		6	PE.2	I/O	General purpose digital I/O pin.
			BPWM_CH1	O	BPWM channel1 output/capture input.
			OP1_O	A	Operational Amplifier output pin.
			I2C2_SCL	I/O	I2C2 clock pin.
			UART2_TXD	O	Data transmitter output pin for UART.
43		7	PE.3	I/O	General purpose digital I/O pin.
			ADC1_P8	A	ADC1 channel analog input.
			OP1_N	A	Operational Amplifier Negitive input pin.
			T1	I/O	Timer1 event counter input / toggle output.
			I2C2_SDA	I/O	I2C2 data input/output pin.
			UART2_RXD	I	Data receiver input pin for UART.
44		8	PE.4	I/O	General purpose digital I/O pin.
			ADC1_P9	A	ADC1 channel analog input.
			OP1_P	A	Operational Amplifier Positive input pin.
45		9	PE.5	I/O	General purpose digital I/O pin.
			BPWM_CH0	O	BPWM channel0 output/capture input.
			I2C1_SCL	I/O	I2C1 clock pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
			UART1_TXD	O	Data transmitter output pin for UART.
46		10	PE.6	I/O	General purpose digital I/O pin.
			T0	I/O	Timer0 event counter input / toggle output.
			I2C1_SDA	I/O	I2C1 data input/output pin.
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
			UART1_RXD	I	Data receiver input pin for UART.
48		11	MCU_VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital function.
			PF.0	I/O	General purpose digital I/O pin.

NM1244Y48 QFN48 7x7	NPT23011 SOP 20	NM18440D LQFP48 7x7	Pin Name	Pin Type	Description
4		12	I2C2_SDA	I/O	I2C2 data input/output pin.
			SPI1_SS	I/O	SPI1 slave select pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
			ECAP0	I	Enhanced Input Capture input pin.
5		13	PF.1	I/O	General purpose digital I/O pin.
			EPWM_CH3	O	EPWM channel3 output/capture input.
			I2C2_SCL	I/O	I2C2 clock pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			ECAP1	I	Enhanced Input Capture input pin.
6		14	PF.2	I/O	General purpose digital I/O pin.
			ADC0_P8	A	ADC0 channel analog input.
			EPWM_CH2	O	EPWM channel2 output/capture input.
			I2C2_SDA	I/O	I2C2 data input/output pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.
7		15	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
8		16	PF.3	I/O	General purpose digital I/O pin.
			ADC1_P3	A	ADC1 channel analog input.
			EPWM_CH1	O	EPWM channel1 output/capture input.
9		17	PF.4	I/O	General purpose digital I/O pin.
			ADC1_P4	A	ADC1 channel analog input.
			EPWM_CH0	O	EPWM channel0 output/capture input.
10		18	PB.0	I/O	General purpose digital I/O pin.
			ADC0_P0	A	ADC0 channel analog input.
			ACMP0_P0	A	Analog comparator0 positive input pin.
			ECAP0	I	Enhanced Input Capture input pin.
			UART1_TXD	O	Data transmitter output pin for UART.
			ECAP0	I	Enhanced Input Capture input pin.
11		19	PB.1	I/O	General purpose digital I/O pin.
			ADC0_P1	A	ADC0 channel analog input.
			ACMP0_P1	A	Analog comparator0 positive input pin.
			ECAP1	I	Enhanced Input Capture input pin.
			UART1_RXD	I	Data receiver input pin for UART.
			ECAP1	I	Enhanced Input Capture input pin.
12		20	PB.2	I/O	General purpose digital I/O pin.
			ADC0_P2	A	ADC0 channel analog input.
			BPWM_CH1	O	BPWM channel1 output/capture input.
			ACMP0_P2	A	Analog comparator0 positive input pin.
			ECAP2	I	Enhanced Input Capture input pin.
			UART1_TXD	O	Data transmitter output pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.
			T2	I/O	Timer2 event counter input / toggle output.
13		21	PB.3	I/O	General purpose digital I/O pin.
			ADC0_P9	A	ADC0 channel analog input.
			T0	I/O	Timer0 event counter input / toggle output.
			UART1_RXD	I	Data receiver input pin for UART.
14		22	PB.4	I/O	General purpose digital I/O pin.
			ADC1_P0	A	ADC1 channel analog input.
			ACMP0_N	A	Analog comparator0 negative input pin.
			T1	I/O	Timer1 event counter input / toggle output.
			SPI1_SS	I/O	SPI1 slave select pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
15		23	PB.5	I/O	General purpose digital I/O pin.
			ADC0_P5	A	ADC0 channel analog input.

NM1244Y48 QFN48 7x7	NPT23011 SOP 20	NM18440D LQFP48 7x7	Pin Name	Pin Type	Description
			DAC0	A	DAC0 analog output.
			CCAP_P0	I	Timer Continuous Capture input pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
16		24	PB.6	I/O	General purpose digital I/O pin.
			ADC0_P6	A	ADC0 channel analog input.
			PWM_BRK_P1	I	Brake input pin of EPWM.
			CCAP_P0	I	Timer Continuous Capture input pin.
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
			ECAP1	I	Enhanced Input Capture input pin.
			T1	I/O	Timer1 event counter input / toggle output.
17		25	PB.7	I/O	General purpose digital I/O pin.
			ADC0_P7	A	ADC0 channel analog input.
			PWM_BRK_P2	I	Brake input pin of EPWM.
			CCAP_P0	I	Timer Continuous Capture input pin.
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
			ECAP0	I	Enhanced Input Capture input pin.
			EPWM_CH0	O	EPWM channel0 output/capture input.
			EPWM_CH1	O	EPWM channel1 output/capture input.
18		26	PC.5	I/O	General purpose digital I/O pin.
			ADC1_P5	A	ADC1 channel analog input.
			PWM_BRK_P0	I	Brake input pin of EPWM.
			CCAP_P1	I	Timer Continuous Capture input pin.
			ECAP2	I	Enhanced Input Capture input pin.
			EPWM_CH1	O	EPWM channel1 output/capture input.
			EPWM_CH3	O	EPWM channel3 output/capture input.
19		27	PC.6	I/O	General purpose digital I/O pin.
			ADC1_P6	A	ADC1 channel analog input.
			EPWM_CH2	O	EPWM channel2 output/capture input.
			DAC1	O	DAC1 analog output.
			T2	I/O	Timer2 event counter input / toggle output.
			I2C2_SCL	I/O	I2C2 clock pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			EPWM_CH5	O	EPWM channel5 output/capture input.
20		28	PC.7	I/O	General purpose digital I/O pin.
			ADC1_P7	A	ADC1 channel analog input.
			ECAP1	I	Enhanced Input Capture input pin.
23		29	PC.2	I/O	General purpose digital I/O pin.
			ADC1_P2	A	ADC1 channel analog input.
			PWM_BRK_P0	I	Brake input pin of EPWM.
			CCAP_P1	I	Timer Continuous Capture input pin.
			I2C1_SDA	I/O	I2C1 data input/output pin.
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
			UART1_RXD	I	Data receiver input pin for UART.
24		30	PC.3	I/O	General purpose digital I/O pin.
			EXT_CLK	I	External oscillator input pin.
			PWM_BRK_P1	I	Brake input pin of EPWM.
			SPI1_SS	I/O	SPI1 slave select pin.
25		31	PC.4	I/O	General purpose digital I/O pin.
			PWM_BRK_P2	I	Brake input pin of EPWM.
			ECAP0	I	Enhanced Input Capture input pin.
			I2C2_SCL	I/O	I2C2 clock pin.
			SPI1_SS	I/O	SPI1 slave select pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.

NM1244Y48 QFN48 7x7	NPT23011 SOP 20	NM18440D LQFP48 7x7	Pin Name	Pin Type	Description
47	11	32	VSS	P	Ground.
	10	33	W_VB	HP	High side floating supply
	9	34	W_HO	HO	High side gate driver output
	8	35	W_VS	HP	High side floating supply return
	7	36	W_LO	HO	Low side gate driver output
	13	37	V_LO	HO	Low side gate driver output
	14	38	V_VS	HP	High side floating supply return
	15	39	V_HO	HO	High side gate driver output
	16	40	V_VB	HP	High side floating supply
	17	41	U_LO	HO	Low side gate driver output
	18	42	U_VS	HP	High side floating supply return
	19	43	U_HO	HO	High side gate driver output
	20	44	U_VB	HP	High side floating supply
47	11	45	VSS	P	Ground.
	12	46	VIN	HP	The pin VCC in NPT23011. Power supply for the gate driver. Recommend connect a capacitor to VSS to stabilize the input power.
48		47	LDO_5V	P	Internal 5V LDO output for the power supply for digital circuit
32		48	EN_GD	I	Gate driver enable pin. The pin is also internally connected to PA.6 of NM1244
31[3]	1	-	-		PA.5 (PWM0) connect to HIN_U
30[3]	2	-	-		PA.4 (PWM1) connect to LIN_U
29[3]	3	-	-		PA.3 (PWM2) connect to HIN_V
28[3]	4	-	-		PA.2 (PWM3) connect to LIN_V
27[3]	5	-	-		PA.1 (PWM4) connect to HIN_W
26[3]	6	-	-		PA.0 (PWM5) connect to LIN_W

Table 3.3-1 NM18440D LQFP48 Pin Description

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

[3] GPA0 ~ GPA5 are set as EPWM5 ~ EPWM0 respectively in NM18440D

4 BLOCK DIAGRAM

4.1 NM18440 Block Diagram

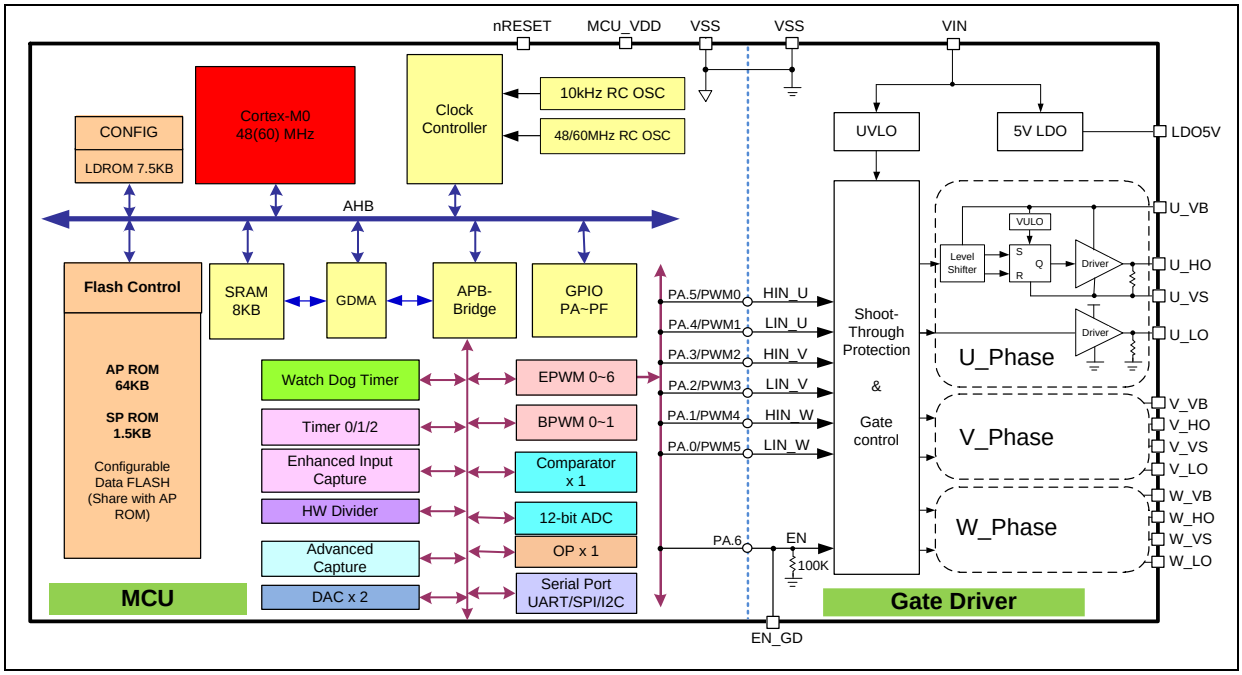
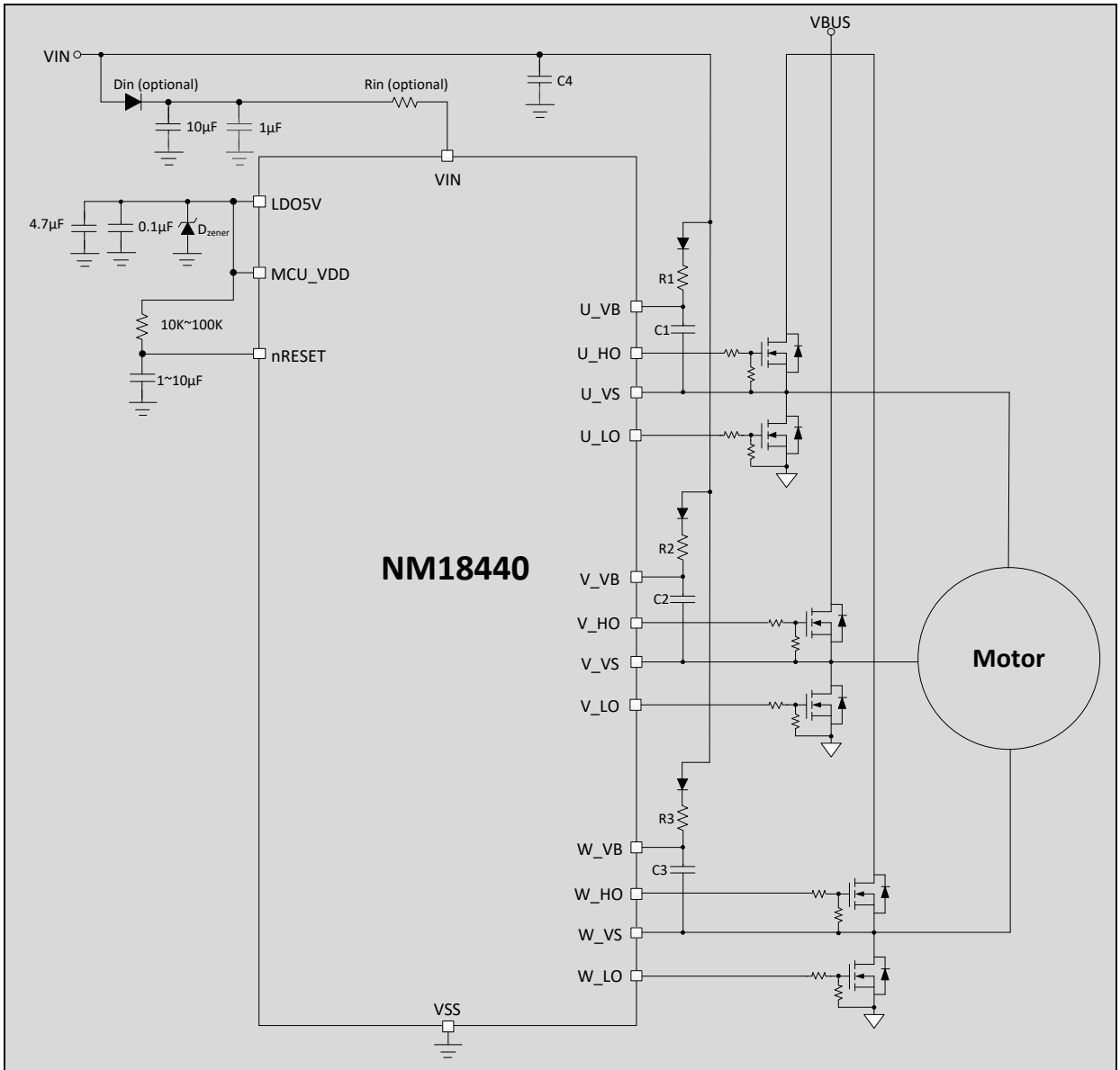


Figure 4.1-1 NM18440 Series Block Diagram

4.2 NM18440 Application Circuit



Note:

1. R1, R2 and R3 are suggest and typically (R1=R2=R3) ≥ 10ohm.
2. Rin is optional only for VIN>20V.
3. It suggests that C4 ≥ 10xC1 , C1=C2=C3.
4. The capacitance and resistance above are for reference only and are only tested under the conditions defined by Nuvoton. Due to the design and layout of the EVB, the capacitance and resistance may vary depending on the situation. Therefore, users should check both of them to suit their product function.

Figure 4.2-1 NM18440 Application Circuit

5 NM18440 ELECTRICAL CHARACTERISTICS

The data is for reference only. Please refer to the TRM of NM1244 and the datasheet of NPT23011 for the detailed electrical characteristics.

5.1 NM1244 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

5.2 NM1244 DC Electrical Characteristics

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
V_{DD}	Operation voltage	2.2	-	5.5	V	V_{DD} = 2.2V ~ 5.5V up to 48 MHz V_{DD} = 3.0V ~ 5.5V up to 60 MHz			
V_{SS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage[3]	1.21	1.23	1.25	V	V_{DD} = 2.2V ~ 5.5V, T_A = -40°C~105°C			
I_{DD}	Operating Current Normal Run Mode HCLK = 60 MHz while(1){} Executed from Flash	-	14.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	60 MHz	V
I_{DD}		-	10.3	-	mA	5.5V	X	60 MHz	X
I_{DD}		-	14.9	-	mA	3V	X	60 MHz	V
I_{DD}		-	10.3	-	mA	3V	X	60 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 48 MHz while(1){} Executed from Flash	-	10.4	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	5.5V	X	48 MHz	X
I_{DD}		-	10.4	-	mA	3V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	3V	X	48 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	5.5V	24 MHz	X	X
I_{DD}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	3V	24 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 16 MHz while(1){} Executed from Flash	-	3.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD}		-	3.0	-	mA	5.5V	16 MHz	X	X

I_{DD}		-	3.9	-	mA	3V	16 MHz	X	V
I_{DD}		-	3.0	-	mA	3V	16 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	3.1	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
I_{DD}		-	2.5	-	mA	5.5V	12 MHz	X	X
I_{DD}		-	3.1	-	mA	3V	12 MHz	X	V
I_{DD}		-	2.4	-	mA	3V	12 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	1.5	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD}		-	1.3	-	mA	5.5V	4 MHz	X	X
I_{DD}		-	1.4	-	mA	3V	4 MHz	X	V
I_{DD}		-	1.2	-	mA	3V	4 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 32 kHz while(1){} Executed from Flash	-	184	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	32 KHz	V	V[1]
I_{DD}		-	182	-	µA	5.5V	32 KHz	V	X
I_{DD}		-	164	-	µA	3V	32 KHz	V	V[1]
I_{DD}		-	162	-	µA	3V	32 KHz	V	X
I_{DD}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	178	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	X	10 KHz	V[2]
I_{DD}		-	178	-	µA	5.5V	X	10 KHz	X
I_{DD}		-	158	-	µA	3V	X	10 KHz	V[2]
I_{DD}		-	158	-	µA	3V	X	10 KHz	X
I_{IDLE}	Operating Current Idle Mode HCLK= 60 MHz	-	8.3	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	3.6	-	mA	5.5V	X	V	X

I_{IDLE}		-	8.3	-	mA	3V	X	V	V
I_{IDLE}		-	3.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK= 48 MHz	-	5.7	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE}		-	5.7	-	mA	3V	X	V	V
I_{IDLE}		-	2.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK = 24 MHz	-	2.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	5.5V	24 MHz	X	X
I_{IDLE}		-	2.9	-	mA	3V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	3V	24 MHz	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 16 MHz	-	2.2	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE}		-	2.1	-	mA	3V	V	X	V
I_{IDLE}		-	1.3	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 12 MHz	-	1.8	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.1	-	mA	5.5V	V	X	X
I_{IDLE}		-	1.7	-	mA	3V	V	X	V
I_{IDLE}		-	1.1	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 4 MHz	-	1.0	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	0.8	-	mA	5.5V	V	X	X

I_{IDLE}		-	1.0	-	mA	3V	V	X	V
I_{IDLE}		-	0.7	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 10 kHz	-	147	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	X	V	V[2]
I_{IDLE}		-	147	-	µA	5.5V	X	V	X
I_{IDLE}		-	127	-	µA	3V	X	V	V[2]
I_{IDLE}		-	126	-	µA	3V	X	V	X
I_{PWD}	Standby Current Power-down Mode (Deep Sleep Mode)	-	1	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.			
I_{PWD}		-	0.8	-	µA	V_{DD} = 3 V, All oscillators and analog blocks turned off.			
I_{LK}	Input Leakage Current	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode			
V_{IL1}	Input Low Voltage (TTL Input)	0.8	1.42		V	V_{DD} = 5.5 V			
		0.8	1.08			V_{DD} = 3.3 V			
V_{IH1}	Input High Voltage (TTL Input)		1.42	2.0	V	V_{DD} = 5.5 V			
			1.08	2.0		V_{DD} = 3.3 V			
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	$0.7V_{DD}$	-	-	V	-			
R_{UP}[3]	Internal Pull-up Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{LOW}[3]	Internal Pull-low Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{RST}	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.2 V ~ 5.5V			
V_{ILS}	Negative-going Threshold (Schmitt input)	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt input)	$0.7V_{DD}$	-	-	V	-			
I_{IL}	Logic 0 Input Current (Quasi-bidirectional Mode)	-	-63.65		µA	V_{DD} = 5.5 V, V_{IN} = 0V			
I_{TL}	Logic 1 to 0 Transition Current	-	-566.7	-	µA	V_{DD} = 5.5 V			
I_{SR}	Source Current (Quasi-	-	-372	-	µA	V_{DD} = 4.5 V, V_{IN} = 2.4 V			

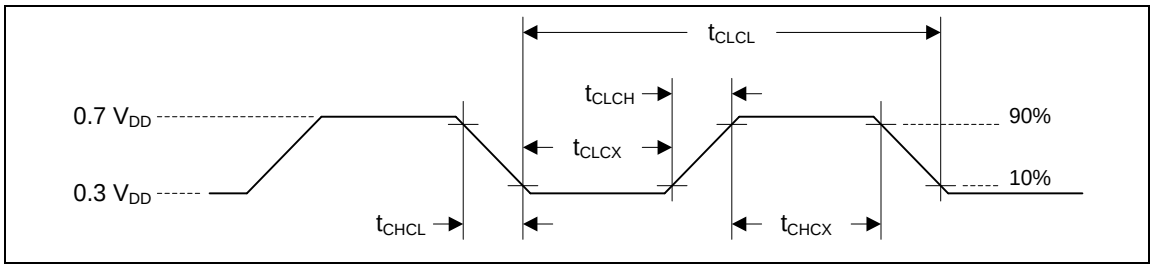
I_{SR}	bidirectional Mode)	-	-76.8	-	µA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR}		-	-37.3	-	µA	V_{DD} = 2.2 V, V_{IN} = 1.8 V
I_{SR}	Source Current (Push-pull Mode)	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR}		-	-2	-	mA	V_{DD} = 2.2 V, V_{IN} = 1.8 V
I_{SK}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain and Push-pull Mode)	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V
I_{SK}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V
I_{SK13}		-	6	-	mA	V_{DD} = 2.2 V, V_{IN} = 0.4 V

Notes:

1. Only enable modules, which support 32 kHz EXT_CLK source
2. Only enable modules, which support 10 kHz LIRC clock source.
3. Guaranteed by design, not test in production.

5.3 NM1244 AC Electrical Characteristics

5.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

5.3.2 External Clock Input (EXT_CLK) (up to 24MHz)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{EXT_CLK}	Operation Voltage	2.2	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
F_{EXT_CLK}	Clock Frequency	-	-	24	MHz	-

5.3.3 48/60 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC60}	Center Frequency	-	60	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1.0	-	+1.0	%	T_A = 25 ℃ V_{DD}=4.5 V~ 5.5 V
		-2.5	-	2.5	%	T_A = -40℃~105℃ V_{DD}=3.0 V~ 5.5 V
f_{HRC48}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1.0	-	+1.0	%	T_A = 25 ℃ V_{DD} = 5.5 V
		-2.5	-	2.5	%	T_A = -40℃~105℃ V_{DD}=2.2 V~ 5.5 V

5.3.4 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-5[1]	-	+5[1]	%	V_{DD} = 2.2 V ~ 5.5 V T_A = -40℃ ~ +105℃

Note1: These parameters are characterized but not tested.

5.4 NM1244 Analog Characteristics

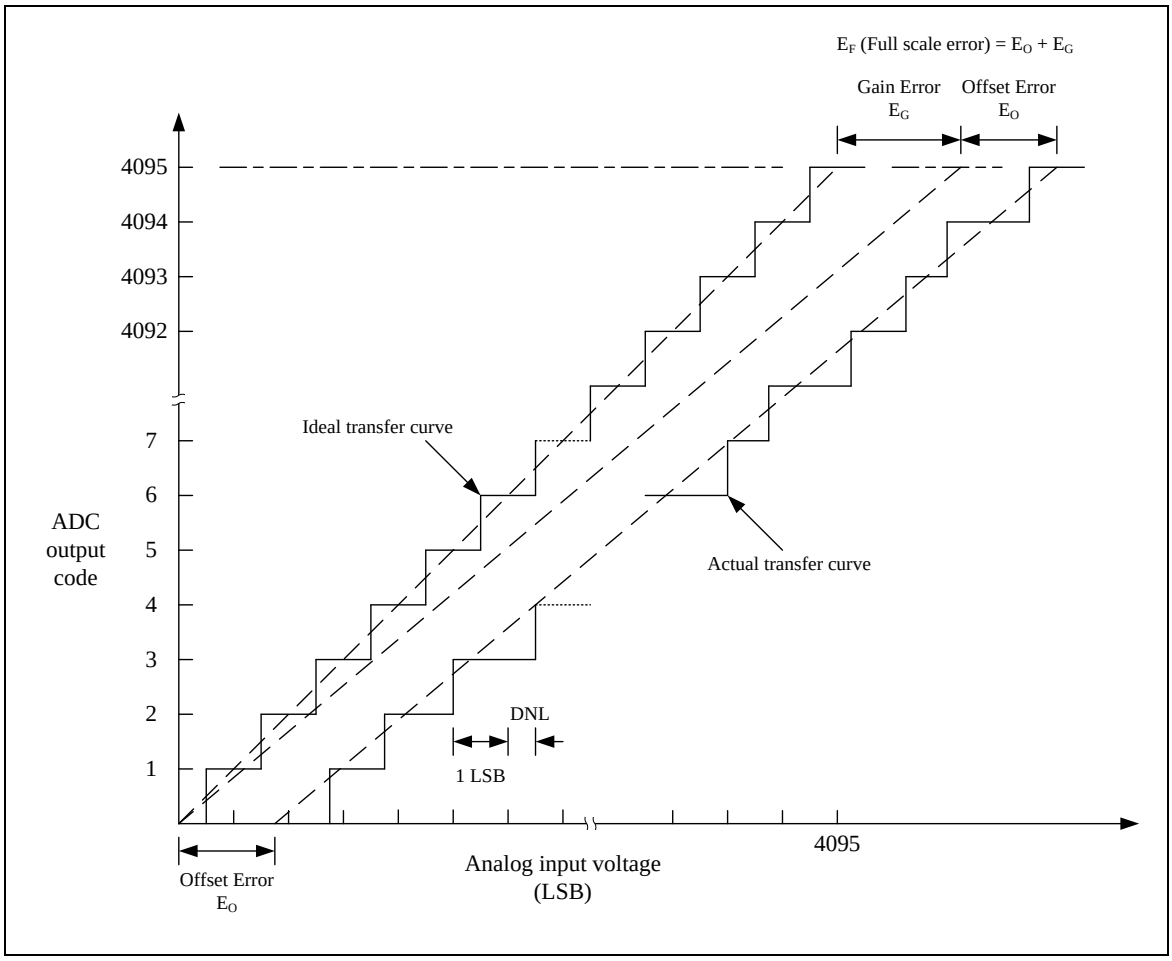
5.4.1 12-bit SAR ADC

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	2	-	LSB	V_{DD} = 3.0 ~5.5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	V_{DD} = 3.0 ~5.5 V
E_O	Offset Error	-	±1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_G	Gain Error (Transfer Gain)	-	-1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_A	Absolute Error	-	±3	-	LSB	V_{DD} = 3.0 ~5.5 V
-	Monotonic	Guaranteed			-	-
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		300			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time[3]		800	1000	ns	V_{DD} = 3.0~5.5 V
I_{DDA}	Operation Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	V_{DD}	V	-
C_{IN}	Input Capacitance[2]	-	1.6	-	pF	-

Note:

1. ADC voltage reference is same with V_{DD} .
2. It's for sample and hold. The maximum value depends on process variation. Basically, the variation of C_{IN} is less than about 10% of typical value.
3. Guaranteed by design, not test in production. The conversion time is upto auto-completion of analog comparison in ADC IP and the typical value is about 800ns at V_{DD} = 5V.


E_F (Full scale error) = E_O + E_G
Gain Error E_G
Offset Error E_O
4095
4094
4093
4092
7
6
5
4
3
2
1
ADC output code
Ideal transfer curve
Actual transfer curve
DNL
1 LSB
4095
Offset Error E_O
Analog input voltage (LSB)

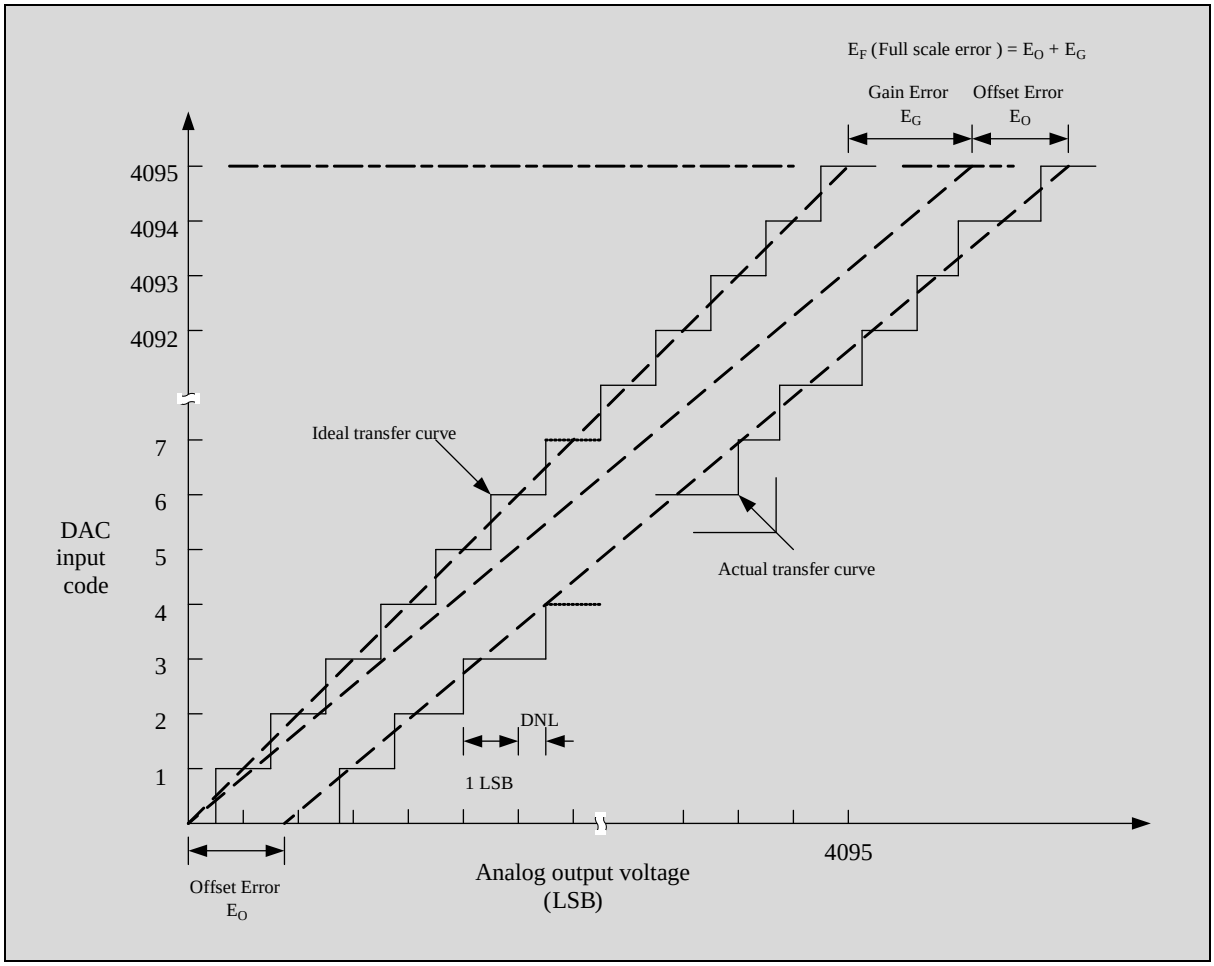
5.4.2 12-bit SAR DAC

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±4	-	LSB	V_{DD} = 5V
INL	Integral Nonlinearity Error	-	±3	-	LSB	V_{DD} = 5V
E_O	Offset Error	-	3	-	LSB	V_{DD} = 5V
E_G	Gain Error (Transfer Gain)	-	3	-	LSB	V_{DD} = 5V
I_{DDA}	Operation Current (Avg.)	-	100	-	uA	V_{DD} = 5V
V_{out}	Analog output Voltage	0	-	V_{DD}	V	-

Note:

1. DAC voltage reference is the same with V_{DD}.



5.4.3 DAC Output buffer

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Input offset voltage	-	2	5	mV	
Output swing	0.1	-	VDD-0.1	V	
Input common mode range	0.1	-	VDD-0.1	V	
DC gain	-	80	-	dB	
Slew rate	3.0	-	-	V/us	V_{DD} = 5V, RLOAD = 33K, CLOAD = 50p
Output Current		3		mA	V_{DD} – 0.3 ~ V_{SS} + 0.3, V_{DD} = 3~5V
Power consumption		200		uA	V_{DD} = 5V

5.4.4 LDO & Power Management

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LDO}	Output Voltage	1.35	1.5	1.65	V	-

Notes:

It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

5.4.5 Brown-out Detector

(V_{DD} – V_{SS} = 0 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{BOD}	Brown-out Hysteresis	30	100	150	mV	
V_{BOD}	Brown-out Detector	4.15	4.3	4.45	V	BOV_VL [2:0] = 7
		3.85	4.0	4.15	V	BOV_VL [2:0] = 6
		3.55	3.7	3.85	V	BOV_VL [2:0] = 5
		2.85	3.0	3.15	V	BOV_VL [2:0] = 4
		2.55	2.7	2.85	V	BOV_VL [2:0] = 3
		2.3	2.4	2.5	V	BOV_VL [2:0] = 2
		2.1	2.2	2.3	V	BOV_VL [2:0] = 1
		1.9	2.0	2.1	V	BOV_VL [2:0] = 0

5.4.6 Power-on Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{POR}	Threshold Voltage	1.60	1.75	1.90	V	-
V_{LVRLPM}	Threshold Voltage(Low Power)	1.3	1.6	2.1	V	-

5.4.7 LVR Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LVR}	Threshold Voltage(high→low)	1.7	1.9	2.1	V	-
V_{LVRHYS}	Hysteresis Voltage	-	-	100	mV	

5.4.8 Comparator

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	V_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	
V_{HYS}	Hysteresis	10	20	30	mV	ACMPHYSEN = 01
V_{HYS}	Hysteresis	60	90	120	mV	ACMPHYSEN = 10
V_{HYS}	Hysteresis	95	150	200	mV	ACMPHYSEN = 11
T_{STB}	Stable time	-	1.06	-	μs	

Notes:

Guaranteed by design, not test in production.

5.4.9 OP Amplifier

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Input offset voltage	-	2	5	mV	
Output swing	0.1	-	VDD-0.1	V	
Input common mode range	0.1	-	VDD-0.1	V	
DC gain	-	80	-	dB	
PSRR+	-	90	-	dB	VDD=5V
CMRR	-	90	-	dB	VDD=5V
Slew rate	6.0	-	-	V/us	VDD=5V, RLOAD=33K, CLOAD=50p
Wake up time	-	-	1	us	
Maximum output voltage swing from rail		20		mV	V_{DD} =5.5, RL=10K
		100		mV	V_{DD} =5.5, RL=2K
Open-loop output implement		200		ohm	V_{DD} =5, f=10MHz
Close-loop output implement		95		ohm	V_{DD} =5, f=10MHz

5.4.10 Temperature Sensor

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	-	105	℃	
-	Gain [1],	-	-1.81	-	mV/℃	
-	Offset [1,2]	-	715	-	mV	TA = 0 ℃

Note:

1. The temperature sensor formula for the output voltage (Vtemp) is list as below equation.
   Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)
2. The Gain and Offset may have some drift for different chips. Register SYS_TSOFFSET is a reference data measured by ADC in factory test.

5.4.11 ESD Characteristics

Symbol	Ratings	Condition	Package	Maximum Value	Unit
V_{ESD}	Electrostatic discharge (Human body mode)	TA = + 25 ℃	LQFP 48	8000	V
	Electrostatic discharge (Charged Device mode)			500	V

5.4.12 EFT Characteristics

Symbol	Condition	Package	Pass Level	Unit
	Fsys			
	HIRC	LQFP 48	+/- 4000	V

5.5 NM1244 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.35	1.5	1.65	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Sector Erase Time	-		5	ms	
T_{PROG}	Program Time	-	5	6.5	us	Per Byte
I_{DD1}	Read Current	-	4	5.5	mA	@50MHz
I_{DD2}	Program Current	-	-	3.5	mA	
I_{DD3}	Erase Current	-	-	2	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
   Guaranteed by design, not test in production.

5.6 NPT23011 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	- 0.3	200	V
V_S	High side floating supply offset voltage	V_B – 20	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S – 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	- 0.3	25	
V_{LO}	Low side output voltage	- 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage	- 0.3	V_{CC} + 0.3	
dV_S / dt	Allowable offset supply voltage transient	—	50	V / ns
P_D	Package power dissipation @ TA ≤ + 25 ℃ (20 lead SOIC)	—	1.5	W
R_{thJA}	Thermal resistance, junction to ambient (20 lead SOIC)	—	60	℃ / W
T_J	Junction temperature	—	150	℃
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

5.7 NPT23011 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply absolute voltage	V_S + 12	V_S + 18	V
V_S	High side floating supply offset voltage	- 6	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	12	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
tdead	HIN & LIN dead time (depends on MCU control)	1	-	us
T_A	Ambient temperature	- 40	125	℃

5.8 NPT23011 Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, T_A = 25 ºC, unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
**V_{IH}	Logic " 1 " input voltage	V_{CC} = 10V to 15V	2.4	-	-	V
**V_{IL}	Logic " 0 " input voltage	V_{CC} = 10V to 15V	-	-	0.8	
I_{LK}	Offset supply leakage current (one phase)	V_B = V_S = 200 V	-	-	60	uA
I_{QBS}	Quiescent VBS supply current (one phase)	V_{IN} = 0 V or 5 V	-	-	250	
I_{QCC}	Quiescent VCC supply current	V_{IN} = 0 V or 5 V	-	-	1000	
I_{IN+}	Logic " 1 " input bias current	V_{IN} = 5 V	-	50	100	
I_{IN-}	Logic " 0 " input bias current	V_{IN} = 0 V	-	0	1	
V_{CCUV+}	VCC supply under voltage positive going threshold		8	9	10	V
V_{BSUV+}	VBS supply under voltage positive going threshold		7.7	8.7	9.7	
V_{CCUV-}	VCC supply under voltage negative going threshold		7	8	9	
V_{BSUV-}	VBS supply under voltage negative going threshold		6.8	7.8	8.8	
I_{O+}	Souring peak current	C_L=0.22uF, 20KHz	-	300	-	mA
I_{O-}	Sink peak current	C_L=0.22uF, 20KHz	-	600	-	mA
**R_{IN}	HIN, LIN pin pull low resistor		-	100	-	KΩ
R_{OUT}	HO, LO pin pull low resistor(Applied between LO – COM, HO – VS)		-	100	-	KΩ
R_{EN}	EN pin pull low resistor		-	100	-	KΩ

Note:
1. Different versions decided by metal layers change.
2. ESD device; MM>200V; HBM>2KV; HV pin(VB/HO/VS)>1KV; power bus holding voltage should be > 20V
3. Device are ESD sensitive. Handling precautions are recommended.

** : EPWMx of NM1240 and HINx/LINx of NPT23011 are bonded inside NM18440, so specification are characterized but not tested. The item is only for reference.

5.9 NPT23011 Dynamic Electrical Characteristics

VBIAS (VCC, VBS) = 15 V, VSS = COM, CL = 1nF, TA = 25 ºC, unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
**ton	Turn-on propagation delay	-	330	-	ns	VS = 0V
**toff	Turn-off propagation delay	-	250	-	ns	VS = 0V
tr	Turn on rise time	-	50	-	ns	
tf	Turn off fall time	-	30	-	ns	
DT	Dead Time	-	500	-	ns	

Note： 1. Input PWM pulse width must be ≧ 1 μs for HO & LO normally output.

** : EPWMx of NM1240 and HINx/LINx of NPT23011 are bonded inside NM18440, so specification are characterized but not tested. The item is only for reference.

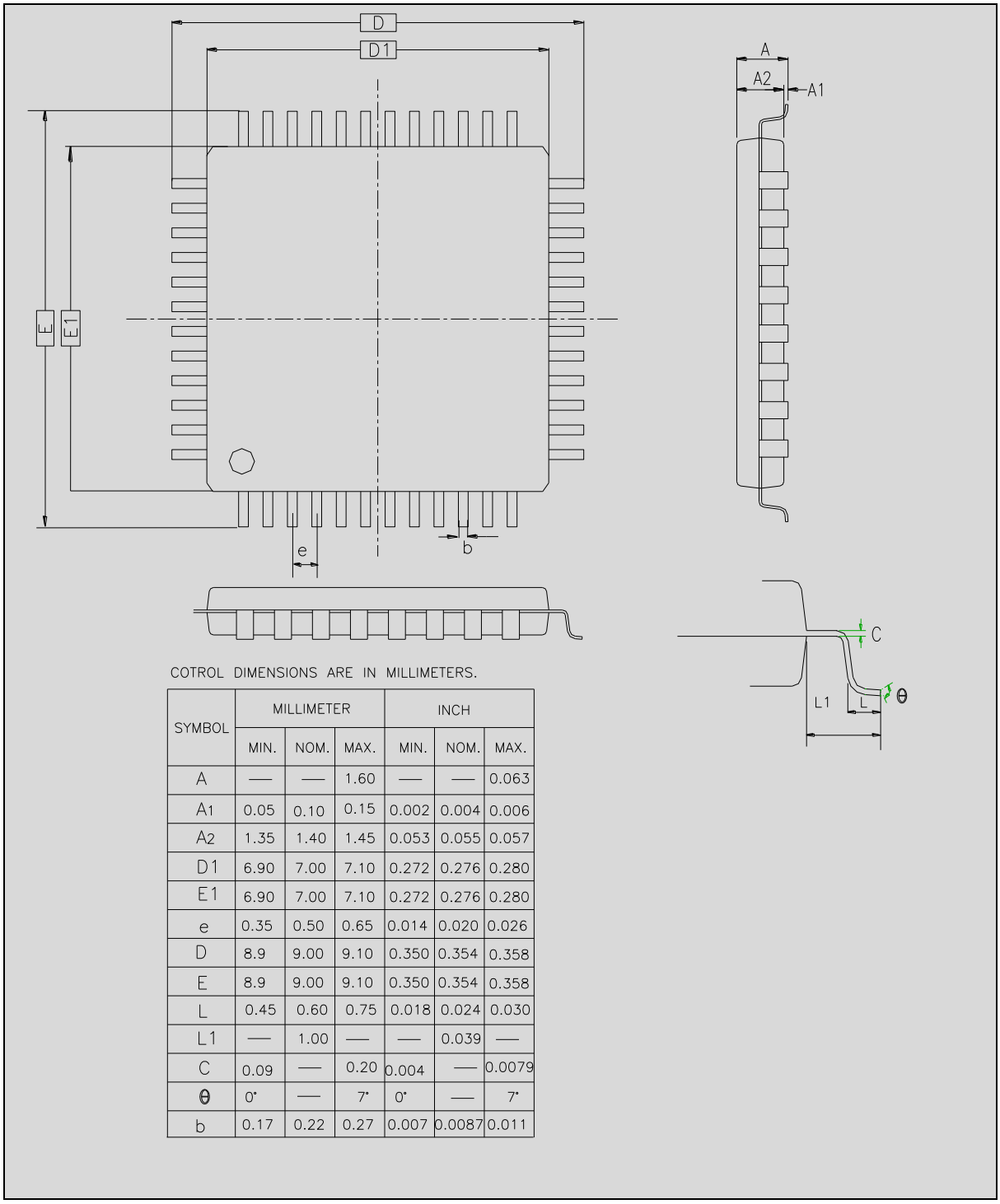
5.10 DC Electrical Characteristic for LDO_5V_OUT

VBIAS(VCC, VBS) = 15 V, TA= 25ºC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{5V}	5V Output Voltage		4.75	5	5.25	V
I_{5V}	5V Output Current		-	30	-	mA

6 PACKAGE DIMENSIONS

6.1 48-pin LQFP (7mm x 7mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

7 ORDERING INFORMATION

Part Number	Supplied As	Package Type	Operating Temperature
NM18440D	2000 units/ T&R	LQFP48, 7mm x 7mm, Green Package	Commercial, -40℃~105℃

8 REVISION HISTORY

Revision	Date	Description
0.01	February 07, 2022	1. Preliminary version 0.01
0.02	May 07, 2022	2. Modify typo: “VCC Range” to “VIN Range” in section 2 FEATURES
0.02	August 24, 2022	3. Modify the note of section 5.8 NPT23011 Static Electrical Characteristics
0.02	November 08, 2022	1. Add compliance statement of International Environmental Regulations.