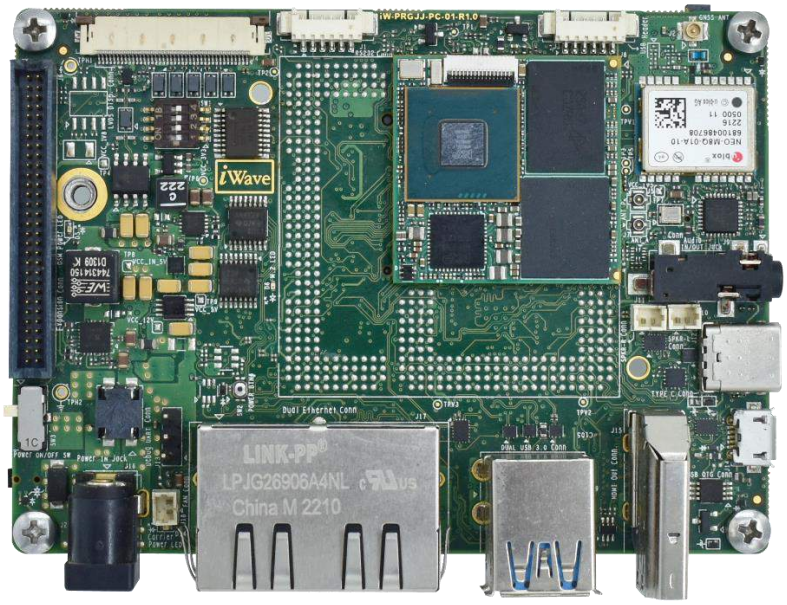
iW-RainboW-G46S

i.MX 8XLite

Pico ITX Single Board Computer

Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Pico ITX Single Board Computer based on the NXP's i.MX 8XLite Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8XLite Pico ITX SBC from a Hardware Systems perspective.

1.2 Pico ITX SBC Overview

The Pico ITX is a versatile small form factor SBC (Single Board Computer) definition targeting application that require low power, low costs, and high performance. The SBCs are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies and GBE are concentrated on the SBC.

NXP's i.MX 8XLite SoC based Pico ITX Single Board computer is rich with i.MX 8XLite features along with eMMC, Dual Ethernet PHY, RS232 and comes in compact 100mm x 72mm form factor.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
OTG	On-The-Go
PCB	Printed Circuit Sheet

Acronyms	Abbreviations
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SBC	Single Board Computer
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on SBC.

1.5 References

- IMX8DXLA1AEC_Revx.pdf
- iMX8DXL_RM_Rev_x.pdf

1.6 Important Note

In this document, wherever i.MX 8XLite SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_9)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO1_9*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8XLite Pico ITX SBC features and Hardware architecture with high level block diagram.

2.1 i.MX 8XLite Pico ITX SBC Block Diagram

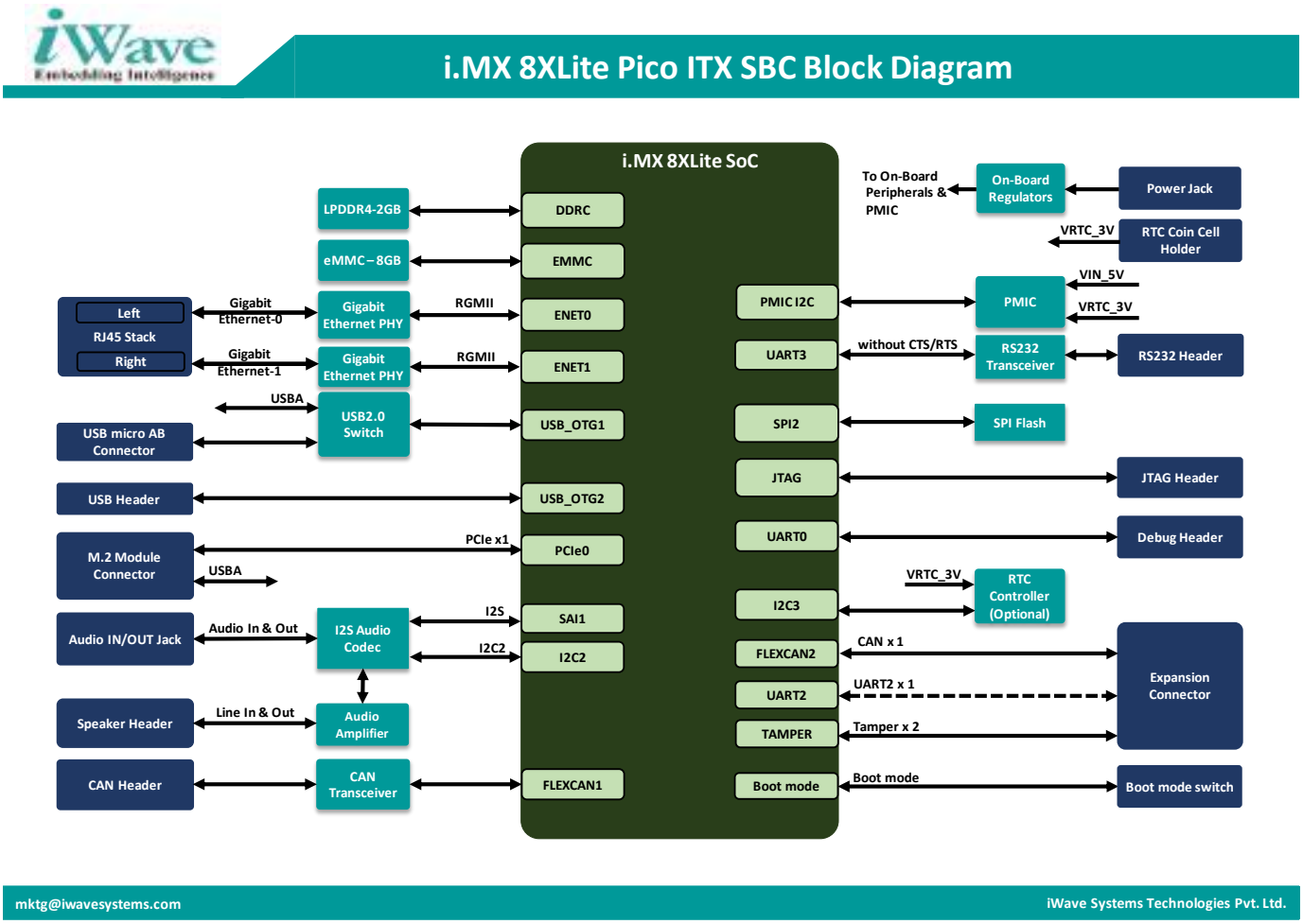

Figure 1: i.MX 8XLite Pico ITX SBC Block Diagram

2.2 i.MX 8XLite Pico ITX SBC Features

i.MX 8XLite Pico ITX SBC supports the following features.

CPU

- i.MX 8XLite Applications Processor
  - i.MX 8XLite Dual : 2 x Cortex-A35, 1 x Cortex-M4F
  - i.MX 8XLite Solo : 1 x Cortex-A35, 1 x Cortex-M4F

Power

- PF7100 PMIC

Memory

- LPDDR4 - 2GB
- eMMC Flash - 8GB (Expandable)[1]
- 16Mb SPI Flash

Network & Communication

- Gigabit Ethernet PHY Transceiver with RJ45 Magjack Connector x 2
- USB 2.0 OTG port through –microAB Receptacle Connector
- USB2.0 Header x 1
- RS232 x 1 (without CTS/RTS)
- CAN x 1

Audio/Video Features

- I2S Audio Codec
- 3.5mm Audio IN/OUT
- Speaker out header

Expansion Connector Interfaces

- CAN x 1 Port
- Tamper x 2 Ports
- UART x 1 Port (Optional)

Miscellaneous Interfaces

- Debug UART Connector
- JTAG Header
- RTC Battery Connector

- M.2 Connector Key B
  - PCIe × 1
  - USB 2.0 x 1
  - I2C x 1
  - Nano SIM Connector

General Specification

- Power Supply : 12V,2 A[2]
- Form Factor : 100mm X 72mm

1. *Memory Size will differ based on iWave's SBC Product Part Number.*
2. *The i.MX 8XLite SBC can support wide range input power from 7V to 24V. By default, it is designed to support 12V.*

2.3 CPU

iW-RainboW-G46S-i.MX 8XLite Pico ITX SBC can support different i.MX 8XLite SoCs from NXP.

2.4 i.MX 8XLite SoC

iW-RainboW-G46S Pico ITX SBC can support i.MX 8XLite SoCs from NXP. The i.MX 8XLite Family consists of two processors: i.MX 8XLite Dual & i.MX 8XLite Solo. The Major Difference between i.MX 8XLite SoCs are:

- i.MX 8XLite Dual : 2 x Cortex-A35, 1 x Cortex-M4F
- i.MX 8XLite Solo : 1 x Cortex-A35, 1 x Cortex-M4F

The i.MX 8XLite processors have advanced multicore processing with V2X acceleration supported by Arm cores. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, SD 3.0 and a wide range of peripheral I/Os such as PCIe 3.0 provide wide flexibility.

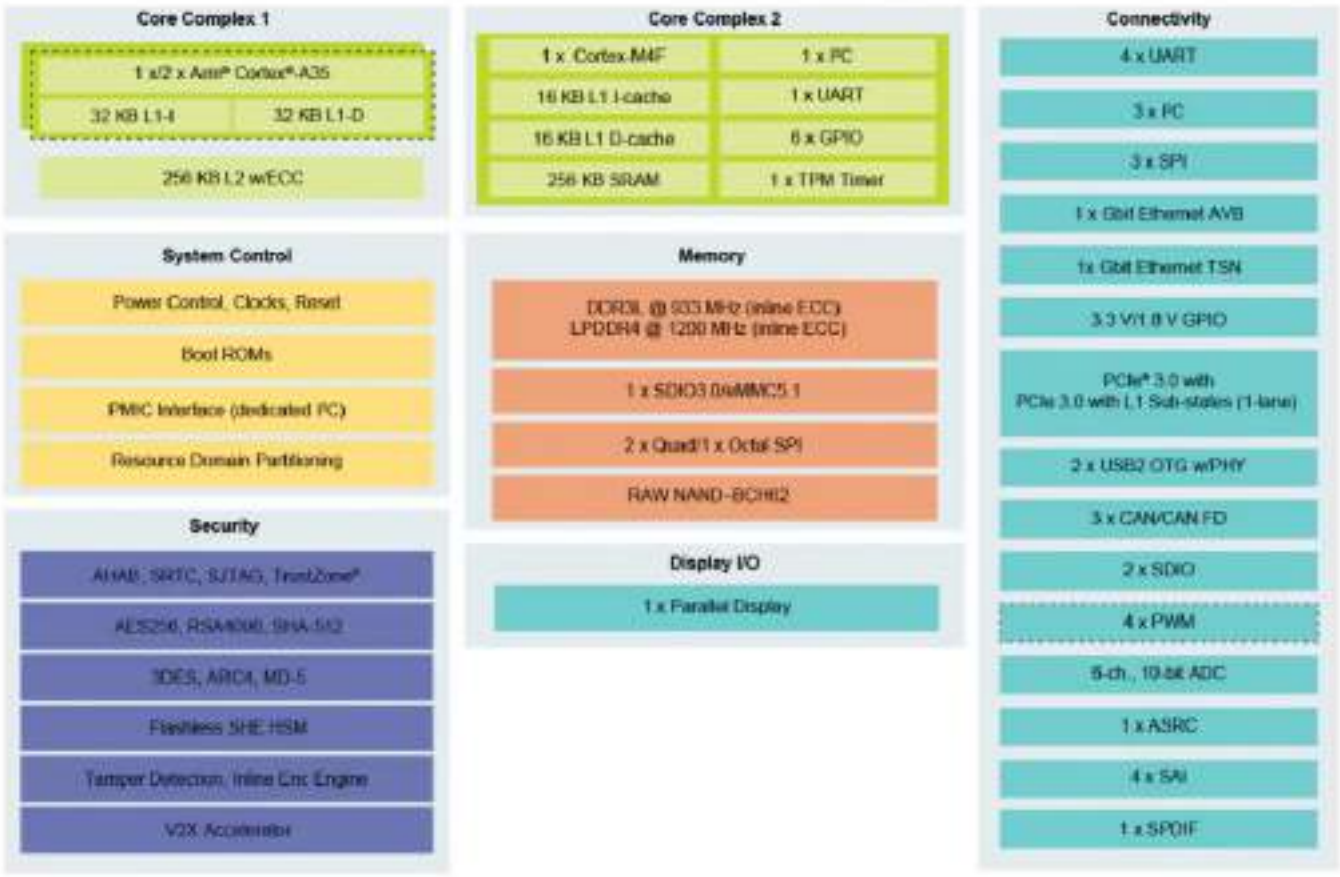

Figure 2: i.MX 8XLite Block Diagram

Note: The i.MX 8XLite processor offers numerous advanced features, please refer the latest i.MX 8XLite Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.5 PMIC

The i.MX 8XLite Pico ITX SBC uses one PF7100 PMIC (U2) for module power management. The PF7100 features five high efficiency step-down regulators and two linear regulators. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PF7100 PMIC comes in 48pin 7x7 QFN Package and is placed on the Top side of the SBC.

2.6 Memory

2.6.1 LPDDR4 RAM

The i.MX 8XLite Pico ITX SBC supports 2GB LPDDR4 RAM memory by default using 16bit DDR_CH0 channel of i.MX 8XLite SoC to support LPDDR4 up to 1.2GHz. LPDDR4 part U5 is placed on Top side of the SBC. To customize the LPDDR4 memory size, contact iWave.

2.6.2 eMMC Flash

The i.MX 8XLite Pico ITX SBC supports 8GB eMMC as default boot and storage device. This is directly connected to eMMC controller of the i.MX 8XLite SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory (U3) is physically located on Top side of the SBC. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.6.3 SPI Flash

The i.MX 8XLite Pico ITX SBC supports SPI Flash through i.MX 8XLite SoC's SPI2 interface. This SPI interface signals are connected to SPI Flash "IS25WP016D-JNLE" and operating at 1.8V Level.

2.7 Boot Media Setting

i.MX 8XLite SoC boot process begins at Power on Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. i.MX 8XLite SoC Boot ROM code uses the state of the internal register BOOT_MODE [1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device.

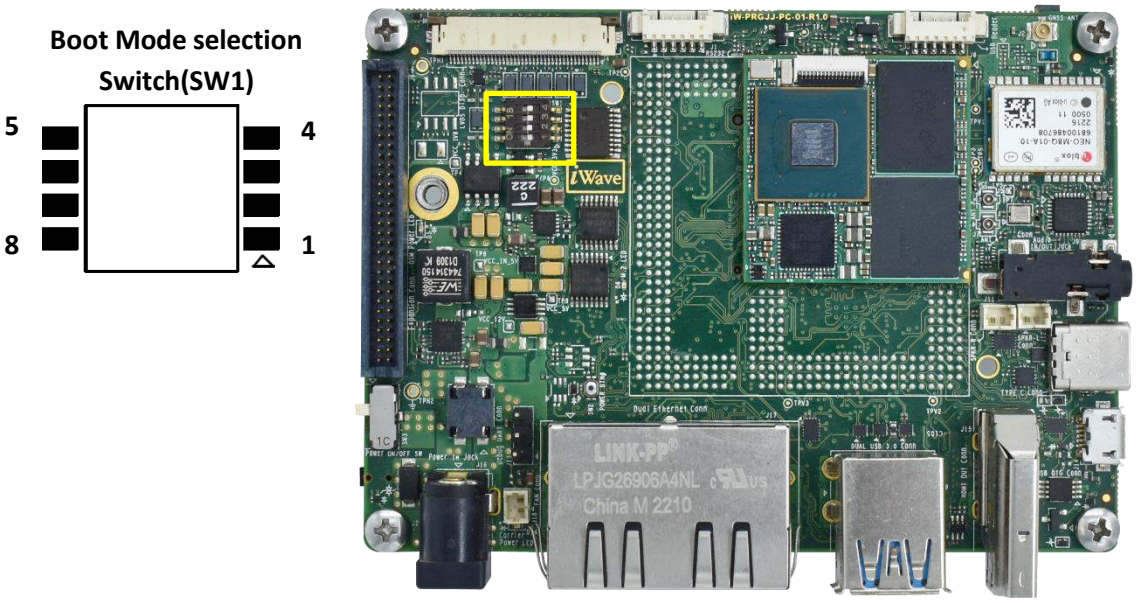

Figure 3: Boot Media Switch

Table 3: Boot Media Settings

Boot Media	Pin number	SW1 (4 Position Switch)
		POS1
eMMC	1	ON
Serial Download mode	1	OFF

2.8 Network & Communication

2.8.1 Gigabit Ethernet Interface

The i.MX 8XLite Pico ITX SBC supports Dual Ethernet Port interface through dual external Ethernet PHY from Atheros, Qualcomm which supports 10/100/1000Mbps Ethernet.

The Ethernet PHY AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary Smart EEE. The Smart EEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

The Ethernet PHY's output signals GBE0 and GBE1 are directly connected to RJ45 Magjack (J17), Left & Right connector respectively. Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. The RJ45 Magjack combo connector is physically located at the top of the board as shown below.

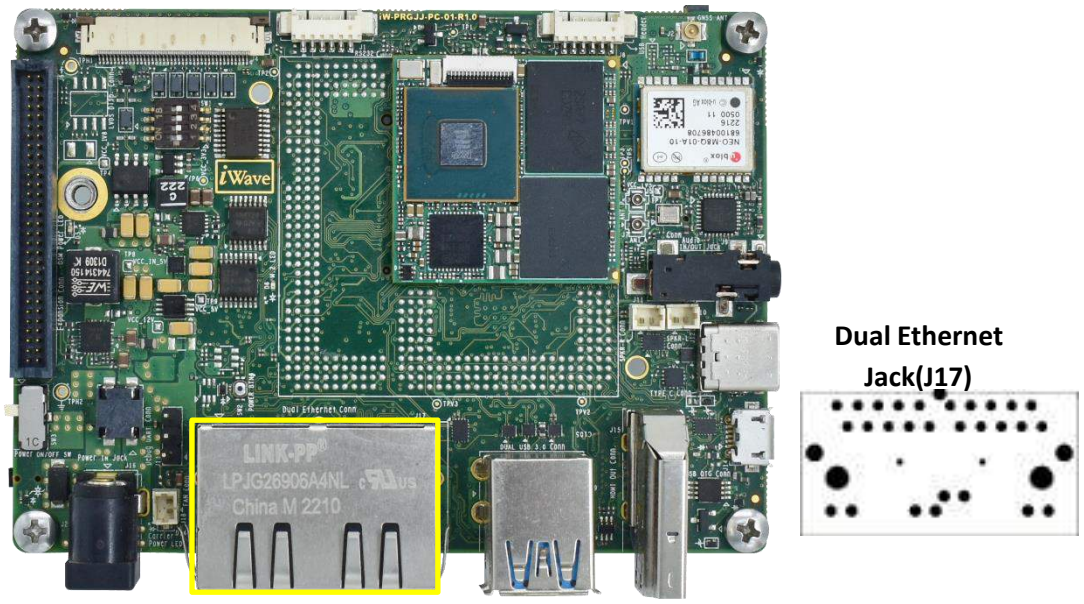

Figure 4: Dual RJ45 Magjack

2.8.2 USB2.0 OTG Interface

The i.MX 8XLite Pico ITX SBC supports USB2.0 OTG interface. This USB2.0 signals is muxed between USB2.0 Micro AB connector (J14) and M.2 key B connector(J28). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status. This USB2.0 OTG connector is physically located at the top of the board as shown below.

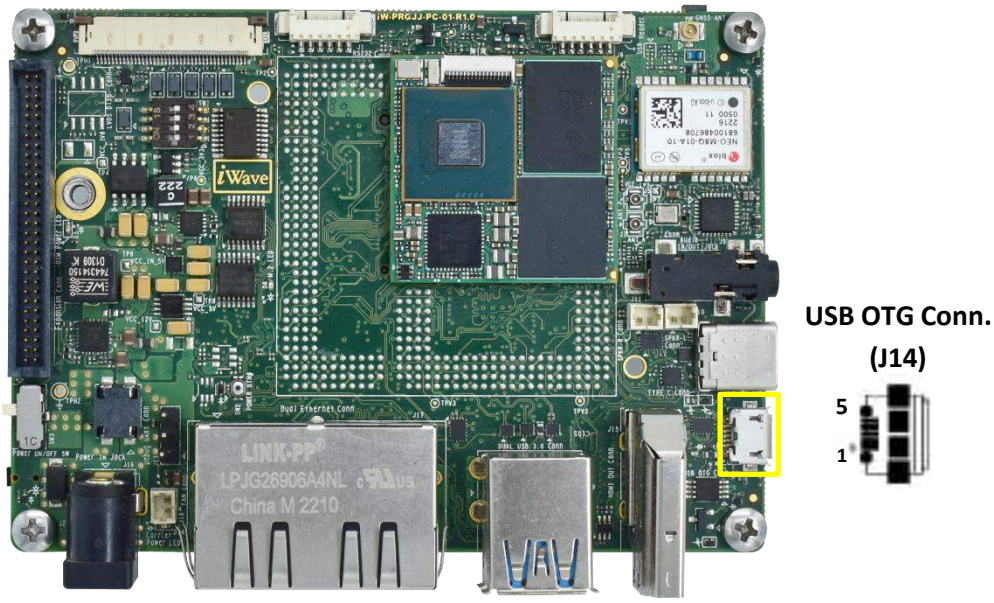

Figure 5: USB OTG Connector

2.8.3 USB2.0 Header

The i.MX 8XLite Pico ITX SBC supports USB2.0 Host interface through a 6pin USB Header. This USB Header(J3) is physically located at the top of the board as shown below.

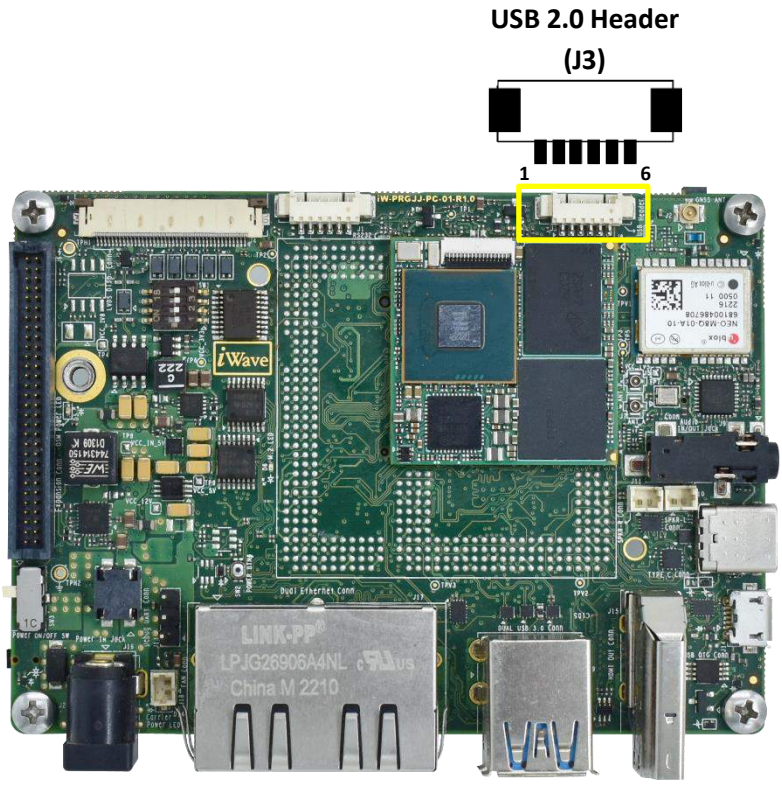

Figure 6: USB Header

Number of Pins : 6

Connector Part : 532610671 from Molex

Table 4: USB Header Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	1	VBUS_HOST_TP	5V. Power	5V Supply Voltage.
2	2	USB_OTG2_DM	I, USB	Differential USB Negative.
3	3	USB_OTG2_DP	I, USB	Differential USB Positive.
4	4	NC	-	NC. *Optional ID pin is available.*
5	5	GND	Power	Ground.
6	6	NC	-	NC.

2.8.4 CAN Interface

The i.MX 8XLite Pico ITX SBC supports Flexible Control Area Network (FLEXCAN) Port from i.MX 8XLite SoC which is connected to MCP2562FD-E/SN CAN Transceiver and CANL & CANH of the transceiver are connected to CAN Header (J23). The Header is placed on bottom side of the SBC.

Number of Pins : 6

Connector Part Number : 532610671 from Molex

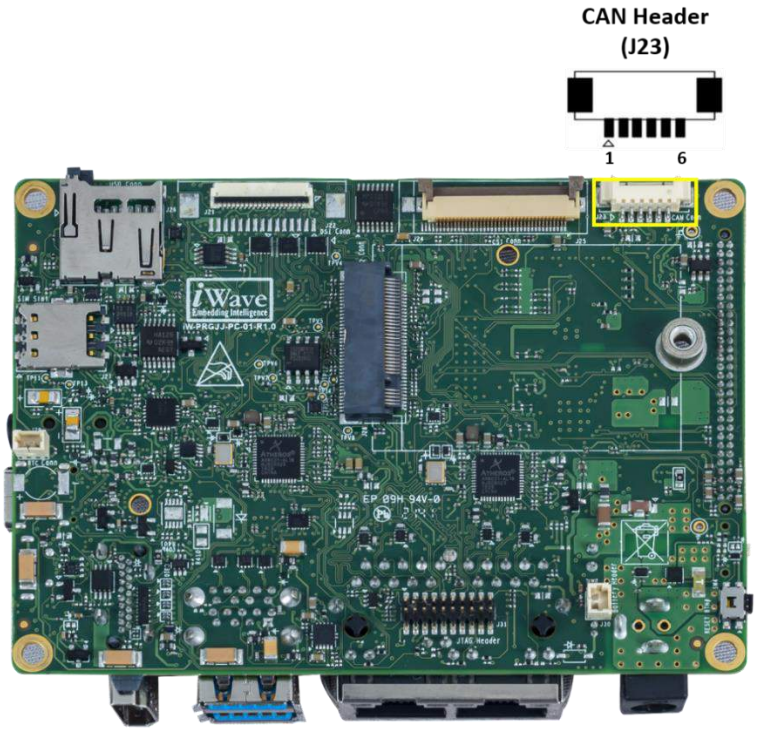

Figure 7: CAN Header

Table 5: CAN Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V_CAN0	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*NC.*
3	CANL	CAN0_L	IO, DIFF	CAN Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN0_H	IO, DIFF	CAN High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.9 Serial Interface Features

2.9.1 Debug UART Interface

The i.MX 8XLite Pico ITX SBC supports debug interface through i.MX 8XLite SoC's UART0 interface. This UART0 signals from the SoC is connected to Debug UART header(J13) through 1.8V to 3.3V level Translator. This Debug UART header can be used for Debug purpose, which is physically located at the top of the board as shown below.

Number of Pins : 3

Connector Part number : M20-9990345 from Harwin

USB to UART Cable : TTL-232R-RPI from FTDI

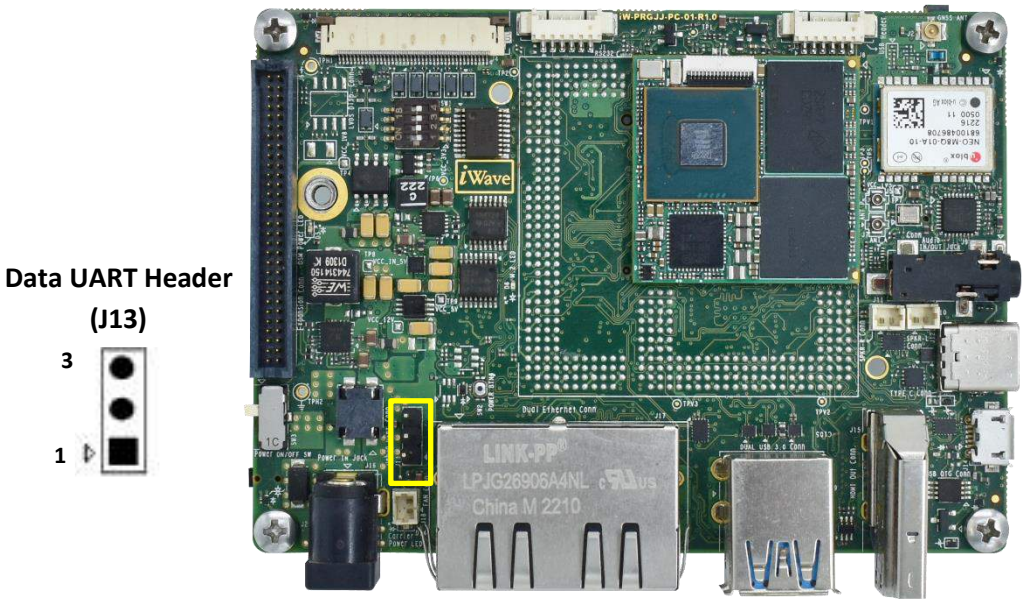

Figure 8: Debug UART Header

Table 6: Debug UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	TX	UART0_RX	O, 3.3V CMOS	UART interface Receive signal.
2	RX	UART0_TX	I, 3.3V CMOS	UART interface Transmit signal.
3	GND	GND	Power	Ground.

2.9.2 RS232 Data UART Interface

The i.MX 8XLite Pico ITX SBC supports RS232 without hardware flow control (CTS/RTS) through i.MX 8XLite SoC's UART3 interface. By default, this UART3 signals from the SoC is connected to "MAX3232" RS-232 Line Driver and Receiver via 1.8V to 3.3V level Translator. The RS232 Signals are connected from MAX3232 to RS232 Header(J1), which is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 532610671 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

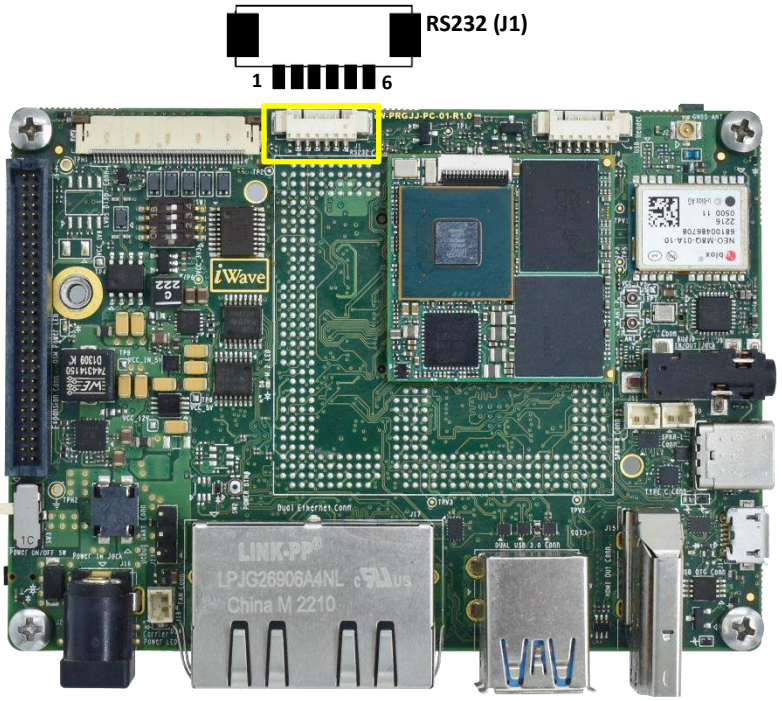

Figure 9: RS232 Header

Table 7: RS232 Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS	-	-	NC.
3	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	TXD	RS232_RXD	O, RS232	RS232 interface Receive signal.
5	RXD	RS232_TXD	I, RS232	RS232 interface Transmit signal.
6	RTS	-	-	NC.

2.10 Audio/Video Features

2.10.1 I2S Audio Interface

The i.MX 8XLite Pico ITX SBC supports Audio IN/OUT through SoC's SAI1 interface which can support I2S format. This four wire I2S signals from the SoC is connected to I2S Audio Codec "SGTL5000" to support CTIA configuration Headphone Stereo output and Mono Mic input through Single 3.5mm audio Jack (J9). The Audio IN/OUT Jack is physically located at the top of the board as shown below.

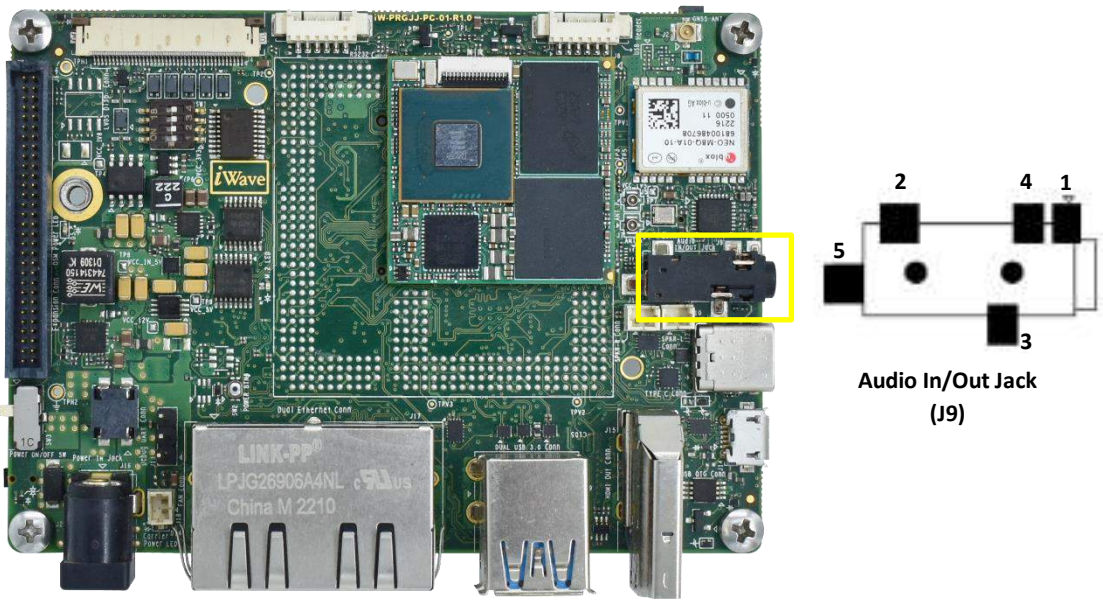

Figure 10: Audio IN/OUT Jack

The i.MX 8XLite Pico ITX SBC supports 3W Audio Amplifier. The LINEOUT signals from "SGTL5000" is connected to an Audio Amplifier. The Output signals from the Amplifier is connected to two Speaker Headers (J10) and (J11). The Speaker Headers is physically located at the top of the board as shown below.

Number of Pins : 2

Connector Part : 10114829-10102LF from Molex

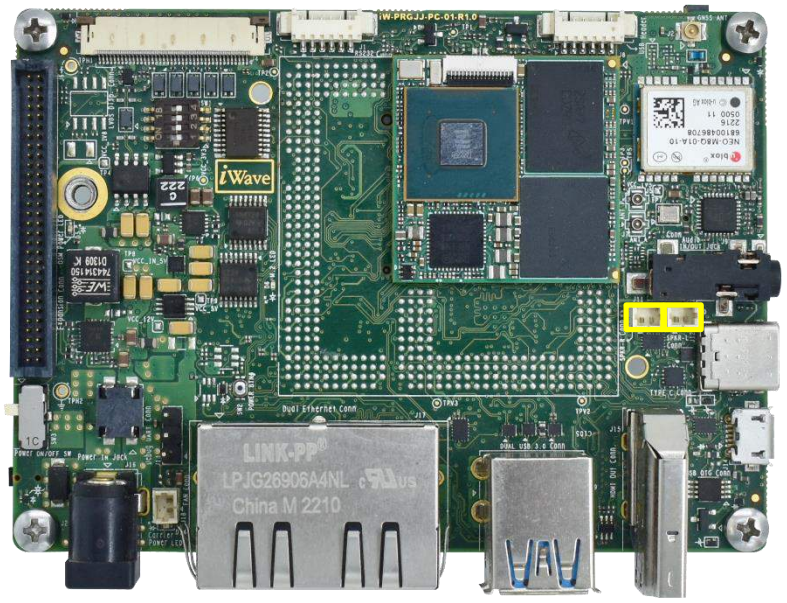

Figure 11: Speaker Headers

Table 8: Speaker Header(J10) Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	SPL+	SPKR_L+	O, Analog Audio	Speaker Left Positive.
2	SPL-	SPKR_L-	O, Analog Audio	Speaker Left Negative.

Table 9: Speaker Header(J11) Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	SPR+	SPKR_R+	O, Analog Audio	Speaker Right Positive.
2	SPR-	SPKR_R-	O, Analog Audio	Speaker Right Negative.

2.11 M.2 Key-B Connector

The i.MX 8XLitePico ITX SBC supports M.2 B key-B socket. M.2 B key-B socket is the Next Generation Form Factor (NGFF) which is designed to support multiple modules and make the M.2 more suitable in application like solid-state storage, WWAN. The M.2 Key B Connector supports PCIe×1, USB 2.0, UIM, I2C and SMBus. The M.2 Key-B Connector (J28) is placed at the bottom side of the board.

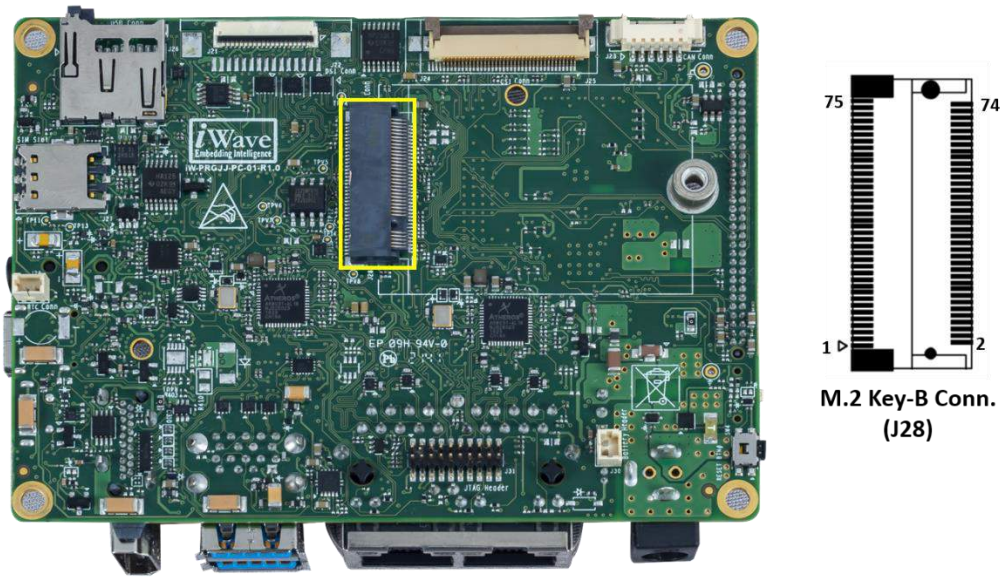

Figure 12: M.2 Key B Connector

The i.MX 8XLite Pico ITX SBC supports a Nano SIM connector to support the WWAN M.2 Modules. The Nano SIM connector (J27) is physically located on the bottom of the board.

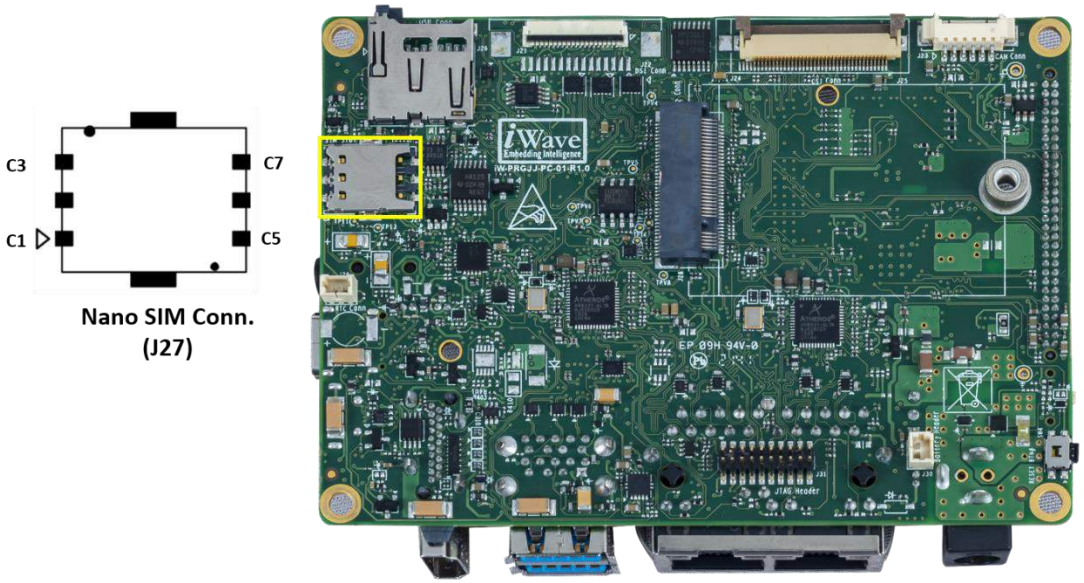

Figure 13: Nano SIM Connector

Table 10: M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	M.2_PWR_OFF#	O, 3.3V CMOS	M.2 Full card Power off Signal.
7	USB_D+	USB_OTG1_DP	IO, USB	USB2.0 PortA Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	M.2_W_DISABLE1#	O, 3.3V CMOS	M.2 Wireless Disable Signal
9	USB_D-	USB_OTG1_DM	IO, USB	USB2.0 PortA Data Minus.
10	GPIO9(LED1#/DAS_DSS#) (I/0)(0/3.3V)	M.2_LED	O, 3.3V CMOS	Provide status indicators via LED.
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	NC	NC	NC.
21	CONFIG_0	M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	NC	NC	NC.
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	NC	NC	NC.
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	NC	NC	NC.
25	DPR (O) (0/1.8V)	M.2_DPR	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	NC	NC	NC.
27	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	NC	NC	NC.
29	PERN1/USB30_RX-/SSIC_RX-	NC	NC	NC.
30	UIM-RESET (I)	M2_UIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	NC	NC	NC.
32	UIM-CLK (I)	M2_UIM_CLK	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	M2_UIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NC	NC.
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NC	NC.
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	I2C2_SCL(SPI1_SDO)	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	PCIE0_A_RX0_N	I,PCIe/SATA	PCIe Port 0 Receive Lane Positive.
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	I2C2_SDA(SPI1_SCK)	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	PCIE0_A_RX0_P	I,PCIe/SATA	PCIe Port 0 Receive Lane Negative.
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	GPIO3_IO13(QSPI0A_DQS)	IO, 1.8V CMOS	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2) (I/O)(0/1.8V)	NC	NC	NC.
47	PETN0/SATA_A-	PCIE0_A_TX0_N	O,PCIe/SATA	PCIe Port 0 Transmit Lane Negative.
48	GPIO4(TX_BLK/GNSS_1/UIM_PWR2)(I/O)(0/1.8V)	NC	NC	NC.
49	PETP0/SATA_A+	PCIE0_A_TX0_P	O,PCIe/SATA	PCIe Port 0 Transmit pair Positive.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
50	PERST# (O)(0/3.3V)	PCIE_RST_B	O, 3.3V CMOS	PCIe Resets Signal.
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	PCIE_CLKREQ_B	IO, 3.3V CMOS	M.2 Clock Request Pin
53	REFCLKN	PCIE_CPU_REFCLK100M_N	O,PCIe	PCIe Channel-A Clock Positive.
54	PEWAKE# (I/O)(0/3.3V)	PCIE_WAKE_B	O, 3.3V CMOS	PCIe Wake Signal
55	REFCLKP	PCIE_CPU_REFCLK100M_P	O,PCIe	PCIe Channel-A Clock Negative.
56	MFG_DATA	I2C2_SDA(SPI1_SCK)	IO, 3.3V CMOS	NC. *Optionally connected I2C Data.*
57	GND	GND	Power	Ground.
58	MFG_CLOCK	I2C2_SCL(SPI1_SDO)	O, 3.3V CMOS	NC. *Optionally connected I2C Clock.*
59	ANTCTL0 (I)(0/1.8 V)	NC	NC	NC.
60	COEX3 (I/O)(0/1.8V)	NC	NC	NC.
61	ANTCTL1 (I)(0/1.8 V)	NC	NC	NC.
62	COEX_TXD (O)(0/1.8V)	NC	NC	NC.
63	ANTCTL2 (I)(0/1.8 V)	NC	NC	NC.
64	COEX_RXD (I)(0/1.8V)	NC	NC	NC.
65	ANTCTL3 (I)(0/1.8 V)	NC	NC	NC.
66	SIM_DETECT (I)	M.2_SIM_DETECT	NC	NC
67	RESET# (O)(0/1.8V)	M.2_RESET(GPIO5_25)	I, 1.8V	M.2 Reset Signal
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK	I, 32.768kHz Clock Supply	*Note: Optionally connected 32.768kHz Clock output*
69	CONFIG_1	M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

Below are the steps for Inserting an M.2 Key B Module to the i.MX 8XLite Pico ITX SBC M.2 Connector

Step 1: Move the Module against housing Chamber.

Step 2: Rotate the Module to 25 Degree and insert until the bottom of the module surface reaches the ramp.

Step 3: Rotate the Module to horizontal Position by hand

Step 4: Fix the module with M3 x4 Screw

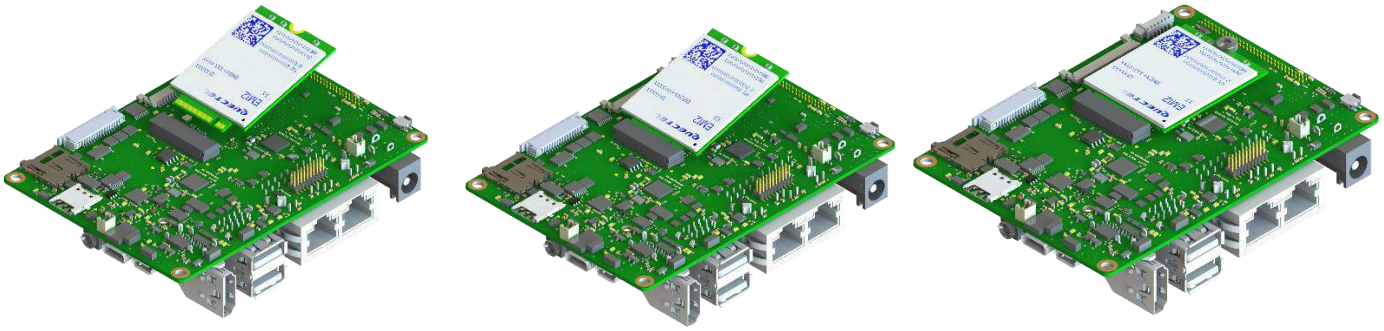

Figure 14: M.2 Module Insertion Guide

2.12 Expansion Connector

The interfaces which are available at 60 Pin Expansion connector are explained in the following section. This Expansion Connector (J6) is physically located at the top of the SBC as shown below.

Number of Pins : 60

Connector Part : TFC-130-01-L-D-A from Samtech

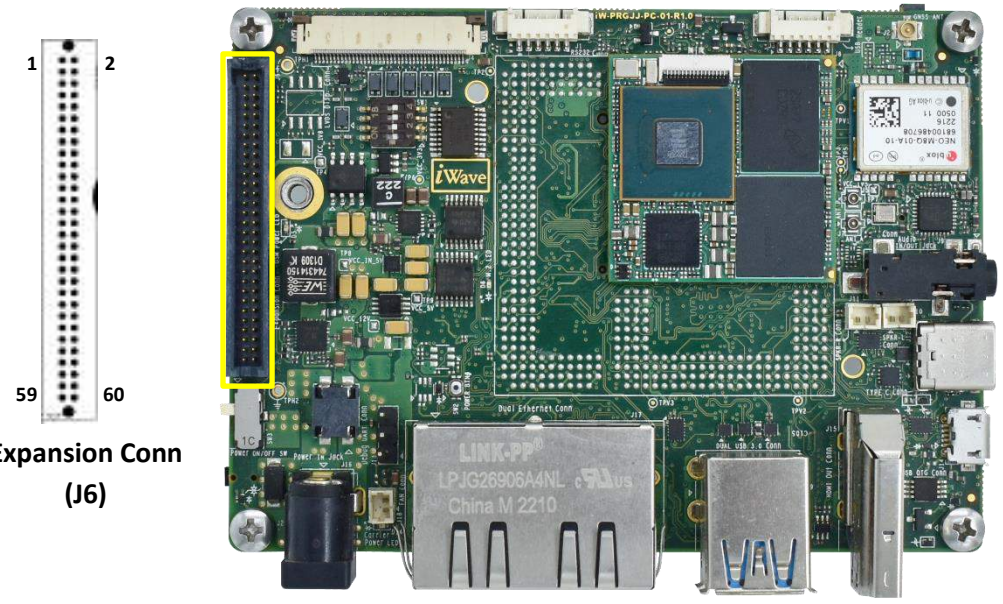

Figure 15: Expansion Connector

Table 11: Expansion Connector Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	SNVS_TAMPER_IN4	SNVS_TAMPER_IN4/AJ 13	1.8V, 100K PD	Tamper IN4
2	NC	-	-	NC.
3	SNVS_TAMPER_OUT0	SNVS_TAMPER_OUT0/ AP22	1.8V, 100K PD	Tamper OUT0
4	NC	-	-	NC.
5	GND	-	Power	Ground
6	GND	-	Power	Ground
7	UART2_RX	UART2_RX/AN33	I, 1.8V CMOS	Optional *By default, connected to CAN*
8	NC	-	-	NC.
9	UART2_TX	UART2_TX/AP34	O, 1.8V CMOS	Optional *By default, connected to CAN*
10	NC	-	-	NC.
11	NC	-	-	NC.
12	GND	-	Power	Ground
13	NC	-	-	NC.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
14	NC	-	-	NC.
15	GND	-	Power	Ground
16	NC	-	-	NC.
17	NC	-	-	NC.
18	GND	-	Power	Ground
19	NC	-	-	NC.
20	NC	-	-	NC.
21	NC	-	-	NC.
22	NC	-	-	NC.
23	NC	-	-	NC.
24	GND	-	Power	Ground
25	GND	-	Power	Ground
26	NC	-	-	NC.
27	NC	-	-	NC.
28	NC	-	-	NC.
29	NC	-	-	NC.
30	GND	-	Power	Ground
31	NC	-	-	NC.
32	NC	-	-	NC.
33	NC	-	-	NC.
34	NC	-	-	NC.
35	NC	-	-	NC.
36	NC	-	-	NC.
37	NC	-	-	NC.
38	NC	-	-	NC.
39	NC	-	-	NC.
40	NC	-	-	NC.
41	NC	-	-	NC.
42	NC	-	-	NC.
43	FLEXCAN2_TX	FLEXCAN2_TX/AL33	O, 1.8V	CAN Transmitter
44	NC	-	-	NC.
45	FLEXCAN2_RX	FLEXCAN2_RX/AL35	I,1.8V	CAN Receiver
46	NC	-	-	NC.
47	NC	-	-	NC
48	NC	-	-	NC.
49	NC	-	-	NC
50	NC	-	-	NC.
51	GND	-	Power	Ground
52	NC	-	-	NC.
53	VCC_5V	-	Power	5V Supply Voltage
54	NC	-	-	NC.
55	VCC_3V3	-	Power	3.3V Supply Voltage

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
56	VCC_1V8	-	Power	1.8V Supply Voltage
57	VCC_3V3	-	Power	3.3V Supply voltage
58	VCC_12V	-	Power	12V Supply Vlotage
59	NC	-	-	NC.
60	GND	-	Power	Ground

*Note: Refer GPIO Column under **"i.MX 8XLite Pin Multiplexing on Expansion Connector** for details on GPIO options available from Expansion connector.*

2.13 Other Features

2.13.1 Fan Header

The i.MX 8XLite Pico ITX SBC supports a Fan Header to connect cooling Fan if required. This Fan Header (J18) is physically located at the top of the board as shown below.

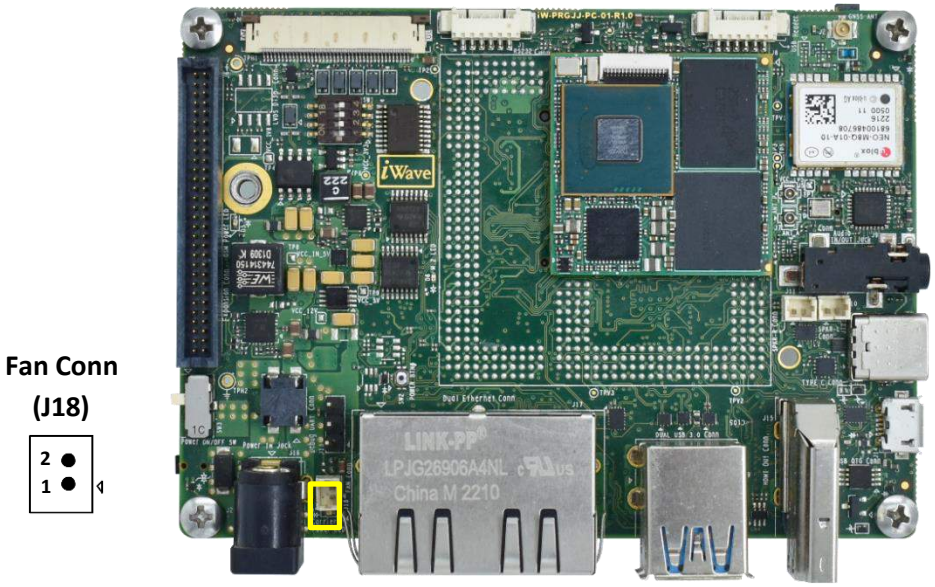

Figure 16: Fan Connector

Number of Pins : 2

Connector Part :10114829-10102LF from Amphenol ICC (FCI)

Table 12: Fan Connector Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN. *Note: Optional 12V power is available.*
2	GND	Power	Ground.

Note: Contact iWave support team if 12V Power Support is required for FAN Header support is required.

2.13.2 RTC Battery Header

The i.MX 8XLite Pico ITX SBC supports external RTC cell. The SBC supports 2pin connector for backup battery or coin cell connection. The 2pin RTC (J29) battery connector is physically located on top side of the SBC as shown below.

The i.MX 8XLite Pico ITX SBC optionally supports external RTC Controller "PCF85263" for Real time clock support. This external RTC Controller IC is connected to i.MX 8XLite SoC through I2C3 Interface and operates at 3.3V voltage level.

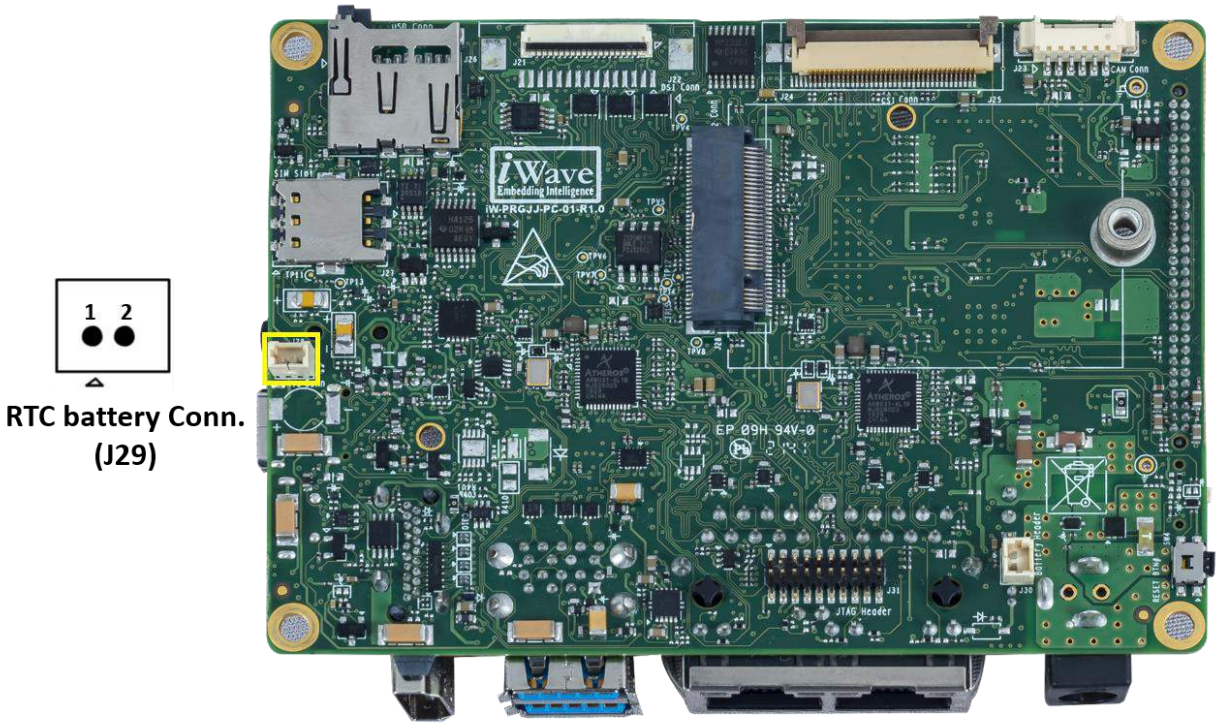

Figure 17: RTC Battery Connector

Number of Pins : 2

Connector Part : 10114829-10102LF from Amphenol ICC (FCI)

Table 13: RTC Battery Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VRTC_3V0	I, Power	+3V Power Input
2	GND	Power	Ground.

Note: Contact iWave support team if External RTC Controller support is required.

2.13.3 JTAG Interface

The supports JTAG interface for CPU debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security.

JTAG Header (J31) is physically located on bottom side of the board.

Number of Pins - 20

Connector Part - 62132021021 from Wruth Electronics.

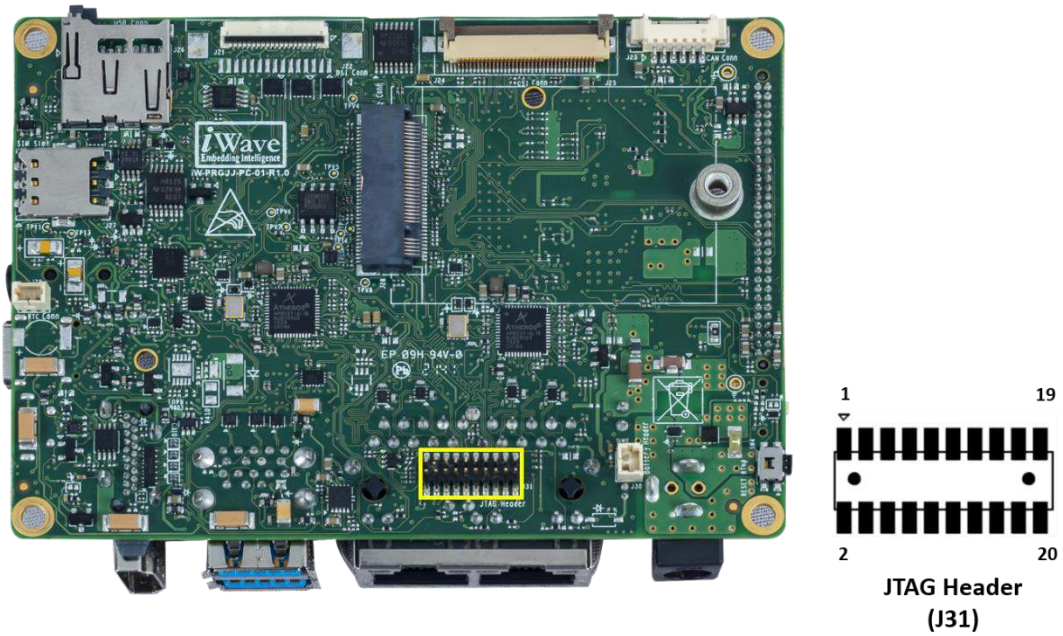

Figure 18: JTAG Header

Table 14: JTAG Header Pin Assignment

Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_1V8	-	O, 1.8V Power	VTREF Voltage Reference.
2	VCC_1V8	-	O, 1.8V Power	Supply Voltage.
3	JTAG_TRSTB	POR_B/AR29	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	-	Power	Ground.
5	JTAG_TDI	JTAG_TDI/AR31	I, 1.8V CMOS	JTAG test data input.
6	GND	-	Power	Ground.
7	JTAG_TMS	JTAG_TMS/AP32	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
8	GND	-	Power	Ground.
9	JTAG_TCK	JTAG_TCK/AR33	I, 1.8V CMOS/ 10K PD	JTAG test Clock.
10	GND	-	Power	Ground.
11	-	-	10K PD	
12	GND	-	Power	Ground.
13	JTAG_TDO	JTAG_TDO/AN31	O, 1.8V CMOS	JTAG test data output.
14	GND	-	Power	Ground.
15	-	-	10K PU	

Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
16	GND	-	Power	Ground.
17	-	-	10K PU	Only pull up is provided.
18	GND	-	Power	Ground.
19	-	-	10K PD	Only pull down is provided.
20	GND	-	Power	Ground.

2.13.4 Power ON/OFF Switch

The i.MX 8XLite Pico ITX SBC has power ON/OFF switch (SW3) to control the Main power Input ON/OFF functionality. The Power ON/OFF switch is physically located at the top of the board as shown below.

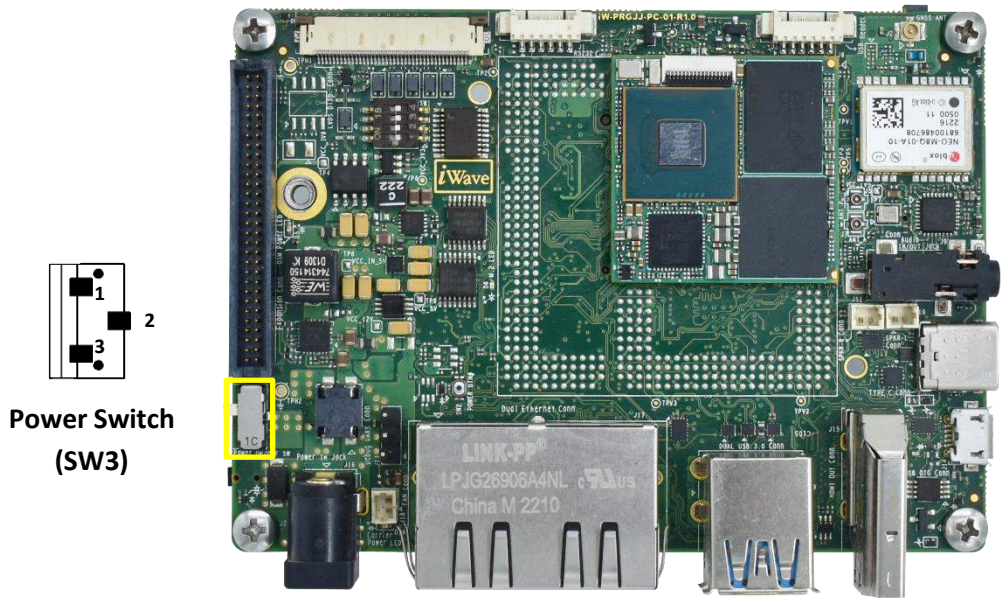

Figure 19: Power ON/OFF Switch

2.13.5 Reset Switch

The i.MX 8XLite Pico ITX SBC supports Push button switch (SW4) to reset the i.MX 8XLite CPU. Reset signal is directly connected from Reset Push button switch. This Reset Push button switch is physically located at the bottom of the board as shown below.

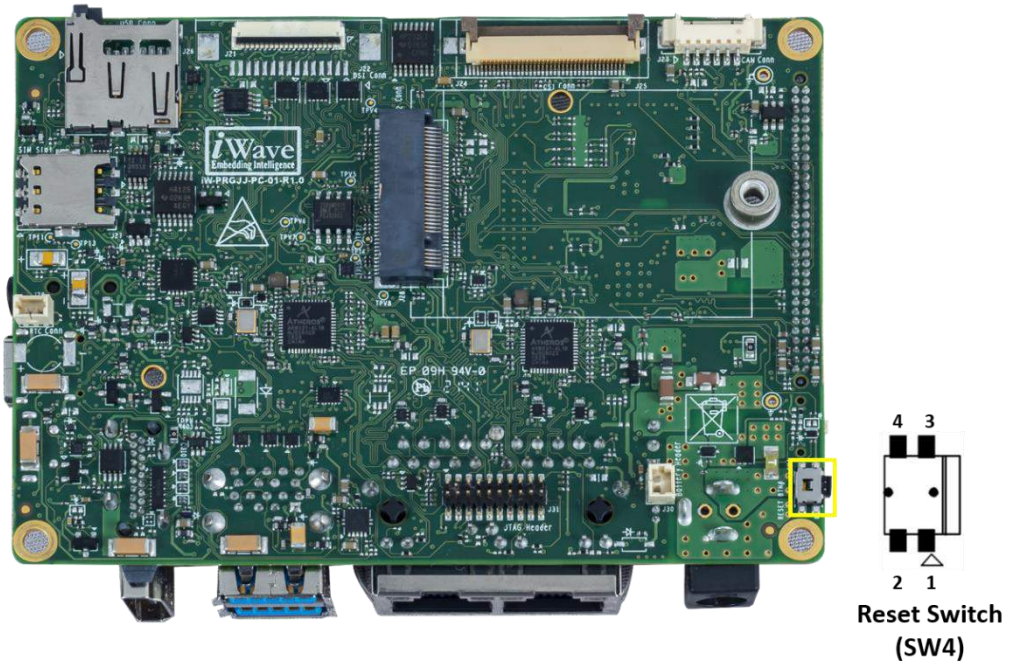

Figure 20: Reset Switch

2.13.6 CPU ON/OFF Switch

The i.MX 8XLite Pico ITX SBC supports Push button switch (SW2) for ON/OFF of the i.MX 8Xlite CPU. The CPU ON/OFF signal is directly connected from ON/OFF Push button switch. This ON/OFF Push button switch is physically located at the top of the board as shown below.

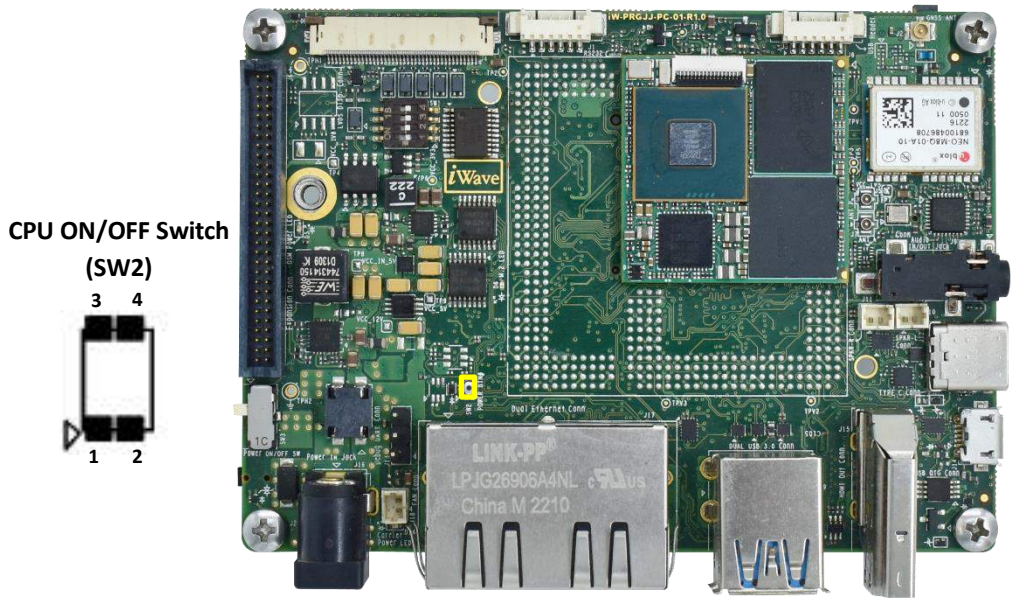

Figure 21: CPU ON/OFF Switch

2.14 i.MX 8XLite Pin Multiplexing on Expansion Connector

The i.MX 8XLite SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8XLite SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8XLite SoC pin connections to the expansion connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8XLite Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SBC for iWave's BSP reusability and to have compatible SBCs in future for upgradability.

Table 15: i.MX 8XLite SoC IOMUX for Expansion Connector Interfaces

Interface	Expansion Connector Pin Number	i.MX 8XLite SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Default
CAN2	45	AL35	ADMA.FLEXCAN2.RX	ADMA.SAI3.RXD	ADMA.UART3.RX	ADMA.SAI1.RXFS	LSIO.GPIO1.IO19	LSIO.GPIO6.IO12	ADMA.FLEXCAN2.RX
	43	AL33	ADMA.FLEXCAN2.TX	ADMA.SAI3.RXFS	ADMA.UART3.TX	ADMA.SAI1.RXC	LSIO.GPIO1.IO20	LSIO.GPIO6.IO13	ADMA.FLEXCAN2.TX
TAMPER	3	AP22	SNVS_TAMPER_OUT0						SNVS_TAMPER_OUT0
	1	AJ13	SNVS_TAMPER_IN4						SNVS_TAMPER_IN4

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8XLite Pico ITX SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The i.MX 8XLite Pico ITX SBC supports 7V to 24V external power and uses on board voltage regulators for internal power management. By default, it supports to work with 12V power input. 12V power input from an external power supply is connected to the i.MX 8XLite Pico ITX SBC (J20). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. The Power Jack is physically placed at the top of the board as shown below.

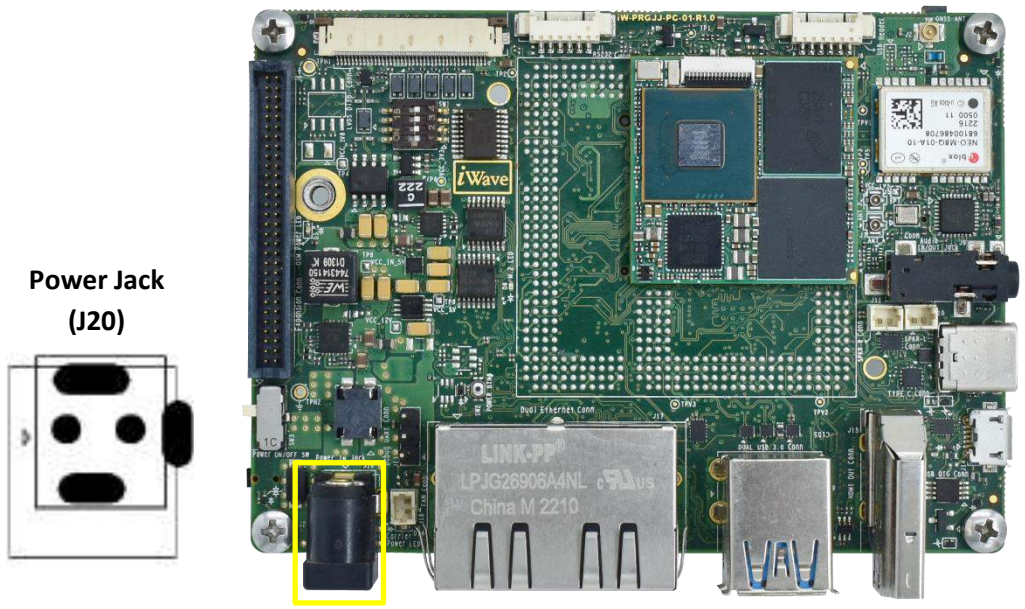

Figure 22: Power Input Jack

Table 16: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[1]	2.8V	3V	3.3V	±20mV

[1] *The i.MX 8XLite Pico ITX SBC uses this voltage as backup power source to PMIC RTC controller when VCC is off.*

3.2 Power Consumption

Table17: i.MX 8XLite Pico ITX SBC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Audio	VCC_12V	0.144/1.728
Ping Ethernet (Eth0) at 1000Mbps	VCC_12V	0.22/2.64
Ping Ethernet (Eth1) at 1000Mbps	VCC_12V	0.198/2.376
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_12V	0.212/2.544
eMMC to USB2.0 file transfer	VCC_12V	0.227/2.724
eMMC to USB2.0 OTG file transfer	VCC_12V	0.257/3.084
eMMC to M.2 PCIe file transfer	VCC_12V	0.23/2.76
File Transfer - Transfer the 1GB files in storage devices	VCC_12V	0.411/4.932
Dhrystone	VCC_12V	0.193/2.316
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background	VCC_12V	0.489/5.868
Low Power Mode Power Consumption		
System Idle Mode.	VCC_12V	0.113/1.356
Deep Sleep Mode.	VCC_12V	0.076/0.912
RTC power when no VCC_12V supply is provided	VRTC_3V0	0.0000005/0.0000015

[1] Power consumption measurements have been done in iWave's i.MX 8XLite based Pico ITX SBC with iWave's iW-PRGWZ-SC-01-R2.0-REL1.0-Linux5.15.52 BSP.

3.3 EnvironmentalCharacteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 8XLite Pico ITX SBC.

Table 18: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2] For more information on Thermal solution & Heat sink refer the following section.

3.3.1 Heat Sink

For any highly integrated SBC, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink or Fan Sink must be used. Always need to remember that more effective thermal solution will give more performance out of the CPU.

Note: iWave supports Heat Sink Solution for i.MX 8XLite Pico ITX SBC. For more information on Heat Sink& Fan Sink contact iWave support team. Do not Power On the i.MX 8XLite Pico ITX SBC without a proper thermal solution.

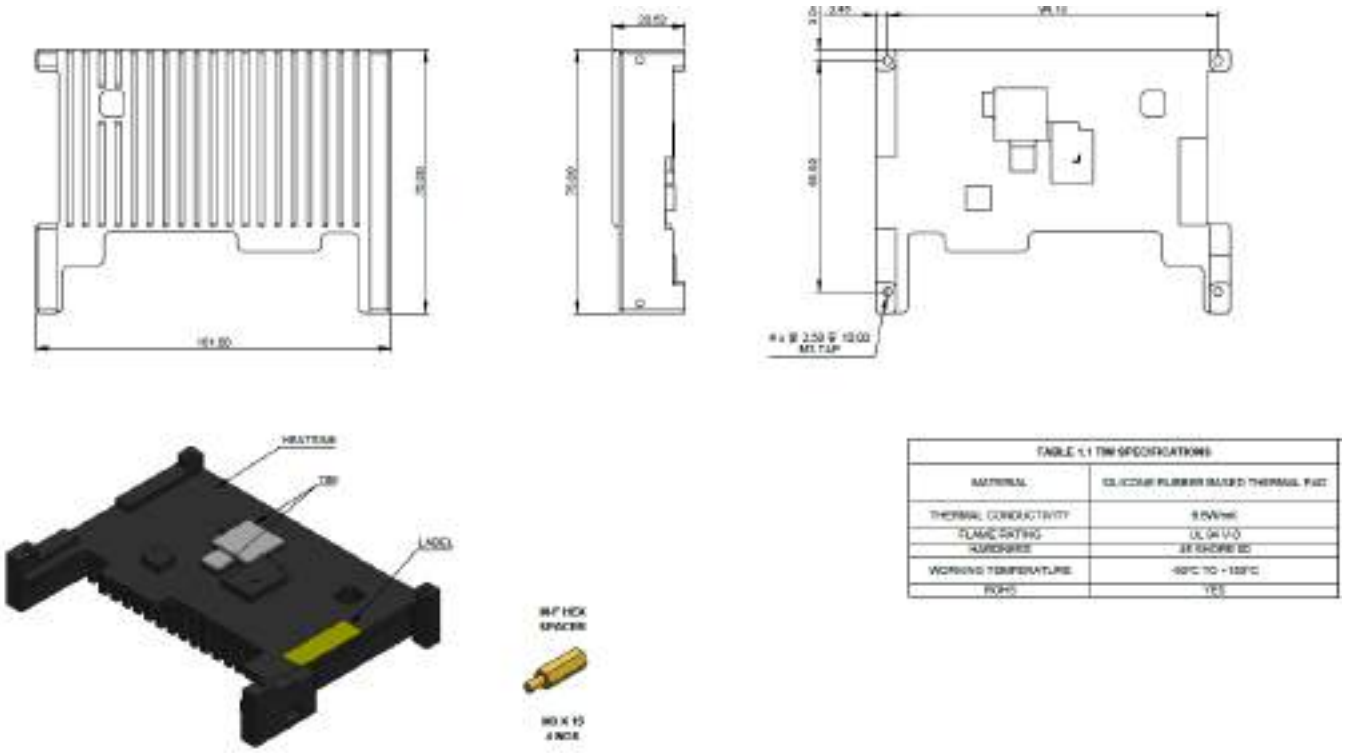

Figure 23: Mechanical dimension of Heat Sink

3.3.2 RoHS Compliance

iWave's i.MX 8XLite Pico ITX SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's i.MX 8XLite Pico ITX SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8XLite Pico ITX SBC Mechanical Dimensions

i.MX 8XLite Pico ITX SBC PCB size is 100mm x 72mm x 1.2mm. Pico ITX SBC mechanical dimension is shown below. (All dimensions are shown in mm)

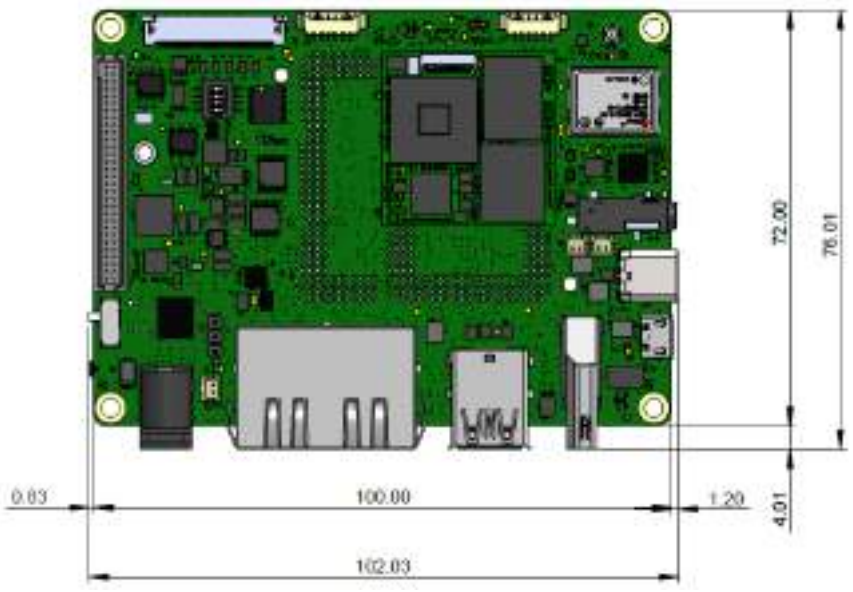

Figure 24: Mechanical Dimensions of i.MX 8XLite Pico ITX SBC Top View

The i.MX 8XLite Pico ITX SBC PCB thickness is 1.2mm±0.15mm, top side maximum height component is 16.40mm (HDMI Connector), followed by Dual Ethernet Connector (16.40mm). In bottom side maximum height component is JTAG connector (5.91mm) followed by M.2 SMT spacer (3.99mm).

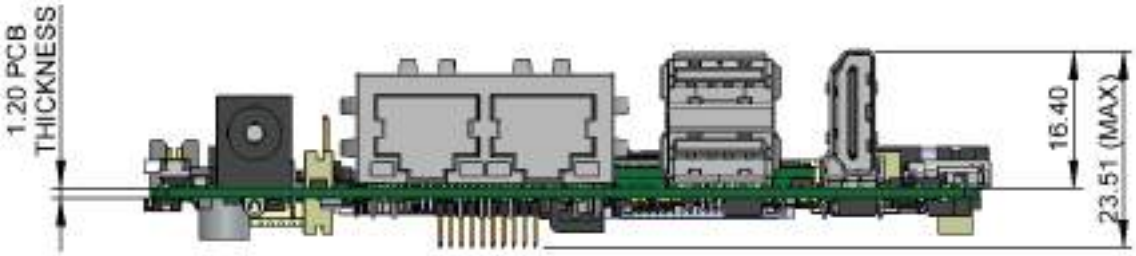

Figure 25: Mechanical Dimensions of i.MX 8XLite Pico ITX SBC Side View-1

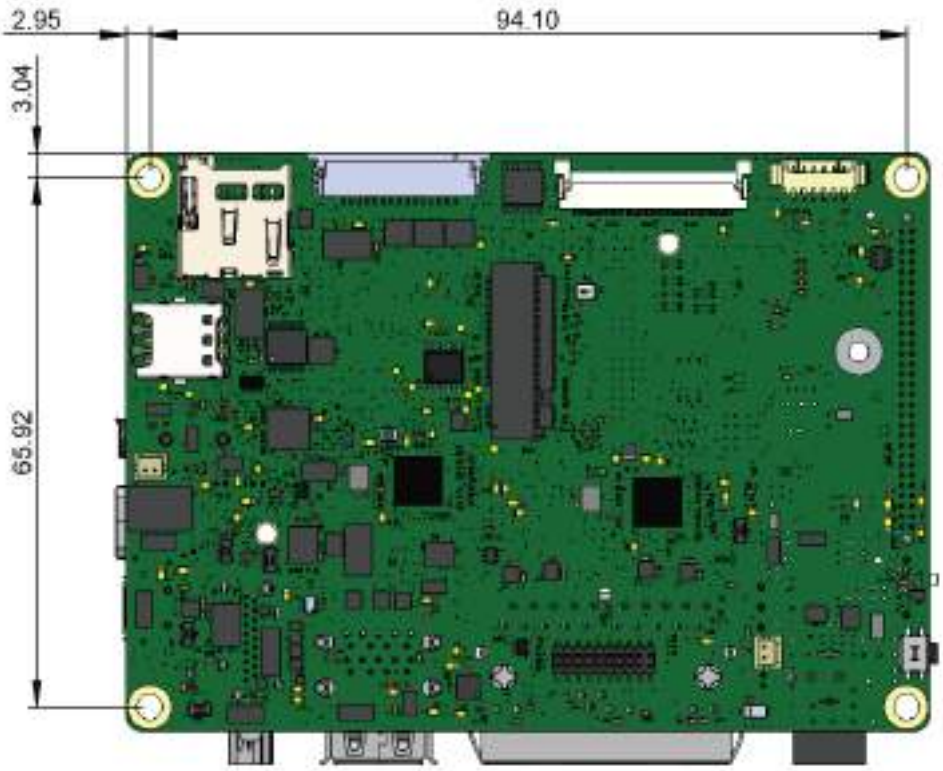

Figure 26: Mechanical Dimensions of i.MX 8XLite Pico ITX SBC Bottom View

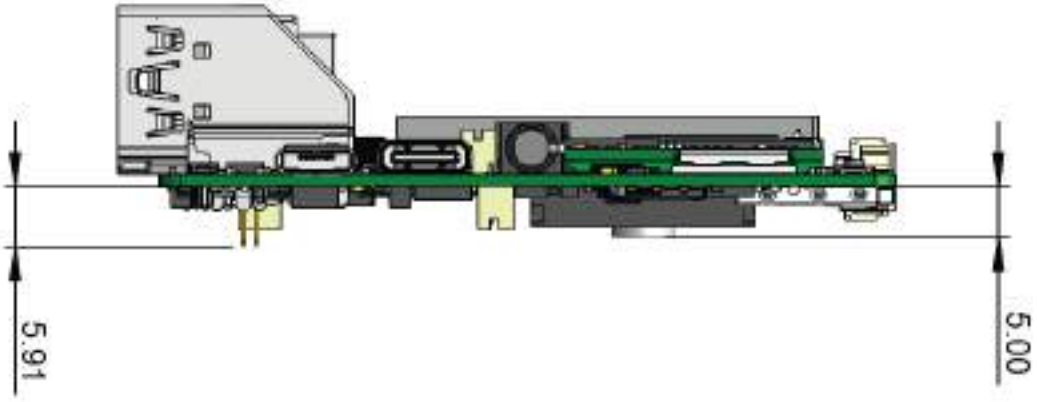

Figure 27: Mechanical Dimensions of i.MX 8XLite Pico ITX SBC Side View-2

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8XLite Pico ITX SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 19: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G46S - i.MX 8XLite Pico ITX SBC		
iW-G46S-OSXD-4L002G-E008G-BIB	i.MX8X Lite Dual, 2GB LPDDR4, 8GB eMMC	-40°C to 85°C

Important Note: Some of the above-mentioned Part Numbers are subject to MOQ purchase. Please contact iWave for further details.

For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.


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