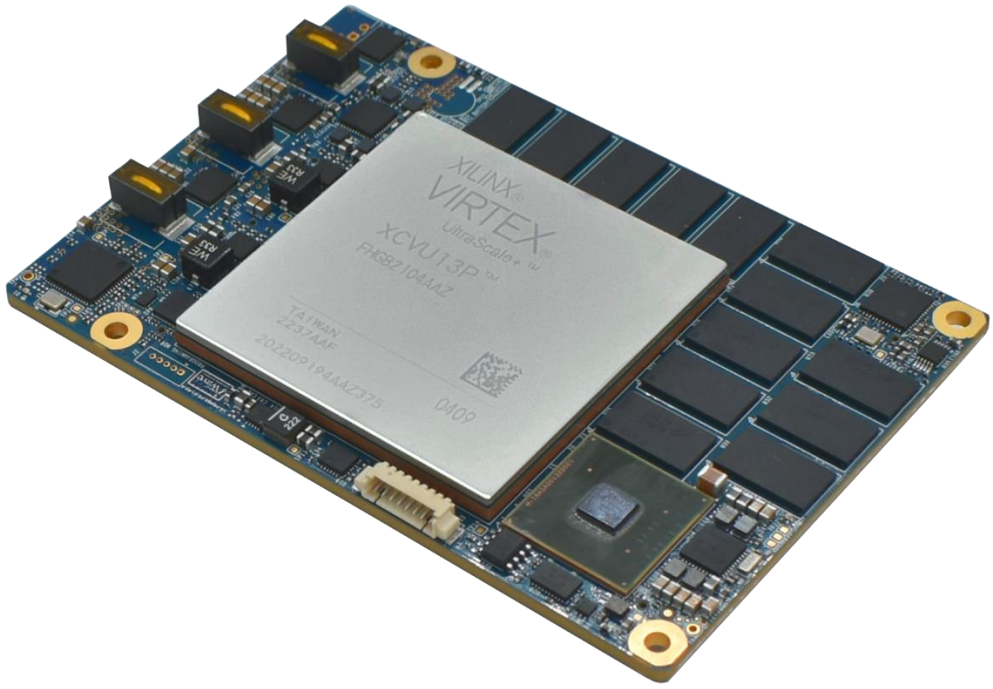
iW-RainboW-G47M
Virtex UltraScale+ FPGA SOM
Datasheet



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Document Revision History

Document Number		iW-PRHBZ-UM-01-R2.0-REL0.1-FPGA-SOM-Datasheet
Release	**Date**	**Description**
0.1	21st July 2023	Initial Draft Version

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware datasheet for the Virtex UltraScale+ FPGA System on Module based on the Xilinx Virtex UltraScale+ FPGA. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This datasheet provides detailed information on the overall design and usage of the Virtex UltraScale+ FPGA System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The Virtex UltraScale+ FPGA SOM is integrated with Xilinx VU13P/VU11P/VU9P/VU7P/VU5P/VU080/VU095/VU160/VU190 FPGA SoC and NXP's LS1021A Layerscape Processor. Virtex UltraScale+ FPGA SOM has a form factor of 110mm x 75mm and provides the functional requirements for an embedded application. Two high speed ruggedized terminal strip connectors and Two High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Virtex UltraScale+ FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
GB	Giga Byte
Gbps	Gigabits per sec
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IFC	Integrated Flash Controller
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
MRAM	Magneto-resistive Random Access Memory
PBL	Pre-boot Loader
PCB	Printed Circuit Board
PL	Programmable Logic
PMIC	Power Management Integrated Circuit
PS	Processing System
RCW	Reset Configuration Word
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SRAM	Static Random Access Memory
TPM	Trusted Platform Module

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

1.5 References

- Virtex UltraScale+ FPGA Technical Reference Manual
- Virtex UltraScale+ FPGA Device Overview
- Virtex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics
- QorIQ LS1021A Reference Manual
- QorIQ LS1021A Data Sheet

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Virtex UltraScale+ FPGA SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Virtex UltraScale+ FPGA SOM Block Diagram

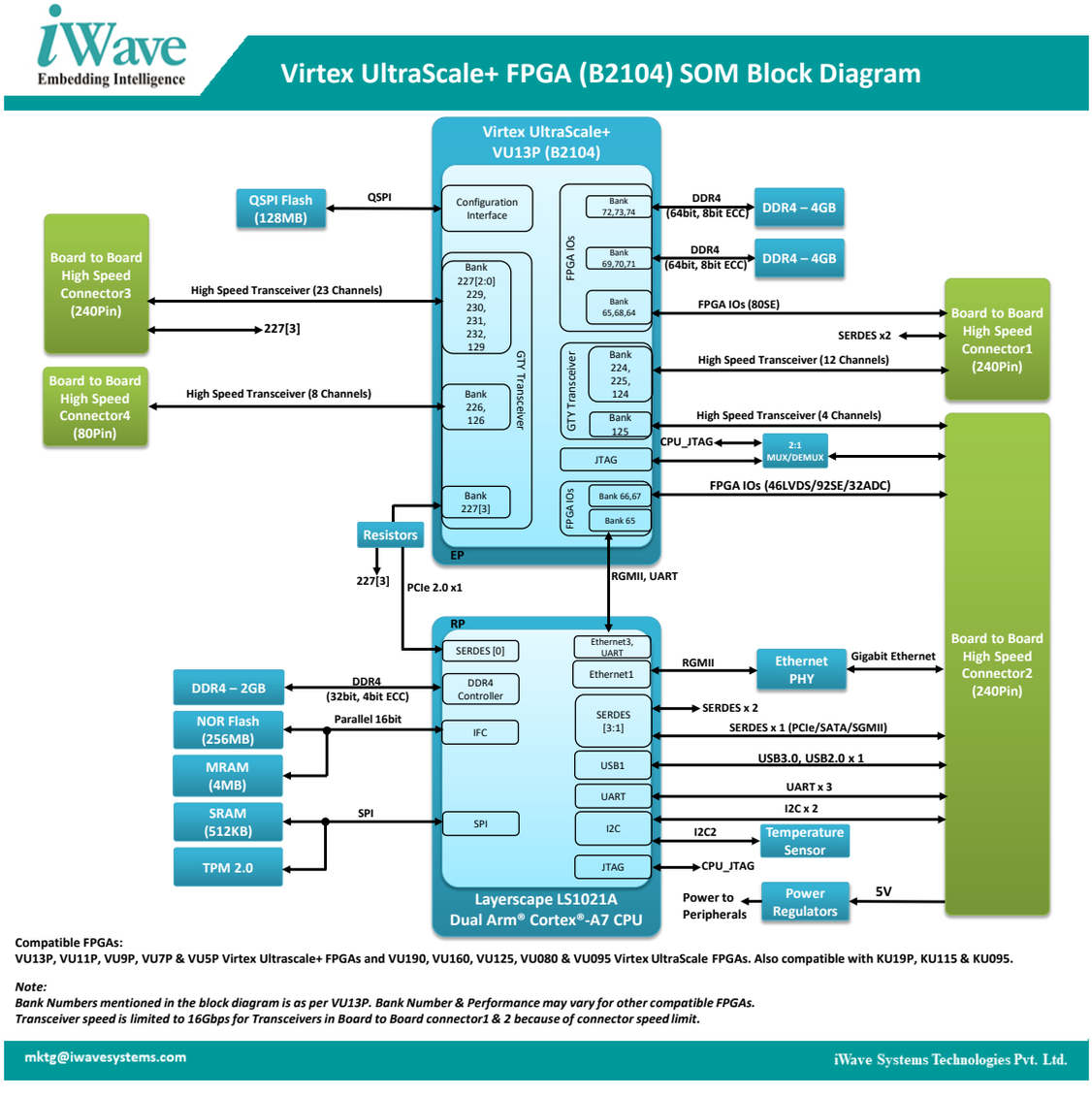


Figure 1: Virtex UltraScale+ FPGA SOM Block Diagram

2.2 Virtex UltraScale+ FPGA SOM Features

The Virtex UltraScale+ FPGA SOM supports the following features.

FPGA

- Xilinx Virtex UltraScale+ FPGA
  - Virtex UltraScale+ FPGA (FHGB2104) Package
  - Compatible with Virtex UltraScale+ VU13P, VU11P, VU9P, VU7P, VU5P and Virtex UltraScale VU080, VU095, VU125, VU160, VU190
  - System Logic cells up to 3,780K Logic cells and up to 3,456K Configurable Logic Blocks.
  - Gen3 x16 Integrated PCIe block for 100G applications
  - 150G Interlaken, 100G Ethernet MAC cores for high-speed connectivity

PMIC

- Dialog's DA9062 PMIC

Memory

- 4GB DDR4 SDRAM1 (64bit) with 8-bit ECC (Expandable)
- 4GB DDR4 SDRAM2 (64bit) with 8-bit ECC (Expandable)
- 128MB QSPI Flash.

CPU

- QorIQ LS1021A Processor
  - Arm® Cortex®-A7 MPCore compliant with Armv7-A™ architecture. LS1021A contains a dual-core Cortex-A7 cores running up to 1.2 GHz
  - 32 KB instruction and data L1 cache with single bit error detection and correction, ECC protection on both instruction and data caches
  - Up to 512 KB coherent L2 cache with single bit error detection and correction, ECC protection

PMIC

- Dialog's DA9062 PMIC (with RTC)

Memory

- 2GB DDR4 SDRAM (32bit) with 4-bit ECC
- 256MB NOR Flash (16bit)
- 4MB MRAM (16bit)

- 512KB SRAM

FPGA to CPU Interfaces

- PCIex1 Gen2
- RGMII
- UART
- Interrupt Request Pins

Other On-SOM Features

- TPM 2.0 Module
- Temperature Sensor
- Gigabit Ethernet PHY Transceiver
- Clock Synthesizer for On-SOM Clocks
- Fan Header

Board to Board Connector1 Interfaces (240pin)

From LS1021A

- 2 SerDes lane for high-speed peripheral (PCIe/SGMII) with reference clock
- 6 GPIOs From LS1021A

From FPGA

- GTY High Speed Transceivers (up to 32.75Gbps) x 12
- FPGA IOs - HP Bank 64
  - Up to 22 LVDS/44 Single ended (SE) IOs
    - Up to 4 pairs of Global Clock Input pins
    - Up to 28 ADC Input pins (Differential/Single Ended)
- FPGA IOs - HP Bank 68
  - Up to 12 LVDS/24 Single ended (SE) IOs
    - Up to 2 pairs of Global Clock Input pins
    - Up to 16 ADC Input pins (Differential/Single Ended)
- FPGA IOs - HP Bank 65
  - Up to 12 Single ended (SE) IOs
    - Up to 7 Global Clock Input pins (SE)

Board to Board Connector2 Interfaces (240pin)

From LS1021A

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY)
- USB2.0 x 1 Port
- USB 3.0 x 1 Port
- Debug UART x 1 Port
- Data UART x 2 Port
- I2C x 2 Ports
- JTAG x1 Port
- Up to 1 SerDes lanes for high-speed peripheral interfaces (SATA, SGMII)
- 11 GPIOs From LS1021A

From FPGA

- GTY High Speed Transceivers (up to 32.75Gbps) x 4
- FPGA IOs - HP Bank 66[1]
  - Up to 24 LVDS IOs/48 Single ended (SE) IOs
    - Up to 4 pairs of Global Clock Input pins
    - Up to 16 ADC Input pins (Differential/Single Ended)
- FPGA IOs - HP Bank 67
  - Up to 22 LVDS IOs/44 Single ended (SE) IOs
    - Up to 4 pairs Global Clock Input pins
    - Up to 15 ADC Input pins (Differential/Single Ended)

Board to Board Connector3 Interfaces (240pin)

From FPGA

- GTY High Speed Transceivers (up to 32.75Gbps) x 24[2]

Board to Board Connector4 Interfaces (80pin)

From FPGA

- GTY High Speed Transceivers (up to 32.75Gbps) x 8

General Specification

- Power Supply : 5V (from Board-to-Board Connector2)
- Form Factor: 110mm x 75mm

[1] The Bank number and signal name (with ball name) in entire document is based on the VU13P device.
[2] Optionally One GTY transceiver link is connected with on-SOM PCIe Interface.

2.3 Virtex UltraScale+ FPGA

2.3.1 FPGA & Design Information

The Virtex UltraScale+ FPGA SoC provides best performance with up to 40% lower power than previous generation Virtex series due to enhanced system logic cell packaging. This also includes the highest signal processing bandwidth in a mid-range device, next generation transceivers. The family is ideal for DSP intensive processing required for next generation and packet processing in 100G networking.

Note: Please refer the latest Virtex UltraScale+ FPGA Datasheet & Technical Reference Manual for more details which may be revised from time to time.

		VU080	VU095	VU125	VU160	VU190	VU5P	VU7P	VU9P	VU11P	VU13P
Logic	System Logic Cells (K)	975	1,176	1,567	2,027	2,350	1,314	1,724	2,586	2,835	3,780
	CLB Flip-Flops	8,91,424	10,75,200	14,32,320	18,52,800	21,48,480	12,01,000	15,76,000	23,64,000	25,92,000	34,56,000
	CLB LUTs	4,45,712	5,37,600	7,16,160	9,26,400	10,74,240	601000	788000	11,82,000	12,96,000	17,28,000
Memory	Maximum Distributed RAM (Kb)	3,980	4,800	9,660	12,690	14,490	18,300	24,100	36,100	36,200	48,300
	Total Block RAM (Mb)	50	60.8	88.6	115.2	132.9	36	50.6	75.9	70.9	94.5
Clocking	CMT (1 MMCM, 2 PLLs)	16	16	20	28	30	NA	NA	NA	NA	NA
Integrated IP	DSP Slices	672	768	1,200	1,560	1,800	3,474	4,560	6,840	9,216	12,288
	PCIe Gen1/2/3	4	4	4	4	6	4	4	6	3	4
	100G Ethernet	4	4	6	9	9	4	6	9	9	12
I/O	Max. Single-Ended HP I/Os	650	650	650	650	650	702	702	702	572	702
	Max. Single-Ended HD or HR I/Os	52	52	52	52	52	NA	NA	NA	NA	NA

Figure 2: Virtex UltraScale+ FPGA Devices Comparison

The Virtex UltraScale+ FPGA's IO Banks are classified as high-performance (HP) banks. The HP Bank I/Os are optimized for highest performance operation organized in banks of 52pins.

In Virtex UltraScale+ FPGA, each IO bank supports four global clock (GC) input pin pairs. GC pins have direct access to the global clock buffers, PLLs of the same Bank. Also, Virtex UltraScale+ FPGA supports high speed GTY transceivers.

2.3.1.1 FPGA Power

The Virtex UltraScale+ FPGA SOM uses discrete power regulators along with DA9062 PMIC from Dialog Semiconductor for FPGA power management. In SOM, FPGA power domain supply voltage (VCC_INT, VCCINT_IO, VCCBRAM) is fixed to 0.85V or 0.9V based on the speed grade of the FPGA.

The Virtex UltraScale+ FPGA SOM supports Dialog semiconductor DA9062 PMIC for other powers to FPGA. The I2C2 module of LS1021A is used for FPGA PMIC interface with I2C address 0x48. The I/O voltage HP Banks which are connected to Board-to-Board Connectors are generated from PMIC LDO1, LDO2, LDO3 and LDO4 respectively.

PMIC's LDO1 is connected to I/O voltage of HP Bank64 and by default set to 1V, LDO2 is connected to I/O voltage of HP Bank65 and by default set to 1.8V, LDO3 is connected to HP Bank66 and by default set to 1V, LDO4 is connected to I/O voltage of HP Bank67 and by default set to 1V. IO voltage of HP 66 and 67 is configurable through software after LS1021A boot-up.

PMIC supports reset output and connected to Virtex UltraScale+ FPGA AL28 pin (IO_L24N_T3U_N11_DOUT_CSO_B_65) for power on reset. Also, PMIC supports IRQ output for events indication and connected to FPGA BC28 pin (IO_T1U_N12_SMBALERT_65).

Important Note: Every Power Off and On, The DA9062 PMIC work as initial OTP Setting.

2.3.1.2 FPGA Reset

The Virtex UltraScale+ FPGA SOM uses PMIC's Reset output (nRESET) for FPGA Power On Reset and connected to AL28 pin (IO_L24N_T3U_N11_DOUT_CSO_B_65) of FPGA.

2.3.1.3 FPGA Reference Clock

The Virtex UltraScale+ FPGA SOM supports on board clock synthesizer for reference clock to different blocks of Virtex UltraScale+ FPGA and LS1021A processor. The reference clock from Clock Synthesizer to FPGA is mentioned in the below table.

Sl. No	On-SOM Clock Synthesizer Frequency	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description	Stability
1	300MHz	IO_L13P_T2L_N0_GC_QBC_72	72	G14	1.8V, LVDS	LVDS reference clock for FPGA DDR4 SDRAM1. This is connected to FPGA Bank72 Global clock pins.	NA
		IO_L13N_T2L_N1_GC_QBC_72		F14			NA
2	300MHz	IO_L13P_T2L_N0_GC_QBC_71	71	J26	1.8V, LVDS	LVDS reference clock for FPGA DDR4 SDRAM2. This is connected to FPGA Bank71 Global clock pins.	NA
		IO_L13N_T2L_N1_GC_QBC_71		H26			NA
3	125MHz	IO_L19P_T3L_N0_DBC_AD9P_64	64	AN22	1.8V, LVDS	Reference clock for FPGA.	NA
		IO_L19N_T3L_N1_DBC_AD9N_64		AN21			NA
4	100MHz	MGTREFCLK0P_227	227	AH11	1.8V, LVDS	Bank227 PCIe Reference Clock0.	NA
		MGTREFCLK0N_227		AH10			NA
5	125MHz	IO_L24P_T3U_N10_EMCCLK_65	65	AL27	1.8V, LVCMOS	External Master Clock	NA

2.3.1.4 FPGA Configuration & Status

In Virtex UltraScale+ SOM, by default QSPI Flash is set as configuration device through mode pins. Memory configuration files are generated from the BIT file in Vivado is programmed to QSPI through JTAG.

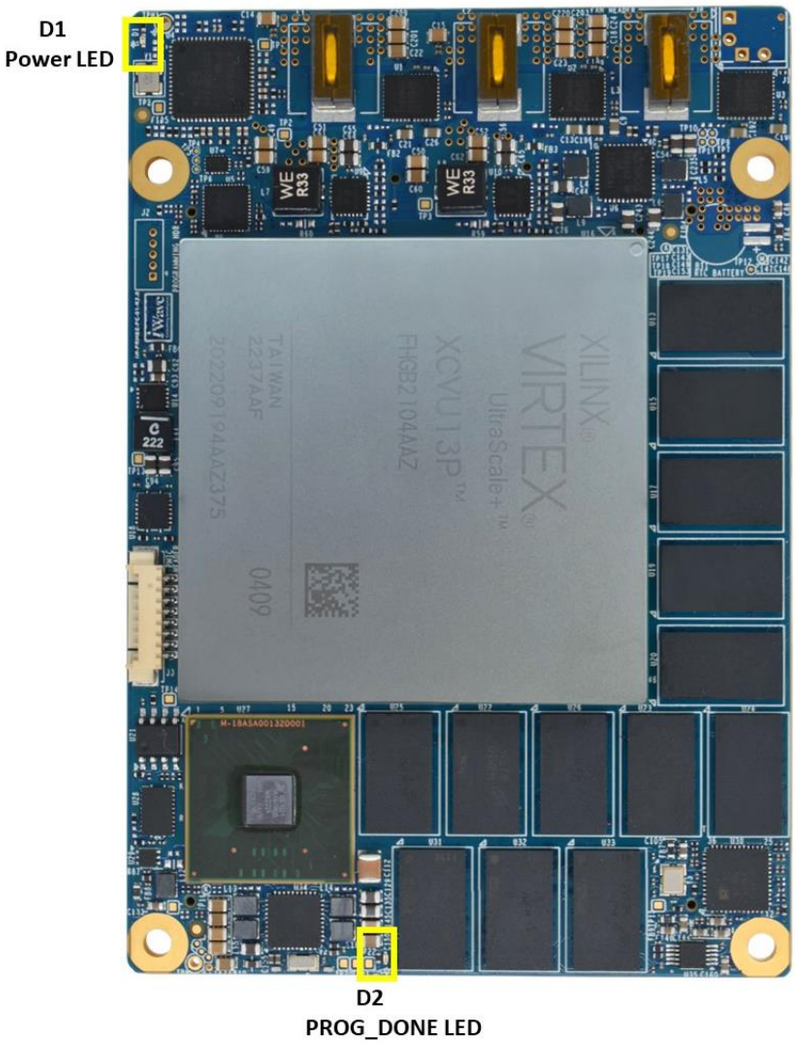


Figure 3: Indication LEDs

The Virtex UltraScale+ FPGA SOM supports two LEDs for the indicate the status of SOM Power and Configuration. LED D1 is for Power LED and it indicates the power which is the final in the power sequence. LED D2 is for PROG_DONE pin of FPGA and it indicates successful completion of FPGA configuration.

The Virtex UltraScale+ FPGA SOM supports three dedicated input and output configuration pins. By default, Weak pre - reconfiguration I/O pull-up resistors disabled for PUDC_B pin, Standard FPGA power-on delay time for POR_OVERRIDE pin is connected to Ground through 4.7K.

2.3.1.5 FPGA Mode Configuration

The Virtex UltraScale+ SOM provides mode pins for selection of configuration device. The SOM supports 4-bit QSPI Flash and JTAG for the configuration of FPGA. By default, mode bit is configured to “001” for QSPI Flash as configuration device.

Below table provides the Mode bit status for available configuration devices of SOM.

MODE2	MODE1	MODE0	CONFIGURATION MODE
0	0	1	QSPI
1	0	1	JTAG

2.3.1.6 FPGA System Monitor/ADC

The Virtex UltraScale+ FPGA contain one System Monitor block (SYSMONE4). It is used to enhance the overall safety, security and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

The SYSMON uses 10-bit 200kSPS ADC to digitize the sensor/ADC inputs. It monitors the die temperature of the FPGA and several internal supply nodes. The SYSMON can also monitor up to 17 external analog channels which includes 16 auxiliary analog inputs and one VP_VN dedicated input. The external auxiliary inputs can be routed through any IO Bank. The ADC voltage reference is selectable between an internal reference and the external pins VREFP and VREFN. In Virtex UltraScale+ FPGA SOM, 1.25V external voltage reference is supported.

2.3.2 FPGA Memory

2.3.2.1 DDR4 SDRAM1 with ECC

The Virtex UltraScale+ FPGA SOM supports 64bit, 4GB DDR4 RAM memory for FPGA with 8-bit ECC. Four 16 bit, 1GB DDR4 SDRAM ICs is used to support RAM memory of 4GB. These DDR4 devices operates at 2666Mbps data rate. In Virtex UltraScale+ FPGA SOM, Bank72, 73 & 74 is used for FPGA DDR4 SDRAM1 interface. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The Virtex UltraScale+ FPGA SOM supports 300MHz LVDS DDR4 reference clock from on board clock synthesizer and connected to Bank72 G14 & F14 dedicated clock input pins through AC Coupling capacitors.

Note: Virtex UltraScale+ FPGA SOM with -2 & -3 speed grade FPGA can support up to 2666Mbps data rate for FPGA DDR4.

2.3.2.2 DDR4 SDRAM2 with ECC

The Virtex UltraScale+ FPGA SOM supports 64bit, 4GB DDR4 RAM memory for FPGA with 8-bit ECC. Four 16 bit, 1GB DDR4 SDRAM ICs is used to support RAM memory of 4GB. These DDR4 devices operates at 2666Mbps data rate. In Virtex UltraScale+ FPGA SOM, Bank69, 70 & 71 is used for FPGA SDRAM2 DDR4 interface. Also, Both SDRAM1 and SDRAM2 supports two 4bit ECC for RAM memory. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The Virtex UltraScale+ FPGA SOM supports 300MHz LVDS DDR4 reference clock from on board clock synthesizer and connected to Bank71 J26 & H26 dedicated clock input pins through AC Coupling capacitors.

Note: Virtex UltraScale+ FPGA SOM with -2 & -3 speed grade FPGA can support up to 2666Mbps data rate for FPGA DDR4.

2.4 Layerscape Processor

2.4.1 Processor & Design Information

The Virtex UltraScale+ FPGA SOM is based on Xilinx Virtex UltraScale+ FPGA integrated with LS1021A Layerscape Processor. Featuring a pair of extremely power-efficient 32-bit Arm Cortex-A7 cores with ECC protected L1 and L2 cache memories for high reliability, running up to 1.2 GHz, and providing pre-silicon CoreMark performance of over 5,000, the LS102xA family delivers greater performance than any previous sub-4W communication processor. The Block Diagram of LS1021A from NXP website is shown below for reference.

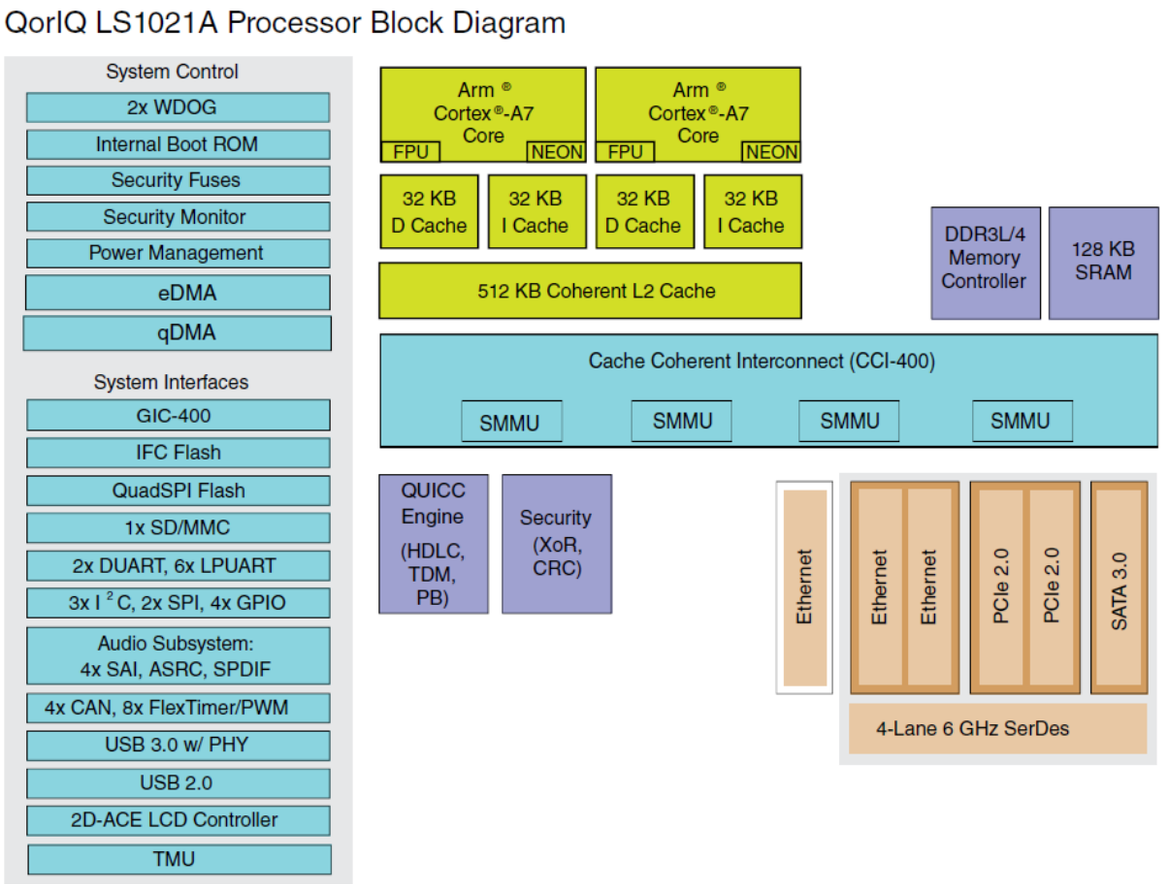


Figure 4: LS1021A Internal Block Diagram

2.4.1.1 LS1021A Booting and Configuration

The Virtex UltraScale+ SOM integrates FPGA SoC with L1021A Layerscape processor. The binary (RCW and u-boot) is programmed into the NOR Flash through JTAG using CodeWarrior TAP module. On POR, Pre-Boot Loader (PBL) will fetch RCW configuration and PBL commands from NOR flash (chosen by cfg_rcw_src selection pins). Then executes u-boot from NOR flash.

2.4.1.2 LS1021A PMIC

The Virtex UltraScale+ FPGA SOM supports Dialog semiconductor DA9062 PMIC and one regulator for LS1021A Processor. The I2C2 module of LS1021A is used for PMIC interface through LS1021A pins with I2C address 0x58.

PMIC supports reset output and connected to LS1021A (LS_PMIC_POR) for power on reset. Also, PMIC supports IRQ output for events indication and connected to LS1021A's GPIO (GPIO3_23).

The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from Board-to-Board Connector2 pin68 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

2.4.1.3 LS1021A Reference Clock

The Virtex UltraScale+ FPGA SOM supports on board clock synthesizer for reference clock to LS1021A Processor. These reference clock from clock synthesizer to LS1021A is mentioned in the below table.

Sl. No	On-SOM Clock Synthesizer Frequency	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description	Stability
1	100MHz	DIFF_SYSCLK	F4	1.8V, LVDS	Differential system clock positive/negative.	NA
		DIFF_SYSCLK_B	G4			
2	100MHz	SD1_REF_CLK1_P	AC8	1.8V, LVDS	SerDes PLL 1 Reference Clock	NA
		SD1_REF_CLK1_N	AB8			NA
3	100MHz	SD1_REF_CLK2_P	AC16	1.8V, LVDS	SerDes PLL 2 Reference Clock	NA
		SD1_REF_CLK2_N	AB16			NA
4	100MHz	DDRCLK	H18	1.8V, LVCMOS	NC. Optionally connected to DDR controller complex clock.	NA
5	100MHz	SYSCLK	F5	1.8V, LVCMOS	System Clock	NA

2.4.2 Processor Memory

2.4.2.1 DDR4 SDRAM with ECC for LS1021A

The Virtex UltraScale+ FPGA SOM supports 32bit, 2GB DDR4 RAM memory for LS1021A. Two 16 bit, 1GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 2GB. Also, Virtex UltraScale+ FPGA SOM supports one 4bit ECC for RAM memory. These DDR4 devices operates at 1600MTps data rate. DDR4 memory is connected to the DDR4 SDRAM controller of the LS1021A Processor.

2.4.2.2 NOR Flash

The Virtex UltraScale+ FPGA SOM supports 256MB NOR Flash memory as boot-device of LS1021A Processor. The NOR Flash is used for programming RCW and U-boot for LS1021A booting purpose. This NOR Flash memory is connected to the Integrated Flash Controller of the LS1021A Processor and operates at 3.3V Voltage level.

2.4.2.3 MRAM

The Virtex UltraScale+ FPGA SOM supports 4MB MRAM memory for storage purpose for Layerscape LS1021A Processor. This MRAM memory is connected to the Integrated Flash Controller of the LS1021A Processor and operates at 3.3V Voltage level.

2.4.2.4 SRAM

The Virtex UltraScale+ FPGA SOM supports 512KB SPI Serial SRAM memory for storage purpose of LS1021A Processor. This SRAM memory is connected to the SPI2 lane of LS1021A and operates at 1.8V Voltage level.

2.5 FPGA to CPU Interfaces

2.5.1 PCIex1 Gen2

The Virtex UltraScale+ SOM supports Generation2 PCIex1 interface between LS1021A Processor and FPGA. Channel3 of FPGA GTY Transceiver Bank227 is connected to LS1021A SERDES SD1 for PCIe interface.

Refer the below table for more details.

Signal Name	LS1021A Pin Name	LS1021A Pin No	FPGA Pin Name	FPGA Pin No.	Signal Type/ Termination*	Description
LS_SD1_RX0_P	SD1_RX0_P	AC10	MGTYTXP3_227	AF7	I, DIFF	SerDes Receive Data0 positive
LS_SD1_RX0_N	SD1_RX0_N	AB10	MGTYTXN3_227	AF6	I, DIFF	SerDes Receive Data0 negative
LS_SD1_TX0_P	SD1_TX0_P	W10	MGTYRXP3_227	AF2	O, DIFF	SerDes Transmit Data0 positive
LS_SD1_TX0_N	SD1_TX0_N	Y10	MGTYRXN3_227	AF1	O, DIFF	SerDes Transmit Data0 negative
LS_PERST0_PL_AR26(EC2_RX_CLK)	EC2_RX_CLK/GPIO3_26/USB2_DIR/FTM2_QD_PHA	R1	IO_T3U_N12_PERSTN0_65	AR26	O, 1.8V	PCIe Reset input from LS1021A to FPGA

** Signal directions mentioned in table are based on LS1021A processor.*

2.5.2 RGMII

The Virtex UltraScale+ SOM supports RGMII interface between LS1021A Processor and FPGA through Ethernet Controller3 interface of LS1021A and HP Bank65 of FPGA.

Refer the below table for more details.

Signal Name	LS1021A Pin Name	LS1021A Pin No	FPGA Pin Name	FPGA Pin No.	Signal Type/ Termination*	Description
LS_EC3_TXCLK_PL_AW26_L13N_65	EC3_GTX_CLK/GPIO4_01/EC2_TX_ER/FTM3_CH0/EC3_TX_CLK	V5	IO_L13N_T2L_N1_GC_QBC_A07_D23_65	AW26	O, 1.8V	Transmit Clock Out
LS_EC3_TXD0_PL_BC26_L6P_65	EC3_TXD0/GPIO3_31/TSEC_1588_PULSE_OUT2/FTM3_CH4	W4	IO_L6P_T0U_N10_AD6P_A20_65	BC26	O, 1.8V	Transmit Data
LS_EC3_TXD1_PL_BF25_L5N_65	EC3_TXD1/GPIO3_30/TSEC_1588_CLK_OUT/FTM3_CH5	W3	IO_L5N_T0U_N9_AD14N_A23_65	BF25	O, 1.8V	Transmit Data

Signal Name	LS1021A Pin Name	LS1021A Pin No	FPGA Pin Name	FPGA Pin No.	Signal Type/ Termination*	Description
LS_EC3_TXD2_PL_BE25_L5P_65	EC3_TXD2/GPIO3_29/TSEC_1588_ALARM_OUT1/FTM3_CH6	V4	IO_L5P_T0U_N8_AD14P_A22_65	BE25	O, 1.8V	Transmit Data
LS_EC3_TXD3_PL_BE26_L4N_65	EC3_TXD3/GPIO3_28/TSEC_1588_ALARM_OUT2/FTM3_CH7	V3	IO_L4N_T0U_N7_DBC_AD7N_A25_65	BE26	O, 1.8V	Transmit Data
LS_EC3_TXEN_PL_BD26_L4P_65	EC3_TX_EN/GPIO4_00/EC1_TX_ER/FTM3_CH1	Y3	IO_L4P_T0U_N6_DBC_AD7P_A24_65	BD26	O, 1.8V	Transmit Enable
LS_EC3_RXCLK_PL_BE28_L3N_65	EC3_RX_CLK/GPIO4_07/TSEC_1588_CLK_IN/FTM3_QD_PHA	V2	IO_L3N_T0L_N5_AD15N_A27_65	BE28	I, 1.8V	Receive Clock
LS_EC3_RXD0_PL_BD28_L3P_65	EC3_RXD0/GPIO4_06/TSEC_1588_TRIG_IN2/EC2_CRS/FTM3_CH2	AA1	IO_L3P_T0L_N4_AD15P_A26_65	BD28	I, 1.8V	Receive Data
LS_EC3_RXD1_PL_BF27_L2N_65	EC3_RXD1/GPIO4_05/TSEC_1588_PULSE_OUT1/FTM3_CH3	Y2	IO_L2N_T0L_N3_FWE_FCS2_B_65	BF27	I, 1.8V	Receive Data
LS_EC3_RXD2_PL_BE27_L2P_65	EC3_RXD2/GPIO4_04/EC1_COL/FTM3_EXTCLK	Y1	IO_L2P_T0L_N2_FOE_B_65	BE27	I, 1.8V	Receive Data
LS_EC3_RXD3_PL_BF29_L1N_65	EC3_RXD3/GPIO4_03/EC1_CRS/FTM3_FAULT	W1	IO_L1N_T0L_N1_DBC_RS1_65	BF29	I, 1.8V	Receive Data
LS_EC3_RXDDV_PL_BF28_L1P_65	EC3_RX_DV/GPIO4_08/TSEC_1588_TRIG_IN1/FTM3_QD_PHB	AA2	IO_L1P_T0L_N0_DBC_RS0_65	BF28	I, 1.8V	Receive Data Valid
LS_EC3_GTXCLK125_PL_AM27_L23P_65	EC3_GTX_CLK125/GPIO4_02/EC2_COL/USB2_DRVVBUS/EC3_RX_ER	Y4	IO_L23P_T3U_N8_I2C_SCLK_65	AM27	I, 1.8V	RGMII TX Reference Clock

** Signal directions mentioned in table are based on LS1021A processor.*

2.5.3 UART

The Virtex UltraScale+ SOM supports UART interface between LS1021A Processor and FPGA through LPUART6 of LS1021A Processor and HP Bank65 of FPGA. Refer the below table for more details.

Signal Name	LS1021A Pin Name	LS1021A Pin No	FPGA Pin Name	FPGA Pin No.	Signal Type/ Termination*	Description
LS_LPUART6_SOUT_PL_AY25_L10N_65	SDHC_DAT3/GPIO2_08/LPUART3_RTS_B/LPUART6_SOUT	G1	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	AY25	O, 1.8V	Transmit Data
LS_LPUART6_SIN_PL_AW25_L10P_65	SDHC_CLK/GPIO2_09/LPUART3_CTS_B/LPUART6_SIN	D1	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	AW25	I, 1.8V	Receive Data

**Signal type is mentioned with respect to LS1021A processor.*

2.5.4 Interrupt Request pins

The Virtex UltraScale+ FPGA SOM supports 5 Interrupt Request signals from LS1021A to FPGA, which is connected from control signals of LS1021A to HP Bank 65 of FPGA.

Function Name	LS1021A Pin Name	LS1021A Pin No	FPGA Pin Name	FPGA Pin No.	Signal Type/ Termination	Description
LS_IRQ0_PL_AU25_CSI_ADV_65	IRQ0	G6	IO_T2U_N12_CSI_ADV_B_65	AU25	I, 1.8V	External Interrupt0 input from FPGA
LS_IRQ1_PL_BB27_L8N_65	IRQ1	G8	IO_L8N_T1L_N3_AD5N_A17_65	BB27	I, 1.8V	External Interrupt1 input from FPGA
LS_IRQ2_PL_BB26_L8P_65	IRQ2	W7	IO_L8P_T1L_N2_AD5P_A16_65	BB26	I, 1.8V	External Interrupt2 input from FPGA
LS_IRQ3_PL_BA28_L9N_65	IRQ3/GPIO1_23	R5	IO_L9N_T1L_N5_AD12N_A15_D31_65	BA28	I, 1.8V	External Interrupt3 input from FPGA
LS_IRQ4_PL_BA27_L9P_65	IRQ4/GPIO1_24/SDHC_VS	L2	IO_L9P_T1L_N4_AD12P_A14_D30_65	BA27	I, 1.8V	External Interrupt4 input from FPGA

**Signal type is mentioned with respect to LS1021A processor.*

2.6 Other On SOM Features

2.6.1 TPM Module

The Virtex UltraScale+ FPGA SOM supports Trusted Platform Module (TPM) 2.0 Module through LS1021A Processor. The TPM technology is designed to provide hardware-based, security-related functions. A TPM chip is a secure crypto-processor that is designed to carry out cryptographic operations. This TPM Module is connected to the SPI2 lane of LS1021A and operates at 3.3V Voltage level.

2.6.2 Temperature Sensor

The Virtex UltraScale+ FPGA SOM supports Temperature sensor to measure the junction temperature of both LS1021A Processor and FPGA. The temperature sensor supports one local channel and two remote channels. The local channel measures IC self-die temperature. Remote channel1 is connected to LS1021A thermal diode and remote channel2 is connected to FPGA thermal diode.

2.7 Board to Board Connectors

Virtex UltraScale+ FPGA transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

Virtex UltraScale+ FPGA Speed Grade	GTY Transceiver line rate (min)	GTY Transceiver line rate (max)	GTH Transceiver line rate (min)	GTH Transceiver line rate (max)
-1 Speed Grade	0.5 Gbps	25.785 Gbps	0.5 Gbps	12.5 Gbps
-2 Speed Grade	0.5 Gbps	28.21 Gbps	0.5 Gbps	16.375 Gbps
-3 Speed Grade	0.5 Gbps	32.75 Gbps	0.5 Gbps	16.375 Gbps

Note: For Backplane application, the transceiver maximum line rate may come down.
GTY transceivers in Virtex UltraScale devices support data rates up to 30.5Gb/s.

Transceiver Quad Migration in Board-to-Board connector for supported FPGA is given in the table below

	VU080	VU095	VU125	VU160	VU190	VU5P	VU7P	VU9P	VU11P	VU13P
Board To Board -1	GTH-224	GTH-224	GTH-224	GTH-224	GTH-224	GTY-224	GTY-224	GTY-224	GTY-224	GTY-224
	GTH-225	GTH-225	GTH-225	GTH-225	GTH-225	GTY-225	GTY-225	GTY-225	GTY-225	GTY-225
	GTY-124	GTY-124	GTY-125	GTY-125	GTY-125	GTY-125	GTY-125	GTY-120	GTY-124	GTY-124
Board To Board -2	GTY-125	GTY-125	GTY-126	GTY-126	GTY-126	GTY-126	GTY-126	GTY-121	GTY-125	GTY-125
Board To Board -3	GTH-230	GTH-230	GTH-230	GTH-230	GTH-230	GTY-230	GTY-230	GTY-230	GTY-230	GTY-230
	GTH-229	GTH-229	GTH-229	GTH-229	GTH-229	GTY-229	GTY-229	GTY-229	GTY-229	GTY-229
	GTY-129	GTY-129	GTY-130	GTY-130	GTY-130	GTY-130	GTY-130	GTY-125	GTY-129	GTY-129
	GTH-231	GTH-231	GTH-231	GTH-231	GTH-231	GTY-231	GTY-231	GTY-231	GTY-231	GTY-231
	NA	NA	GTH-232	GTH-232	GTH-232	GTY-232	GTY-232	GTY-232	GTY-232	GTY-232
	GTH-227	GTH-227	GTH-227	GTH-227	GTH-227	GTY-227	GTY-227	GTY-227	GTY-227	GTY-227
Board To Board -4	GTH-226	GTH-226	GTH-226	GTH-226	GTH-226	GTY-226	GTY-226	GTY-226	GTY-226	GTY-226
	GTY-126	GTY-126	GTY-127	GTY-127	GTY-127	GTY-127	GTY-127	GTY-122	GTY-126	GTY-126

Note: GTY Transceiver speed is limited to 16Gbps for Transceivers in Board-to-Board connector1 & 2 because of connector speed limit.

I/O Bank Migration in Board-to-Board connector for supported FPGA is given in the table below

	VU080	VU095	VU125	VU160	VU190	VU5P	VU7P	VU9P	VU11P	VU13P
Board To Board -1	HR-84/94	HR-84/94	HR-84/94	HR-84/94	HR-84/94	HP-64	HP-64	HP-64	HP-64	HP-64
	HP-68	HP-68	HP-68	HP-68	HP-68	HP-68	HP-68	HP-68	NA	HP-68
	HP-65	HP-65	HP-65	HP-65	HP-65	HP-65	HP-65	HP-65	HP-65	HP-65
Board To Board -2	HP-66	HP-66	HP-66	HP-66	HP-66	HP-66	HP-66	HP-66	HP-66	HP-66
	HP-67	HP-67	HP-67	HP-67	HP-67	HP-67	HP-67	HP-67	HP-67	HP-67

Important Note: The Bank number and signal name (with ball name) in pinout mentioned in this document based on the VU13P device.

2.8 Board to Board Connector1

The Virtex UltraScale+ FPGA SOM supports two 240 pin high speed ruggedized terminal strip connectors, one 240pin High-Speed High-Density connector and one 80pin High-Speed High-Density connector for interfaces expansion. All the effort is made in Virtex UltraScale+ FPGA SOM design to provide the maximum interfaces of Virtex UltraScale+ FPGA to the carrier board by adding these two Board to Board Connectors.

The Virtex UltraScale+ FPGA SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J7) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240
Connector Part Number - QTH-120-01-L-D-A from Samtec
Mating Connector - QSH-120-01-L-D-A from Samtec
Staking Height - 5mm

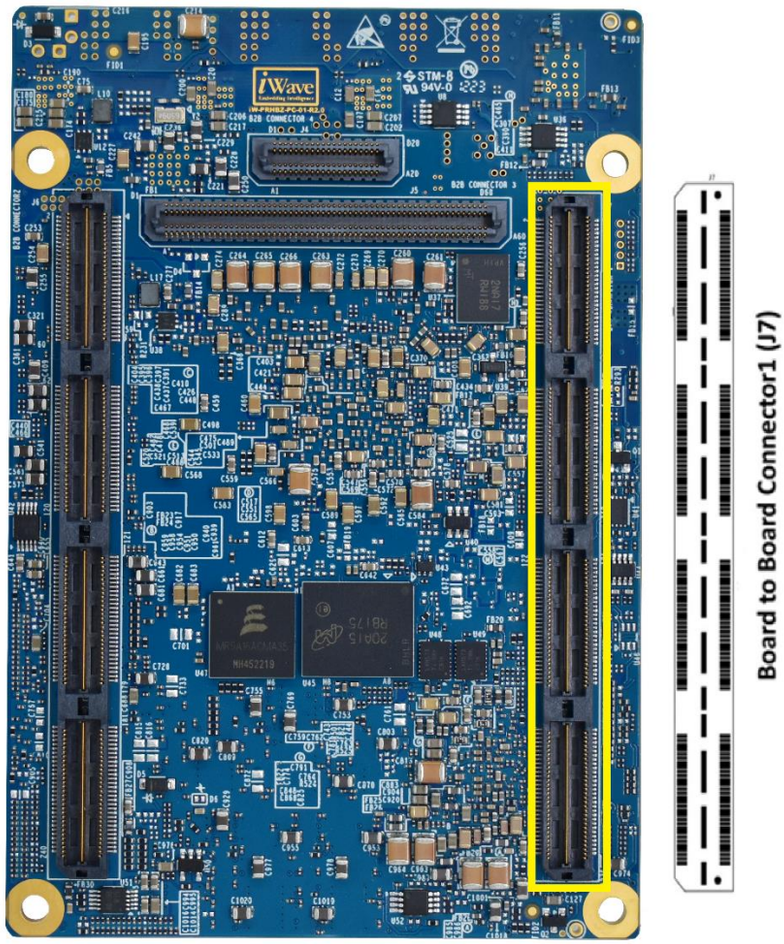


Figure 5: Board to Board Connector1

Table 3: Board to Board Connector1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GND	1	2	GND
GTYTXP0_224	3	4	GTREFCLK0P_224
GTYTXN0_224	5	6	GTREFCLK0N_224
GND	7	8	GND
GTYTXP1_224	9	10	NC
GTYTXN1_224	11	12	PL_AL22_LVD64_L23P
GND	13	14	PL_AM22_LVDS64_L23N
GTYRXN1_224	15	16	PL_AU22_LVDS64_L15P
GTYRXP1_224	17	18	GPIO3_22(EC2_RXD3)
GND	19	20	GND
GTYRXN0_224	21	22	PL_AP23_LVDS64_L20N
GTYRXP0_224	23	24	PL_AN23_LVDS64_L20P
GND	25	26	GND
PL_AV24_LVDS64_L14P	27	28	GPIO3_18(EC2_TXD0)
PL_AW24_LVDS64_L14N	29	30	GPIO3_17(EC2_TXD1)
PL_AL24_LVDS64_L22P	31	32	GPIO3_24(EC2_RXD1)
PL_AM24_LVDS64_L22N	33	34	GPIO4_09(TDMA_RXD)
GND	35	36	GND
GTYTXP2_224	37	38	GPIO3_19(EC2_TXEN)
GTYTXN2_224	39	40	PL_AP24_LVDS64_L21N
GND	41	42	PL_BF10_LVDS68_L3P
GTYTXP3_224	43	44	PL_AN24_LVDS64_L21P
GTYTXN3_224	45	46	PL_AR22_LVDS64_L16P
GND	47	48	PL_AT22_LVDS64_L16N
GTYRXN3_224	49	50	PL_AV22_LVDS64_L15N
GTYRXP3_224	51	52	PL_BF9_LVDS68_L3N
GND	53	54	GND
GTYRXN2_224	55	56	PL_BB10_LVDS68_L8N
GTYRXP2_224	57	58	PL_BB11_LVDS68_L8P
GND	59	60	GND
GND	61	62	GND
LS_SD1_TX2_P	63	64	GTREFCLK1P_224
LS_SD1_TX2_N	65	66	GTREFCLK1N_224
GND	67	68	GND
NC	69	70	PL_AL21_LVDS64_L24P
NC	71	72	PL_AM21_LVDS64_L24N
GND	73	74	PL_BA7_LVDS68_L10P
NC	75	76	PL_BB7_LVDS68_L10N
NC	77	78	NC
GND	79	80	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
LS_SD1_RX2_N	81	82	PL_BC11_LVDS68_L7N
LS_SD1_RX2_P	83	84	PL_BC12_LVDS68_L7P
GND	85	86	GND
PL_AT24_LVDS64_L18P	87	88	PL_AW23_LVDS64_L13N
PL_AU24_LVDS64_L18N	89	90	PL_AV23_LVDS64_L13P
PL_AR23_LVDS64_L17P	91	92	PL_BC8_LVDS68_L9P
PL_AT23_LVDS64_L17N	93	94	PL_BC7_LVDS68_L9N
GND	95	96	GND
GTYTXP0_225	97	98	GTREFCLK0P_225
GTYTXN0_225	99	100	GTREFCLK0N_225
GND	101	102	GND
GTYTXP1_225	103	104	PL_BF22_LVDS64_L4N
GTYTXN1_225	105	106	PL_BE20_LVDS64_L6N
GND	107	108	PL_BD20_LVDS64_L6P
GTYRXN1_225	109	110	PL_BE21_LVDS64_L5N
GTYRXP1_225	111	112	PL_BD21_LVDS64_L5P
GND	113	114	GND
GTYRXN0_225	115	116	PL_BF12_LVDS68_L5N
GTYRXP0_225	117	118	PL_BE12_LVDS68_L5P
GND	119	120	GND
GND	121	122	GND
GTYTXP2_225	123	124	PL_BD9_LVDS68_L6P
GTYTXN2_225	125	126	PL_BD8_LVDS68_L6N
GND	127	128	PL_BE22_LVDS64_L4P
GTYTXP3_225	129	130	PL_BF24_LVDS64_L1P
GTYTXN3_225	131	132	PL_BF23_LVDS64_L1N
GND	133	134	PL_BD24_LVDS64_L3N
GTYRXN3_225	135	136	PL_BA20_LVDS64_L7P
GTYRXP3_225	137	138	PL_BB20_LVDS64_L7N
GND	139	140	GND
GTYRXN2_225	141	142	PL_BA22_LVDS64_L11N_GC
GTYRXP2_225	143	144	PL_AY22_LVDS64_L11P_GC
GND	145	146	GND
PL_BE7_LVDS68_L1P	147	148	PL_BB24_LVDS64_L10N
PL_BF7_LVDS68_L1N	149	150	PL_BA24_LVDS64_L10P
PL_BE23_LVDS64_L2N	151	152	PL_BC22_LVDS64_L9N
PL_BD23_LVDS64_L2P	153	154	PL_BB22_LVDS64_L9P
GND	155	156	GND
LS_SD1_TX3_P	157	158	GTREFCLK1P_225
LS_SD1_TX3_N	159	160	GTREFCLK1N_225
GND	161	162	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
NC	163	164	NC
NC	165	166	NC
GND	167	168	SYSMON_VN
CLK_GEN_IN_N	169	170	PL_AN27_LVDS65_L23N_PERSTN1_SDA
CLK_GEN_IN_P	171	172	PL_BC24_LVDS64_L3P
GND	173	174	GND
LS_SD1_RX3_N	175	176	PL_BE10_LVDS68_L4N
LS_SD1_RX3_P	177	178	PL_BE11_LVDS68_L4P
GND	179	180	GND
GND	181	182	GND
GTYTXP0_124	183	184	GTREFCLK0P_124
GTYTXN0_124	185	186	GTREFCLK0N_124
GND	187	188	GND
GTYTXP1_124	189	190	PL_AV26_LVDS65_L13P_A06_D22_GC
GTYTXN1_124	191	192	PL_AY27_LVDS65_L11N_A11_D27_GC
GND	193	194	PL_AY26_LVDS65_L11P_A10_D26_GC
GTYRXN1_124	195	196	PL_AY28_LVDS65_L12N_A09_D25_GC
GTYRXP1_124	197	198	PL_AW28_LVDS65_L12P_A08_D24_GC
GND	199	200	GND
GTYRXN0_124	201	202	PL_BF8_LVDS68_L2N
GTYRXP0_124	203	204	PL_BE8_LVDS68_L2P
GND	205	206	GND
PL_BA8_LVDS68_L12N_GC	207	208	NC
PL_BA9_LVDS68_L12P_GC	209	210	PL_BC27_LVDS65_L6N
PL_BB9_LVDS68_L11P_GC	211	212	PL_AV27_LVDS65_L14P_A04_D20_GC
PL_BC9_LVDS68_L11N_GC	213	214	PL_AV28_LVDS65_L14N_A05_D21_GC
GND	215	216	GND
GTYTXP2_124	217	218	GTREFCLK1P_124
GTYTXN2_124	219	220	GTREFCLK1N_124
GND	221	222	GND
GTYTXP3_124	223	224	PL_AP26_LVDS65_L19N_DBC_D11
GTYTXN3_124	225	226	PL_AP25_LVDS65_L19P_DBC_D10
GND	227	228	PL_AT28_LVDS65_L18N_D13
GTYRXN3_124	229	230	PL_AR28_LVDS65_L18P_D12
GTYRXP3_124	231	232	SOMPWR_EN
GND	233	234	GND
GTYRXN2_124	235	236	PL_BA23_LVDS64_L12N_GC
GTYRXP2_124	237	238	PL_AY23_LVDS64_L12P_GC
GND	239	240	GND

2.8.1 LS1021A Interfaces

The interfaces which are supported in Board-to-Board Connector1 from LS1021A Processor is explained in the following section

2.8.1.1 SerDes Interface

The Virtex UltraScale+ FPGA SOM supports 2 highspeed SerDes lane and its reference clock through LS1021A Layerscape Processor in board-to-board connector1

For more details on SerDes Interface pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
63	LS_SD1_TX2_P	SD1_TX2_P	W13	O, DIFF	SerDes Transmit Data Positive
65	LS_SD1_TX2_N	SD1_TX2_N	Y13	O, DIFF	SerDes Transmit Data Negative
81	LS_SD1_RX2_N	SD1_RX2_N	AB13	I, DIFF	SerDes Receive Data Negative
83	LS_SD1_RX2_P	SD1_RX2_P	AC13	I, DIFF	SerDes Receive Data Positive
177	LS_SD1_RX3_P	SD1_RX3_P	AC14	I, DIFF	SerDes Receive Data3 Positive
175	LS_SD1_RX3_N	SD1_RX3_N	AB14	I, DIFF	SerDes Receive Data3 Negative
157	LS_SD1_TX3_P	SD1_TX3_P	W14	O, DIFF	SerDes Transmit Data3 Positive
159	LS_SD1_TX3_N	SD1_TX3_N	Y14	O, DIFF	SerDes Transmit Data3 Negative

2.8.1.2 GPIOs From LS1021A

The Virtex UltraScale+ FPGA SOM supports 6 GPIOs from LS1021A Layerscape Processor in board-to-board connector1

For more details on GPIOs pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
18	GPIO3_22(EC2_RXD3)	EC2_RXD3/GPIO3_22/CAN4_RX/USB2_D3/FTM2_CH4	R2	O, 1.8V	General Purpose Output from LS1021A Processor
28	GPIO3_18(EC2_TXD0)	EC2_TXD0/GPIO3_18/USB2_D4/FTM2_CH2	T3	I, 1.8V	General Purpose Input from LS1021A Processor
30	GPIO3_17(EC2_TXD1)	EC2_TXD1/GPIO3_17/USB2_D5/FTM2_CH3	T4	I, 1.8V	General Purpose Input from LS1021A Processor
32	GPIO3_24(EC2_RXD1)	EC2_RXD1/GPIO3_24/USB2_D1/FTM2_CH1	U1	I, 1.8V	General Purpose Input from LS1021A Processor
34	GPIO4_09(TDMA_RXD)	TDMA_RXD/GPIO4_09/UC1_RXD7/SAI3_RX_DATA/FTM4_CH7/2D-ACE_D00	H3	I, 1.8V	General Purpose Input from LS1021A Processor
38	GPIO3_19(EC2_TXEN)	EC2_TX_EN/GPIO3_19/USB2_STP/FTM2_FAULT	T5	O, 1.8V	General Purpose Input from LS1021A Processor

2.8.2 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Virtex UltraScale+ FPGA is explained in the following section.

2.8.2.1 GTY High Speed Transceivers

The Virtex UltraScale+ FPGA supports 12 GTY transceivers through three transceiver Quad with line rate from 500Mbps to 32.75Gbps based on the speed grade of the FPGA. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

In Virtex UltraScale+ FPGA SOM, on board reference clock to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required peripheral standards on GTY transceivers. Also, on board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommend.

For more details on GTY transceiver pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank224 Transceiver Quad Pins						
3	GTYTXP0_224	MGTYTXP0_224	224	BF5	O, DIFF	GTY Bank224 channel0 High speed differential transmitter positive.
5	GTYTXN0_224	MGTYTXN0_224	224	BF4	O, DIFF	GTY Bank224 channel0 High speed differential transmitter negative.
9	GTYTXP1_224	MGTYTXP1_224	224	BD5	O, DIFF	GTY Bank224 channel1 High speed differential transmitter positive.
11	GTYTXN1_224	MGTYTXN1_224	224	BD4	O, DIFF	GTY Bank224 channel1 High speed differential transmitter negative.
15	GTYRXN1_224	MGTYRXN1_224	224	BA1	I, DIFF	GTY Bank224 channel1 High speed differential receiver negative.
17	GTYRXP1_224	MGTYRXP1_224	224	BA2	I, DIFF	GTY Bank224 channel1 High speed differential receiver positive.
21	GTYRXN0_224	MGTYRXN0_224	224	BC1	I, DIFF	GTY Bank224 channel0 High speed differential receiver negative.
23	GTYRXP0_224	MGTYRXP0_224	224	BC2	I, DIFF	GTY Bank224 channel0 High speed differential receiver positive.
37	GTYTXP2_224	MGTYTXP2_224	224	BB5	O, DIFF	GTY Bank224 channel2 High speed differential transmitter positive.
39	GTYTXN2_224	MGTYTXN2_224	224	BB4	O, DIFF	GTY Bank224 channel2 High speed differential transmitter negative.
43	GTYTXP3_224	MGTYTXP3_224	224	AV7	O, DIFF	GTY Bank224 channel3 High speed differential transmitter positive.

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
45	GTYTXN3_224	MGTYTXN3_224	224	AV6	O, DIFF	GTY Bank224 channel3 High speed differential transmitter negative.
49	GTYRXN3_224	MGTYRXN3_224	224	AV1	I, DIFF	GTY Bank224 channel3 High speed differential receiver negative.
51	GTYRXP3_224	MGTYRXP3_224	224	AV2	I, DIFF	GTY Bank224 channel3 High speed differential receiver positive.
55	GTYRXN2_224	MGTYRXN2_224	224	AW3	I, DIFF	GTY Bank224 channel2 High speed differential receiver negative.
57	GTYRXP2_224	MGTYRXP2_224	224	AW4	I, DIFF	GTY Bank224 channel2 High speed differential receiver positive.
4	GTREFCLK0P_224	MGTREFCLK0P_224	224	AW9	I, DIFF	GTY Bank224 differential reference clock0 positive.
6	GTREFCLK0N_224	MGTREFCLK0N_224	224	AW8	I, DIFF	GTY Bank224 differential reference clock0 negative.
64	GTREFCLK1P_224	MGTREFCLK1P_224	224	AV11	I, DIFF	GTY Bank224 differential reference clock1 positive.
66	GTREFCLK1N_224	MGTREFCLK1N_224	224	AV10	I, DIFF	GTY Bank224 differential reference clock1 negative.
Bank225 Transceiver Quad Pins						
97	GTYTXP0_225	MGTYTXP0_225	225	AU9	O, DIFF	GTY Bank225 channel0 High speed differential transmitter positive.
99	GTYTXN0_225	MGTYTXN0_225	225	AU8	O, DIFF	GTY Bank225 channel0 High speed differential transmitter negative.
103	GTYTXP1_225	MGTYTXP1_225	225	AT7	O, DIFF	GTY Bank225 channel1 High speed differential transmitter positive.
105	GTYTXN1_225	MGTYTXN1_225	225	AT6	O, DIFF	GTY Bank225 channel1 High speed differential transmitter negative.
109	GTYRXN1_225	MGTYRXN1_225	225	AT1	I, DIFF	GTY Bank225 channel1 High speed differential receiver negative.
111	GTYRXP1_225	MGTYRXP1_225	225	AT2	I, DIFF	GTY Bank225 channel1 High speed differential receiver positive.
115	GTYRXN0_225	MGTYRXN0_225	225	AU3	I, DIFF	GTY Bank225 channel0 High speed differential receiver negative.
117	GTYRXP0_225	MGTYRXP0_225	225	AU4	I, DIFF	GTY Bank225 channel0 High speed differential receiver positive.
123	GTYTXP2_225	MGTYTXP2_225	225	AR9	O, DIFF	GTY Bank225 channel2 High speed differential transmitter positive.
125	GTYTXN2_225	MGTYTXN2_225	225	AR8	O, DIFF	GTY Bank225 channel2 High speed differential transmitter negative.
129	GTYTXP3_225	MGTYTXP3_225	225	AP7	O, DIFF	GTY Bank225 channel3 High speed differential transmitter positive.

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
131	GTYTXN3_225	MGTYTXN3_225	225	AP6	O, DIFF	GTY Bank225 channel3 High speed differential transmitter negative.
135	GTYRXN3_225	MGTYRXN3_225	225	AP1	I, DIFF	GTY Bank225 channel3 High speed differential receiver negative.
137	GTYRXP3_225	MGTYRXP3_225	225	AP2	I, DIFF	GTY Bank225 channel3 High speed differential receiver positive.
141	GTYRXN2_225	MGTYRXN2_225	225	AR3	I, DIFF	GTY Bank225 channel2 High speed differential receiver negative.
143	GTYRXP2_225	MGTYRXP2_225	225	AR4	I, DIFF	GTY Bank225 channel2 High speed differential receiver positive.
98	GTREFCLK0P_225	MGTREFCLK0P_225	225	AT11	I, DIFF	GTY Bank225 differential reference clock0 positive.
100	GTREFCLK0N_225	MGTREFCLK0N_225	225	AT10	I, DIFF	GTY Bank225 differential reference clock0 negative.
158	GTREFCLK1P_225	MGTREFCLK1P_225	225	AP11	I, DIFF	GTY Bank225 differential reference clock1 positive.
160	GTREFCLK1N_225	MGTREFCLK1N_225	225	AP10	I, DIFF	GTY Bank225 differential reference clock1 negative.
Bank124 Transceiver Quad Pins						
183	GTYTXP0_124	MGTYTXP0_124	124	BF42	O, DIFF	GTY Bank124 channel0 High speed differential transmitter positive.
185	GTYTXN0_124	MGTYTXN0_124	124	BF43	O, DIFF	GTY Bank124 channel0 High speed differential transmitter negative.
189	GTYTXP1_124	MGTYTXP1_124	124	BD42	O, DIFF	GTY Bank124 channel1 High speed differential transmitter positive.
191	GTYTXN1_124	MGTYTXN1_124	124	BD43	O, DIFF	GTY Bank124 channel1 High speed differential transmitter negative.
195	GTYRXN1_124	MGTYRXN1_124	124	BA46	I, DIFF	GTY Bank124 channel1 High speed differential receiver negative.
197	GTYRXP1_124	MGTYRXP1_124	124	BD43	I, DIFF	GTY Bank124 channel1 High speed differential receiver positive.
201	GTYRXN0_124	MGTYRXN0_124	124	BC46	I, DIFF	GTY Bank124 channel0 High speed differential receiver negative.
203	GTYRXP0_124	MGTYRXP0_124	124	BC45	I, DIFF	GTY Bank124 channel0 High speed differential receiver positive.
217	GTYTXP2_124	MGTYTXP2_124	124	BB42	O, DIFF	GTY Bank124 channel2 High speed differential transmitter positive.
219	GTYTXN2_124	MGTYTXN2_124	124	BB43	O, DIFF	GTY Bank124 channel2 High speed differential transmitter negative.
223	GTYTXP3_124	MGTYTXP3_124	124	AW40	O, DIFF	GTY Bank124 channel3 High speed differential transmitter positive.

B2B-1 Pin No	B2B Connector1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
225	GTYTXN3_124	MGTYTXN3_124	124	AW41	O, DIFF	GTY Bank124 channel3 High speed differential transmitter negative.
229	GTYRXN3_124	MGTYRXN3_124	124	AV44	I, DIFF	GTY Bank124 channel3 High speed differential receiver negative.
231	GTYRXP3_124	MGTYRXP3_124	124	AV43	I, DIFF	GTY Bank124 channel3 High speed differential receiver positive.
235	GTYRXN2_124	MGTYRXN2_124	124	AW46	I, DIFF	GTY Bank124 channel2 High speed differential receiver negative.
237	GTYRXP2_124	MGTYRXP2_124	124	AW45	I, DIFF	GTY Bank124 channel2 High speed differential receiver positive.
184	GTREFCLK0P_124	MGTREFCLK0P_124	124	BA40	I, DIFF	GTY Bank124 differential reference clock0 positive.
186	GTREFCLK0N_124	MGTREFCLK0N_124	124	BA41	I, DIFF	GTY Bank124 differential reference clock0 negative.
218	GTREFCLK1P_124	MGTREFCLK1P_124	124	AY38	I, DIFF	GTY Bank124 differential reference clock1 positive.
220	GTREFCLK1N_124	MGTREFCLK1N_124	124	AY39	I, DIFF	GTY Bank124 differential reference clock1 negative.

2.8.2.2 FPGA IOs – HP BANK64

The Virtex UltraScale+ FPGA SOM supports 22 DIFF IOs/44 Single Ended (SE) IOs on Board-to-Board Connector1 from FPGA High-Performance (HP) Bank64. Upon these 22 DIFF IOs/44 SE IOs, up to 28 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank64 is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. By default, IO voltage of Bank64 is set as 1.0V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Virtex UltraScale+ FPGA datasheet. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for Bank64.

In the Virtex UltraScale+ FPGA SOM, Bank64 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank64 signals are routed as DIFF IOs, these pins can be used as SE IOs if required.

For more details on HP Bank64 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
27	PL_AV24_LVDS64_L14P_GC	IO_L14P_T2L_N2_GC_64	64	AV24	IO,1.8V	Bank64 IO14 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock.
29	PL_AW24_LVDS64_L14N_GC	IO_L14N_T2L_N3_GC_64	64	AW24	IO,1.8V	Bank64 IO14 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock.
31	PL_AL24_LVDS64_L22P	IO_L22P_T3U_N6_DBC_AD0P_64	64	AL24	IO,1.8V	Bank64 IO22 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input0 positive.
33	PL_AM24_LVDS64_L22N	IO_L22N_T3U_N7_DBC_AD0N_64	64	AM24	IO,1.8V	Bank64 IO22 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input0 negative.
87	PL_AT24_LVDS64_L18P	IO_L18P_T2U_N10_AD2P_64	64	AT24	IO,1.8V	Bank64 IO18 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input2 positive.
89	PL_AU24_LVDS64_L18N	IO_L18N_T2U_N11_AD2N_64	64	AU24	IO,1.8V	Bank64 IO18 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input2 negative.
91	PL_AR23_LVDS64_L17P	IO_L17P_T2U_N8_AD10P_64	64	AR23	IO,1.8V	Bank64 IO17 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input10 positive
93	PL_AT23_LVDS64_L17N	IO_L17N_T2U_N9_AD10N_64	64	AT23	IO,1.8V	Bank64 IO17 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input10 negative.
12	PL_AL22_LVDS64_L23P	IO_L23P_T3U_N8_64	64	AL22	IO,1.8V	Bank64 IO23 differential positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
14	PL_AM22_LVDS64_L23N	IO_L23N_T3U_N9_64	64	AM22	IO,1.8V	Bank64 IO23 differential negative or Single ended I/O.
16	PL_AU22_LVDS64_L15P	IO_L15P_T2L_N4_AD11P_64	64	AU22	IO,1.8V	Bank64 IO15 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input11 positive.
50	PL_AV22_LVDS64_L15N	IO_L15N_T2L_N5_AD11N_64	64	AV22	IO,1.8V	Bank64 IO15 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input11 negative.
22	PL_AP23_LVDS64_L20N	IO_L20N_T3L_N3_AD1N_64	64	AP23	IO,1.8V	Bank64 IO20 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input1 negative.
24	PL_AN23_LVDS64_L20P	IO_L20P_T3L_N2_AD1P_64	64	AN23	IO,1.8V	Bank64 IO20 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input1 positive.
40	PL_AP24_LVDS64_L21N	IO_L21N_T3L_N5_AD8N_64	64	AP24	IO,1.8V	Bank64 IO21 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input8 negative.
44	PL_AN24_LVDS64_L21P	IO_L21P_T3L_N4_AD8P_64	64	AN24	IO,1.8V	Bank64 IO21 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input8 positive.
46	PL_AR22_LVDS64_L16P	IO_L16P_T2U_N6_QBC_AD3P_64	64	AR22	IO,1.8V	Bank64 IO16 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input3 positive.
48	PL_AT22_LVDS64_L16N	IO_L16N_T2U_N7_QBC_AD3N_64	64	AT22	IO,1.8V	Bank64 IO16 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input3 negative.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
70	PL_AL21_LVDS64_L24P	IO_L24P_T3U_N10_64	64	AL21	IO,1.8V	Bank64 IO24 differential positive or Single ended I/O.
72	PL_AM21_LVDS64_L24N	IO_L24N_T3U_N11_64	64	AM21	IO,1.8V	Bank64 IO24 differential negative or Single ended I/O.
88	PL_AW23_LVDS64_L13N_GC	IO_L13N_T2L_N1_GC_QBC_64	64	AW23	IO,1.8V	Bank64 IO13 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock.
90	PL_AV23_LVDS64_L13P_GC	IO_L13P_T2L_N0_GC_QBC_64	64	AV23	IO,1.8V	Bank64 IO13 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock.
104	PL_BF22_LVDS64_L4N	IO_L4N_T0U_N7_DBC_AD7N_64	64	BF22	IO, 1.8V	Bank64 IO4 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 negative.
106	PL_BE20_LVDS64_L6N	IO_L6N_T0U_N11_AD6N_64	64	BE20	IO, 1.8V	Bank64 IO6 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 negative.
108	PL_BD20_LVDS64_L6P	IO_L6P_T0U_N10_AD6P_64	64	BD20	IO, 1.8V	Bank64 IO6 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 positive.
110	PL_BE21_LVDS64_L5N	IO_L5N_T0U_N9_AD14N_64	64	BE21	IO, 1.8V	Bank64 IO5 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input14 negative.
112	PL_BD21_LVDS64_L5P	IO_L5P_T0U_N8_AD14P_64	64	BD21	IO, 1.8V	Bank64 IO5 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input14 positive
128	PL_BE22_LVDS64_L4P	IO_L4P_T0U_N6_DBC_AD7P_64	64	BE22	IO, 1.8V	Bank64 IO4 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 positive.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
130	PL_BF24_LVDS64_L1P	IO_L1P_T0L_N0_DBC_64	64	BF24	IO, 1.8V	Bank64 IO1 differential positive or Single ended I/O.
132	PL_BF23_LVDS64_L1N	IO_L1N_T0L_N1_DBC_64	64	BF23	IO, 1.8V	Bank64 IO1 differential negative or Single ended I/O.
134	PL_BD24_LVDS64_L3N	IO_L3N_T0L_N5_AD15N_64	64	BD24	IO, 1.8V	Bank64 IO3 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 negative.
136	PL_BA20_LVDS64_L7P	IO_L7P_T1L_N0_QBC_AD13P_64	64	BA20	IO, 1.8V	Bank64 IO7 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 positive.
138	PL_BB20_LVDS64_L7N	IO_L7N_T1L_N1_QBC_AD13N_64	64	BB20	IO, 1.8V	Bank64 IO7 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 negative.
142	PL_BA22_LVDS64_L11N_GC	IO_L11N_T1U_N9_GC_64	64	BA22	IO, 1.8V	Bank64 IO11 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock.
144	PL_AY22_LVDS64_L11P_GC	IO_L11P_T1U_N8_GC_64	64	AY22	IO, 1.8V	Bank64 IO11 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock.
148	PL_BB24_LVDS64_L10N	IO_L10N_T1U_N7_QBC_AD4N_64	64	BB24	IO, 1.8V	Bank64 IO10 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input4 negative.
150	PL_BA24_LVDS64_L10P	IO_L10P_T1U_N6_QBC_AD4P_64	64	BA24	IO, 1.8V	Bank64 IO10 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input4 positive.
151	PL_BE23_LVDS64_L2N	IO_L2N_T0L_N3_64	64	BE23	IO, 1.8V	Bank64 IO2 differential negative or Single ended I/O.
153	PL_BD23_LVDS64_L2P	IO_L2P_T0L_N2_64	64	BD23	IO, 1.8V	Bank64 IO2 differential positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
152	PL_BC22_LVDS64_L9N	IO_L9N_T1L_N5_AD12N_64	64	BC22	IO, 1.8V	Bank64 IO9 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 negative.
154	PL_BB22_LVDS64_L9P	IO_L9P_T1L_N4_AD12P_64	64	BB22	IO, 1.8V	Bank64 IO9 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 positive.
172	PL_BC24_LVDS64_L3P	IO_L3P_T0L_N4_AD15P_64	64	BC24	IO, 1.8V	Bank64 IO3 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 positive.
236	PL_BA23_LVDS64_L12N_GC	IO_L12N_T1U_N11_GC_64	64	BA23	IO, 1.8V	Bank64 IO12 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock.
238	PL_AY23_LVDS64_L12P_GC	IO_L12P_T1U_N10_GC_64	64	AY23	IO, 1.8V	Bank64 IO12 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock.

**IO Type of IOs originating from VU13P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx VU13P FPGA datasheet.*

2.8.2.3 FPGA IOs – HP BANK68

The Virtex UltraScale+ FPGA SOM supports 12 DIFF IOs/24 Single Ended (SE) IOs on Board-to-Board Connector1 from FPGA High-Performance (HP) Bank68. Upon these 12 DIFF IOs/24 SE IOs, up to 4 Global Clock Inputs and up to 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank68 is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. By default, IO voltage of Bank68 is set as 1.0V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Virtex UltraScale+ FPGA datasheet. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for Bank68.

In the Virtex UltraScale+ FPGA SOM, Bank68 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank68 signals are routed as DIFF IOs, these pins can be used as SE IOs if required.

For more details on HP Bank68 pinouts on Board-to-Board Connector1, refer the below table

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
42	PL_BF10_LVDS68_L3P	IO_L3P_T0L_N4_AD15P_68	68	BF10	IO, 1.8V	Bank68 IO3 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 positive.
52	PL_BF9_LVDS68_L3N	IO_L3N_T0L_N5_AD15N_68	68	BF9	IO, 1.8V	Bank68 IO3 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 negative.
56	PL_BB10_LVDS68_L8N	IO_L8N_T1L_N3_AD5N_68	68	BB10	IO, 1.8V	Bank68 IO8 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input5 negative.
58	PL_BB11_LVDS68_L8P	IO_L8P_T1L_N2_AD5P_68	68	BB11	IO, 1.8V	Bank68 IO8 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input5 positive.
74	PL_BA7_LVDS68_L10P	IO_L10P_T1U_N6_QBC_AD4P_68	68	BA7	IO, 1.8V	Bank68 IO10 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input4 positive.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
76	PL_BB7_LVDS68_L10N	IO_L10N_T1U_N7_QBC_AD4N_68	68	BB7	IO, 1.8V	Bank68 IO10 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input4 negative.
82	PL_BC11_LVDS68_L7N	IO_L7N_T1L_N1_QBC_AD13N_68	68	BC11	IO, 1.8V	Bank68 IO7 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 negative.
84	PL_BC12_LVDS68_L7P	IO_L7P_T1L_N0_QBC_AD13P_68	68	BC12	IO, 1.8V	Bank68 IO7 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 positive.
92	PL_BC8_LVDS68_L9P	IO_L9P_T1L_N4_AD12P_68	68	BC8	IO, 1.8V	Bank68 IO9 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 positive.
94	PL_BC7_LVDS68_L9N	IO_L9N_T1L_N5_AD12N_68	68	BC7	IO, 1.8V	Bank68 IO9 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 negative.
116	PL_BF12_LVDS68_L5N	IO_L5N_T0U_N9_AD14N_68	68	BF12	IO, 1.8V	Bank68 IO5 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input14 negative.
118	PL_BE12_LVDS68_L5P	IO_L5P_T0U_N8_AD14P_68	68	BE12	IO, 1.8V	Bank68 IO5 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input14 positive.
124	PL_BD9_LVDS68_L6P	IO_L6P_T0U_N10_AD6P_68	68	BD9	IO, 1.8V	Bank68 IO6 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 positive.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
126	PL_BD8_LVDS68_L3P	IO_L6N_T0U_N11_AD6N_68	68	BD8	IO, 1.8V	Bank68 IO6 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 negative.
147	PL_BE7_LVDS68_L1P	IO_L1P_T0L_N0_DBC_68	68	BE7	IO, 1.8V	Bank68 IO1 differential positive or Single ended I/O.
149	PL_BF7_LVDS68_L1N	IO_L1N_T0L_N1_DBC_68	68	BF7	IO, 1.8V	Bank68 IO1 differential negative or Single ended I/O.
176	PL_BE10_LVDS68_L4N	IO_L4N_T0U_N7_DBC_AD7N_68	68	BE10	IO, 1.8V	Bank68 IO4 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 negative.
178	PL_BE11_LVDS68_L4P	IO_L4P_T0U_N6_DBC_AD7P_68	68	BE11	IO, 1.8V	Bank68 IO4 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 positive.
202	PL_BF8_LVDS68_L2N	IO_L2N_T0L_N3_68	68	BF8	IO, 1.8V	Bank68 IO2 differential negative or Single ended I/O.
204	PL_BE8_LVDS68_L2P	IO_L2P_T0L_N2_68	68	BE8	IO, 1.8V	Bank68 IO2 differential positive or Single ended I/O.
207	PL_BA8_LVDS68_L12N_GC	IO_L12N_T1U_N11_GC_68	68	BA8	IO, 1.8V	Bank68 IO12 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock.
209	PL_BA9_LVDS68_L12P_GC	IO_L12P_T1U_N10_GC_68	68	BA9	IO, 1.8V	Bank68 IO12 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock.
211	PL_BB9_LVDS68_L3P_GC	IO_L11P_T1U_N8_GC_68	68	BB9	IO, 1.8V	Bank68 IO11 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock.
213	PL_BC9_LVDS68_L11N_GC	IO_L11N_T1U_N9_GC_68	68	BC9	IO, 1.8V	Bank68 IO11 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock.

**IO Type of IOs originating from VU13P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx VU13P FPGA datasheet*

2.8.2.4 FPGA IOs – HP BANK65

The Virtex UltraScale+ FPGA SOM supports 5 DIFF IOs/12 Single Ended (SE) IOs on Board-to-Board Connector1 from FPGA High-Performance (HP) Bank65, up to 7 Global Clock Inputs are available.

The IO voltage of Bank65 is connected from LDO2 output of the PMIC. By Default, the Bank65 IO voltage is set to 1.8V.

In the Virtex UltraScale+ FPGA SOM, Bank65 signals are routed as DIFF IOs to Board-to-Board Connector1. Even though Bank65 signals are routed as DIFF IOs, these pins can be used as SE IOs if required.

For more details on HP Bank65 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
190	PL_AV26_LVDS65_L13P_A06_D22_GC	IO_L13P_T2L_N0_GC_QBC_A06_D22_65	65	AV26	IO, 1.8V	Bank65 Single ended I/O. Same pin can be configured as GC Global Clock.
192	PL_AY27_LVDS65_L11N_A11_D27_GC	IO_L11N_T1U_N9_GC_A11_D27_65	65	AY27	IO, 1.8V	Bank65 Single ended I/O. Same pin can be configured as GC Global Clock.
194	PL_AY26_LVDS65_L11P_A10_D26_GC	IO_L11P_T1U_N8_GC_A10_D26_65	65	AY26	IO, 1.8V	Bank65 Single ended I/O. Same pin can be configured as GC Global Clock.
196	PL_AY28_LVDS65_L12N_A09_D25_GC	IO_L12N_T1U_N11_GC_A09_D25_65	65	AY28	IO, 1.8V	Bank65 Single ended I/O. Same pin can be configured as GC Global Clock.
198	PL_AW28_LVDS65_L12P_A08_D24_GC	IO_L12P_T1U_N10_GC_A08_D24_65	65	AW28	IO, 1.8V	Bank65 Single ended I/O. Same pin can be configured as GC Global Clock.
210	PL_BC27_LVDS65_L6N	IO_L6N_T0U_N11_AD6N_A21_65	65	BC27	IO, 1.8V	Bank65 Single ended I/O.
212	PL_AV27_LVDS65_L14P_A04_D20_GC	IO_L14P_T2L_N2_GC_A04_D20_65	65	AV27	IO, 1.8V	Bank65 Single ended I/O. Same pin can be configured as GC Global Clock.
214	PL_AV28_LVDS65_L14N_A05_D21_GC	IO_L14N_T2L_N3_GC_A05_D21_65	65	AV28	IO, 1.8V	Bank65 Single ended I/O. Same pin can be configured as GC Global Clock.
224	GA1(PL_AP26_LVDS65_L19N_DBC_D11)	IO_L19N_T3L_N1_DBC_AD9N_D11_65	65	AP26	IO, 1.8V	Bank65 Single ended I/O.
226	GA2(PL_AP25_LVDS65_L19P_DBC_D10)	IO_L19P_T3L_N0_DBC_AD9P_D10_65	65	AP25	IO, 1.8V	Bank65 Single ended I/O.
228	GA3(PL_AT28_LVDS65_L18N_D13)	IO_L18N_T2U_N11_AD2N_D13_65	65	AT28	IO, 1.8V	Bank65 Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
230	GA4(PL_AR28_LVDS65_L18P_D12)	IO_L18P_T2U_N10_AD2P_D12_65	65	AR28	IO, 1.8V	Bank65 Single ended I/O.

**IO Type of IOs originating from VU13P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx VU13P FPGA datasheet.*

2.8.3 Power Control Input

The Virtex UltraScale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin in Board-to-Board Connector1. Also, in Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance. For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
232	SOMPWR_EN	NA	NA	NA	I, 5V	Active High SOM power enable. *Important Note:* *High – SOM power ON* *Low – SOM Power OFF*
1, 7, 13, 19, 25, 35, 41, 47, 53, 59, 61, 67, 73, 79, 85, 95, 101, 107, 113, 119, 121, 127, 133, 139, 145, 155, 161, 167, 173, 179, 181, 187, 193, 199, 205, 215, 221, 227, 233, 239, 2, 8, 20, 26, 36, 54, 60, 62, 68, 80, 86, 96, 102, 114, 120, 122, 140, 146, 156, 162, 174, 180, 182, 188, 200, 206, 216, 222, 234, 240	GND	NA	NA	NA	Power	Ground.

2.9 Board to Board Connector2

The Virtex UltraScale+ FPGA SOM Board to Board connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2 (J6) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A from Samtec

Mating Connector - QSH-120-01-L-D-A from Samtec

Staking Height - 5mm

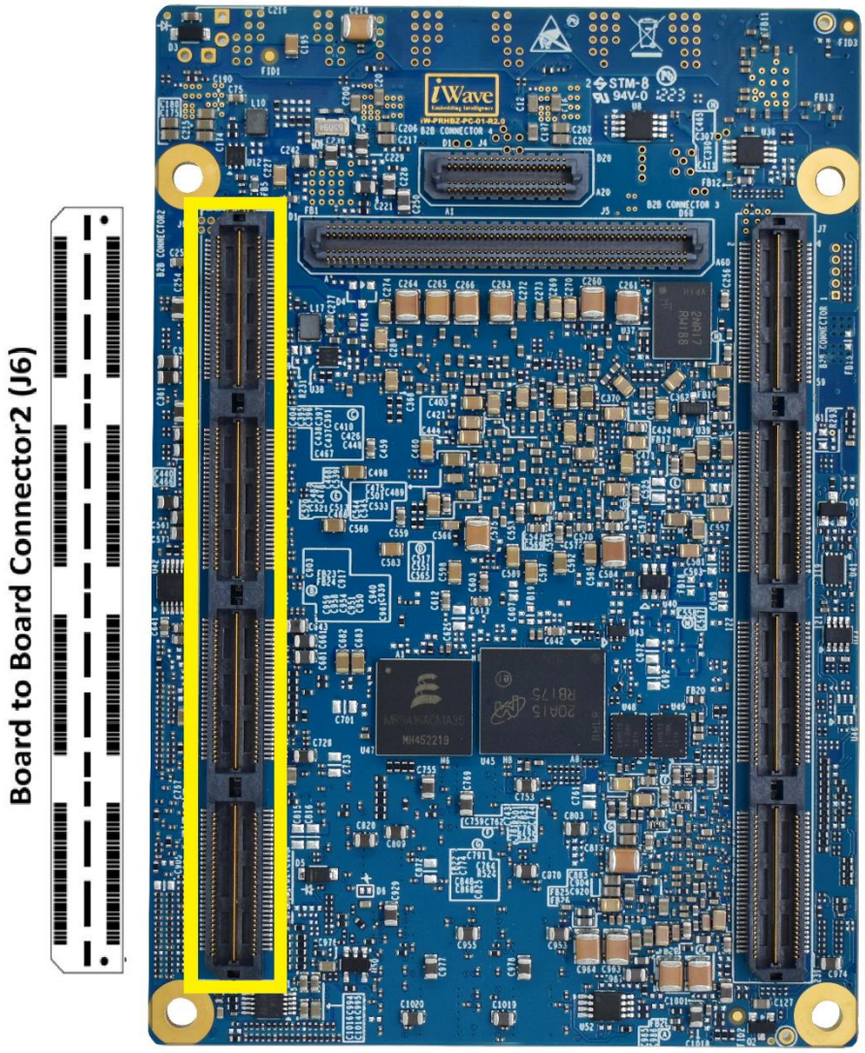


Figure 6: Board to Board Connector2

Table 4: Board to Board Connector2 Pinout

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
VCC_5V	1	2	VCC_5V
VCC_5V	3	4	VCC_5V
VCC_5V	5	6	VCC_5V
VCC_5V	7	8	VCC_5V
VCC_5V	9	10	VCC_5V
VCC_5V	11	12	VCC_5V
VCC_5V	13	14	VCC_5V
VCC_5V	15	16	VCC_5V
VCC_5V	17	18	VCC_5V
VCC_5V	19	20	VCC_5V
GND	21	22	GND
GND	23	24	GND
JTAG_TRST	25	26	LS_USB1_D_M
JTAG_TDI	27	28	LS_USB1_D_P
JTAG_TMS	29	30	GND
JTAG_TCK	31	32	LS_USB2EN_GPIO3_16(EC2_TXD2)
JTAG_TDO	33	34	LS_USB1_ID
RESET_SW_IN	35	36	LS_USB1_VBUS
GND	37	38	LS_IIC2_SDA
GPHY_DTXRXM	39	40	PL_AP28_LVDS65_L20N_D09
GPHY_DTXRXP	41	42	GPIO4_26(SDHC_DAT7)
GND	43	44	GPIO4_16(TDMB_TXD)
GPHY_CTXRXM	45	46	LS_IIC1_SDA
GPHY_CTXRXP	47	48	LS_IIC1_SCL
GND	49	50	LS_LPUART3_SOUT
GPHY_BTXRXM	51	52	LS_LPUART3_SIN
GPHY_BTXRXP	53	54	LS_UART1_SOUT
GND	55	56	LS_UART1_SIN
GPHY_ATXRXM	57	58	GPHY_LINK_LED2
GPHY_ATXRXP	59	60	GPHY_ACTIVITY_LED1
GPIO3_15(EC2_TXD3)	61	62	GPIO4_19(CLK09)
PL_AN28_LVDS65_L20P_D08	63	64	GPIO4_14(TDMB_RXD)
GPIO4_25(SDHC_DAT6)	65	66	GPIO4_15(TDMB_RSYNC)
PL_AV17_T1U_N12_66	67	68	VRTC_3V0
GPIO4_18(TDMB_RQ)	69	70	LS_IIC2_SCL
GPIO4_12(TDMA_TSYNC)	71	72	GPIO4_24(SDHC_DAT5)
GND	73	74	GND
PL_AV16_LVDS67_L18N	75	76	LS_IIC2_SCL
PL_AU16_LVDS67_L18P	77	78	LS_IIC2_SDA

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
LS_LPUART5_SIN	79	80	PL_AY11_LVDS67_L8N
LS_LPUART5_SOUT	81	82	PL_AY12_LVDS67_L8P
PL_AR13_LVDS67_L22N_DBC	83	84	PL_BF13_LVDS67_L1N
PL_AP13_LVDS67_L22P_DBC	85	86	PL_BF14_LVDS67_L1P
PL_AR16_LVDS67_L19P_DBC	87	88	PL_BC14_LVDS67_L6P
PL_AR15_LVDS67_L19N_DBC	89	90	PL_BC13_LVDS67_L6N
PL_AL15_LVDS67_L23P	91	92	PL_AU13_LVDS67_L15P
PL_AM15_LVDS67_L23N	93	94	PL_AV13_LVDS67_L15N
PL_BD13_LVDS67_L4P_DBC	95	96	PL_AV14_LVDS67_L16N_QBC
PL_BE13_LVDS67_L4N_DBC	97	98	PL_AU14_LVDS67_L16P_QBC
PL_AN14_LVDS67_L21P	99	100	PL_BB15_LVDS67_L10P_QBC
PL_AN13_LVDS67_L21N	101	102	PL_BB14_LVDS67_L10N_QBC
PL_AP15_LVDS67_L20P	103	104	PL_BA12_LVDS67_L7P_QBC
PL_AP14_LVDS67_L20N	105	106	PL_BB12_LVDS67_L7N_QBC
GND	107	108	GND
PL_AW16_LVDS67_L14P_GC	109	110	PL_AW14_LVDS67_L13P_GC
PL_AW15_LVDS67_L14N_GC	111	112	PL_AW13_LVDS67_L13N_GC
GND	113	114	GND
PL_AY13_LVDS67_L12P_GC	115	116	PL_BA15_LVDS67_L11P_GC
PL_BA13_LVDS67_L12N_GC	117	118	PL_BA14_LVDS67_L11N_GC
GND	119	120	GND
PL_AY15_LVDS67_L9N	121	122	PL_AN18_LVDS66_L19P_DBC
PL_AY16_LVDS67_L9P	123	124	PL_AN17_LVDS66_L19N_DBC
PL_BE16_LVDS67_L3N	125	126	PL_AW20_LVDS66_L9P
PL_BD16_LVDS67_L3P	127	128	PL_AY20_LVDS66_L9N
GND	129	130	GND
PL_AL20_LVDS66_L24P	131	132	PL_AL17_LVDS66_L22P_DBC
PL_AM20_LVDS66_L24N	133	134	PL_AM17_LVDS66_L22N_DBC
PL_AN19_LVDS66_L20P	135	136	PL_AM16_LVDS66_L21P
PL_AP19_LVDS66_L20N	137	138	PL_AN16_LVDS66_L21N
PL_BD15_LVDS67_L5P	139	140	PL_AL19_LVDS66_L23P
PL_BD14_LVDS67_L5N	141	142	PL_AM19_LVDS66_L23N
PL_BF15_LVDS67_L2N	143	144	PL_AP18_LVDS66_L17P
PL_BE15_LVDS67_L2P	145	146	PL_AR18_LVDS66_L17N
PL_AP20_LVDS66_L18P	147	148	PL_BD18_LVDS66_L3P
PL_AR20_LVDS66_L18N	149	150	PL_BE18_LVDS66_L3N
PL_AY18_LVDS66_L8P	151	152	PL_BE17_LVDS66_L1P_DBC
PL_BA18_LVDS66_L8N	153	154	PL_BF17_LVDS66_L1N_DBC
PL_AV21_LVDS66_L10P_QBC	155	156	PL_AR17_LVDS66_L16P_QBC
PL_AW21_LVDS66_L10N_QBC	157	158	PL_AT17_LVDS66_L16N_QBC
PL_BC19_LVDS66_L4P_DBC	159	160	PL_BF18_LVDS66_L2N

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
PL_BD19_LVDS66_L4N_DBC	161	162	PL_BF19_LVDS66_L2P
PL_BB19_LVDS66_L6P	163	164	PL_AT18_LVDS66_L15P
PL_BC18_LVDS66_L6N	165	166	PL_AU17_LVDS66_L15N
GND	167	168	GND
PL_AT20_LVDS66_L14P_GC	169	170	PL_AV19_LVDS66_L12P_GC
PL_AU20_LVDS66_L14N_GC	171	172	PL_AW19_LVDS66_L12N_GC
GND	173	174	GND
PL_AT19_LVDS66_L13P_GC	175	176	PL_AV18_LVDS66_L11P_GC
PL_AU19_LVDS66_L13N_GC	177	178	PL_AW18_LVDS66_L11N_GC
GND	179	180	GND
PL_BC17_LVDS66_L5N	181	182	PL_AY17_LVDS66_L7P_QBC
PL_BB17_LVDS66_L5P	183	184	PL_BA17_LVDS66_L7N_QBC
GND	185	186	GND
GTYRXP0_125	187	188	GTREFCLK0P_125
GTYRXN0_125	189	190	GTREFCLK0N_125
GND	191	192	GND
GTYTXP0_125	193	194	GTYRXP3_125
GTYTXN0_125	195	196	GTYRXN3_125
GND	197	198	GND
GTYRXP1_125	199	200	GTYTXP3_125
GTYRXN1_125	201	202	GTYTXN3_125
GND	203	204	GND
GTYTXP1_125	205	206	LS_SD1_RX1_P
GTYTXN1_125	207	208	LS_SD1_RX1_N
GND	209	210	GND
GTYRXP2_125	211	212	LS_SD1_TX1_P
GTYRXN2_125	213	214	LS_SD1_TX1_N
GND	215	216	GND
GTYTXP2_125	217	218	NC
GTYTXN2_125	219	220	NC
GND	221	222	GND
GTREFCLK1P_125	223	224	JTAG_MUX_SEL
GTREFCLK1N_125	225	226	NC
GND	227	228	GND
LS_USB1_RX_P	229	230	NC
LS_USB1_RX_M	231	232	NC
GND	233	234	GND
LS_USB1_TX_P	235	236	NC
LS_USB1_TX_M	237	238	NC
GND	239	240	GND

2.9.1 LS1021A Interfaces

The interfaces which are supported in Board-to-Board Conenector2 from LS1021A Processor is explained in the following section.

2.9.1.1 USB3.0

The LS1021A Layerscape processor supports USB3.0 interface through Board-to-Board Connector2 from USB PHY integrated in the Layerscape processor.

For more details on USB3.0 pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
157	LS_USB1_TX_P	USB1_TX_P	B2	O, USB	USB PHY 3.0 Transmit Data Positive
159	LS_USB1_TX_M	USB1_TX_M	A2	O, USB	USB PHY 3.0 Transmit Data Negative
175	LS_USB1_RX_M	USB1_RX_M	A4	I, USB	USB PHY 3.0 Receive Data Negative
177	LS_USB1_RX_P	USB1_RX_P	B4	I, USB	USB PHY 3.0 Receive Data Positive

2.9.1.2 Gigabit Ethernet Interface

The Virtex UltraScale+ FPGA SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2.The MAC is integrated in the LS1021A Processor and connected to the external Gigabit Ethernet PHY “KSZ9031RNXIC” on SOM. This Gigabit Ethernet PHY is interfaced with Ethernet Controller 1 RGMII interface of LS1021A and works at 1.8V IO voltage level.

In Virtex UltraScale+ FPGA SOM, LS1021A GPIO “LS_ETH_RSTN_GPIO4_23(SDHC_DAT4)” is used for Ethernet PHY reset. Also, SOM supports Ethernet PHY interrupt through LS1021A GPIO “LS_ETH_INT_GPIO1_25(IRQ5)”. This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magjack is required on the carrier board.

In Virtex UltraScale+ FPGA SOM, Ethernet PHY Address is fixed to 001 as per below table.

PHYADDRESS2	PHYADDRESS1	PHYADDRESS0	Ethernet PHY Address
PHYAD2	GPHY_LINK_LED2	GPHY_ACTIVITY_LED1	1
0(PD)	0(PD)	1(PU)	

Important Note: GPHY_ACTIVITY_LED1 signal is muxed with PHYADDRESS2 pin. The same GPHY_ACTIVITY_LED1 signal is connected to 60th pin of Board to Board connector2 to support Gigabit Ethernet Activity LED.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
59	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
57	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
53	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
51	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
47	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
45	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
41	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
39	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
60	GPHY_ACTIVITY_LED1	NA	NA	NA	O, 1.8V CMOS/ 10K PU	Gigabit Ethernet 1000Mbps Link status LED (Active High).
58	GPHY_LINK_LED2	NA	NA	NA	O, 1.8V CMOS/ 10K PD	Gigabit Ethernet Activity LED (Active High).

2.9.1.3 USB2.0 Interface

The Virtex UltraScale+ FPGA SOM supports one USB2.0 & 3.0 OTG interface on Board-to-Board Connector2 & 1. USB1 controller of LS1021A is used for USB2.0 & 3.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 & 3.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

Also, Virtex UltraScale+ FPGA SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
26	LS_USB1_D_M	USB1_D_M	C3	IO, USB	USB PHY Data Minus
28	LS_USB1_D_P	USB1_D_P	D3	IO, USB	USB PHY Data Plus
34	LS_USB1_ID	USB1_ID	E3	I, 3.3V	USB PHY ID Detect
36	LS_USB1_VBUS	USB1_VBUS	C1	I,5V Power	USB VBUS for VBUS monitoring.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
32	USB2EN_GPIO3_16 (EC2_TXD2)	EC2_TXD2/GPIO 3_16/CAN3_TX/ USB2_D6/FTM2 _CH7	R3	O, 3.3V	USB Power Enable Output from LS1021A

2.9.1.4 Debug UART Interface

The Virtex UltraScale+ FPGA SOM supports one Debug UART interface on Board-to-Board Connector2. The DUART controller of LS1021A is used for Debug UART interface. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
54	LS_UART1_SOUT	UART1_SOUT/G PIO1_15	N1	O, 1.8V LVCMOS	Debug UART Transmit data
56	LS_UART1_SIN	UART1_SIN/GPI O1_17	M1	I, 1.8V LVCMOS	Debug UART Receive data

2.9.1.5 Data UART Interface

The Virtex UltraScale+ FPGA SOM supports two DATA UART interface on Board-to-Board Connector2. The pins from eSDHC controller of alternate function are used in the Data UART interface. This controller supports full-duplex asynchronous receiver and transmitter path with autobaud rates.

For more details on Data UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
50	LS_LPUART3_SOUT	SDHC_CMD/GPIO2_04/LPUAR T3_SOUT	E2	O, 1.8V LVCMOS	Data UART Transmit Data
52	LS_LPUART3_SIN	SDHC_DAT0/GPIO2_05/LPUAR T3_SIN	E1	I, 1.8V LVCMOS	Data UART Receive Data
81	LS_LPUART5_SOUT	SDHC_DAT1/GPIO2_06/LPUAR T2_RTS_B/LPUART5_SOUT	F2	O, 1.8V LVCMOS	Data UART Transmit Data
79	LS_LPUART5_SIN	SDHC_DAT2/GPIO2_07/LPUAR T2_CTS_B/LPUART5_SIN	F1	I, 1.8V LVCMOS	Data UART Receive Data

2.9.1.6 I2C Interface

The Virtex UltraScale+ FPGA SOM supports two I2C interface on Board-to-Board Connector2. The I2C controller of LS1021A processor's is used for I2C interface with the standard NXP I2C bus protocol. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C2 interface is connected to On-SOM PMIC with I2C address 0x58 and 0x48, MPS Regulator with

I2C address 0x60, Temperature Sensor with I2C address 0x4C and Clock Synthesizer with I2C address 0x76 in the Virtex UltraScale+ FPGA SOM. Also, one more I2C interface (I2C1) can be taken out on Board-to-Board Connector2.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
46	LS_IIC1_SDA	IIC1_SDA	P6	IO, 1.8V	I2C1 Serial Data
48	LS_IIC1_SCL	IIC1_SCL	N6	O, 1.8V	I2C1 Serial Clock
76	LS_IIC2_SCL	IIC2_SCL/GPIO4_27/SDHC_CD_B/SPI2_PCS3	K1	O, 1.8V	I2C2 Serial Clock
78	LS_IIC2_SDA	IIC2_SDA/GPIO4_28/SDHC_WP/SPI2_PCS4	L1	IO, 1.8V	I2C2 Serial Data

2.9.1.7 JTAG Interface

The Virtex UltraScale+ FPGA SOM supports JTAG interface on Board-to-Board Connector2. Both LS1021A and FPGA share a common set of JTAG pins in the Board-to-Board2 connector and each have their own TAP controller. FPGA and LS1021A's JTAG signals are given to JTAG Selection 2:1 Mux IC which will select according to JTAG_SEL pin configuration.

Refer the below table for JTAG selection details.

JTAG_SEL	JTAG Controller
0	LS1021A
1	FPGA

By default, the JTAG_SEL will be high and FPGA will be selected as JTAG controller. Refer the below given pinout for more details.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
27	JTAG_TDI	TDI_0	0	AE15	I, 1.8V LVCMOS	JTAG Test Data Input.
29	JTAG_TMS	TMS_0	0	AG15	I, 1.8V LVCMOS	JTAG Test Mode Select.
31	JTAG_TCK	TCK_0	0	AE13	I, 1.8V LVCMOS	JTAG Test Clock.
33	JTAG_TDO	TDO_0	0	AC13	O, 1.8V LVCMOS	JTAG Test Data Output.

If the JTAG_SEL pin is low it will select LS1021A as JTAG controller. Refer the below pinout for more details.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
25	LS_JTAG_TRST	TRST_B	F6	I, 1.8V LVCMOS	JTAG Test Reset from LS1021A
27	JTAG_TDI	TDI	E7	I, 1.8V LVCMOS	JTAG Test Data Input.
29	JTAG_TMS	TMS	F8	I, 1.8V LVCMOS	JTAG Test Mode Select.
31	JTAG_TCK	TCK	E8	I, 1.8V LVCMOS	JTAG Test Clock.
33	JTAG_TDO	TDO	F7	O, 1.8V LVCMOS	JTAG Test Data Output.

2.9.1.8 SerDes Interface

The Virtex UltraScale+ FPGA SOM supports 1 highspeed SerDes lanes through LS1021A Layerscape Processor in board-to-board connector2

For more details on SerDes Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
206	LS_SD1_RX1_P	SD1_RX1_P	AC11	I, DIFF	SerDes Receive Data1 Positive
208	LS_SD1_RX1_N	SD1_RX1_N	AB11	I, DIFF	SerDes Receive Data1 Negative
212	LS_SD1_TX1_P	SD1_TX1_P	W11	O, DIFF	SerDes Transmit Data1 Positive
214	LS_SD1_TX1_N	SD1_TX1_N	Y11	O, DIFF	SerDes Transmit Data1 Negative
218	LS_SD1_REF_CLK2_P	SD1_REF_CLK2_P	AC16	I, DIFF	SerDes PLL 2 Reference Clock Positive
220	LS_SD1_REF_CLK2_N	SD1_REF_CLK2_N	AB16	I, DIFF	SerDes PLL 2 Reference Clock Negative

2.9.1.9 GPIOs From LS1021A

The Virtex UltraScale+ FPGA SOM supports 11 GPIOs from LS1021A Layerscape Processor in board-to-board connector2

For more details on GPIOs pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	LS1021A Pin Name	LS1021A Pin No	Signal Type/ Termination	Description
44	GPIO4_16(TDMB_TXD)	TDMB_TXD/GPIO4_16/UC3_TXD7/SPDIF_OUT/SAI4_TX_DATA/FTM4_CH0/2D-ACE_D07	M3	IO, 1.8V	General Purpose I/O from LS1021A
61	GPIO3_15(EC2_TXD3)	EC2_TXD3/GPIO3_15/CAN4_TX/USB2_D7/FTM2_CH5	R4	IO, 1.8V	General Purpose I/O from LS1021A
62	GPIO4_19(CLK09)	CLK09/GPIO4_19/BRGO2/SAI3_RX_BCLK/FTM4_QD_PHA/2D-ACE_D10	K5	IO, 1.8V	General Purpose I/O from LS1021A
64	GPIO4_14(TDMB_RXD)	TDMB_RXD/GPIO4_14/UC3_RXD7/SPDIF_IN/SAI4_RX_DATA/FTM4_CH2/2D-ACE_D05	K3	IO, 1.8V	General Purpose I/O from LS1021A
65	GPIO4_25(SDHC_DAT6)	SDHC_DAT6/GPIO4_25/USB1_DRVVBUS/SDHC_DAT0_DIR	J2	IO, 1.8V	General Purpose I/O from LS1021A
66	GPIO4_15(TDMB_RSYNC)	TDMB_RSYNC/GPIO4_15/UC3_CTSB_RXDV/SPDIF_PLOCK/SAI4_TX_BCLK/FTM4_CH1/2D-ACE_D06	L3	IO, 1.8V	General Purpose I/O from LS1021A
69	GPIO4_18(TDMB_RQ)	TDMB_RQ/GPIO4_18/UC3_CDB_RXER/SPDIF_EXTCLK/SAI4_RX_BCLK/FTM4_EXTCLK/2D-ACE_D09	K4	IO, 1.8V	General Purpose I/O from LS1021A
71	GPIO4_12(TDMA_TSYNC)	TDMA_TSYNC/GPIO4_12/UC1_RTSB_TXEN/SAI3_TX_SYNC/FTM4_CH4/2D-ACE_D03	J5	IO, 1.8V	General Purpose I/O from LS1021A
42	GPIO4_26(SDHC_DAT7	SDHC_DAT7/GPIO4_26/USB1_PWRFAULT/SDHC_DAT123_DIR	J1	IO, 1.8V	General Purpose I/O from LS1021A
72	GPIO4_24(SDHC_DAT5)	SDHC_DAT5/GPIO4_24/SDHC_CMD_DIR	H1	IO, 1.8V	General Purpose I/O from LS1021A

2.9.2 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Virtex UltraScale+ FPGA is explained in the following section.

2.9.2.1 GTY High Speed Transceivers

The Virtex UltraScale+ FPGA supports 4 GTY transceivers through one transceiver Quad with line rate from 500Mbps to 32.75Gbps based on the speed grade of the FPGA. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

In Virtex UltraScale+ FPGA SOM, on board reference clock to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required

peripheral standards on GTY transceivers. Also, on board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommend.

For more details on GTY transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
Bank125 Transceiver Quad Pins						
193	GTYTXP0_125	MGTYTXP0_125	125	AU40	O, DIFF	GTY Bank125 channel0 High speed differential transmitter positive.
195	GTYTXN0_125	MGTYTXN0_125	125	AU41	O, DIFF	GTY Bank125 channel0 High speed differential transmitter negative.
205	GTYTXP1_125	MGTYTXP1_125	125	AT38	O, DIFF	GTY Bank125 channel1 High speed differential transmitter positive.
207	GTYTXN1_125	MGTYTXN1_125	125	AT39	O, DIFF	GTY Bank125 channel1 High speed differential transmitter negative.
201	GTYRXN1_125	MGTYRXN1_125	125	AT44	I, DIFF	GTY Bank125 channel1 High speed differential receiver negative.
199	GTYRXP1_125	MGTYRXP1_125	125	AT43	I, DIFF	GTY Bank125 channel1 High speed differential receiver positive.
189	GTYRXN0_125	MGTYRXN0_125	125	AU46	I, DIFF	GTY Bank125 channel0 High speed differential receiver negative.
187	GTYRXP0_125	MGTYRXP0_125	125	AU45	I, DIFF	GTY Bank125 channel0 High speed differential receiver positive.
217	GTYTXP2_125	MGTYTXP2_125	125	AR40	O, DIFF	GTY Bank125 channel2 High speed differential transmitter positive.
219	GTYTXN2_125	MGTYTXN2_125	125	AR41	O, DIFF	GTY Bank125 channel2 High speed differential transmitter negative.
200	GTYTXP3_125	MGTYTXP3_125	125	AP38	O, DIFF	GTY Bank125 channel3 High speed differential transmitter positive.
202	GTYTXN3_125	MGTYTXN3_125	125	AP39	O, DIFF	GTY Bank125 channel3 High speed differential transmitter negative.
196	GTYRXN3_125	MGTYRXN3_125	125	AP44	I, DIFF	GTY Bank125 channel3 High speed differential receiver negative.
194	GTYRXP3_125	MGTYRXP3_125	125	AP43	I, DIFF	GTY Bank125 channel3 High speed differential receiver positive.
213	GTYRXN2_125	MGTYRXN2_125	125	AR46	I, DIFF	GTY Bank125 channel2 High speed differential receiver negative.
211	GTYRXP2_125	MGTYRXP2_125	125	AR45	I, DIFF	GTY Bank125 channel2 High speed differential receiver positive.
188	GTREFCLK0P_125	MGTREFCLK0P_125	125	AV38	I, DIFF	GTY Bank125 differential reference clock0 positive.
190	GTREFCLK0N_125	MGTREFCLK0N_125	125	AV39	I, DIFF	GTY Bank125 differential reference clock0 negative.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
223	GTREFCLK1P_125	MGTREFCLK1P_125	125	AU36	I, DIFF	GTY Bank125 differential reference clock1 positive.
225	GTREFCLK1N_125	MGTREFCLK1N_125	125	AU37	I, DIFF	GTY Bank125 differential reference clock1 negative.

2.9.2.2 FPGA IOs – HP BANK66

The Virtex UltraScale+ FPGA SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector2 from FPGA's High Performance (HP) Bank66. Upon these 24 LVDS IOs/48 SE IOs, up to 4 GC Global Clock Inputs and up to 16 SYSMON auxiliary analog inputs are available.

The IO voltage of Bank66 is connected from LDO3 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. By default, IO voltage of Bank66 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Virtex UltraScale+ FPGA datasheet. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO3 to output appropriate IO voltage for Bank66.

In the Virtex UltraScale+ FPGA SOM, Bank66 signals are routed as LVDS IOs to Board-to-Board Connector2. Even though Bank66 signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

For more details on HP Bank66 pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
131	PL_AL20_LVDS66_L24P	IO_L24P_T3U_N10_66	66	AL20	IO, 1.8V	Bank66 IO24 differential positive or Single ended I/O.
133	PL_AM20_LVDS66_L24N	IO_L24N_T3U_N11_66	66	AM20	IO, 1.8V	Bank66 IO24 differential negative or Single ended I/O.
135	PL_AN19_LVDS66_L20P	IO_L20P_T3L_N2_AD1P_66	66	AN19	IO, 1.8V	Bank66 IO20 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input1 positive.
137	PL_AP19_LVDS66_L20N	IO_L20N_T3L_N3_AD1N_66	66	AP19	IO, 1.8V	Bank66 IO20 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input1 negative.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
147	PL_AP20_LVDS66_L18P	IO_L18P_T2U_N10_AD2P_66	66	AP20	IO, 1.8V	Bank66 IO18 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input2 positive.
149	PL_AR20_LVDS66_L18N	IO_L18N_T2U_N11_AD2N_66	66	AR20	IO, 1.8V	Bank66 IO18 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input2 negative.
151	PL_AY18_LVDS66_L8P	IO_L8P_T1L_N2_AD5P_66	66	AY18	IO, 1.8V	Bank66 IO8 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input5 positive.
153	PL_BA18_LVDS66_L8N	IO_L8N_T1L_N3_AD5N_66	66	BA18	IO, 1.8V	Bank66 IO8 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input5 negative.
155	PL_AV21_LVDS66_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_66	66	AV21	IO, 1.8V	Bank66 IO10 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input4 positive.
157	PL_AW21_LVDS66_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_66	66	AW21	IO, 1.8V	Bank66 IO10 differential negative or Single ended I/O . Same pin can be configured as PLSYSMON differential analog input4 negative .
159	PL_BC19_LVDS66_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_66	66	BC19	IO, 1.8V	Bank66 IO4 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 positive.
161	PL_BD19_LVDS66_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_66	66	BD19	IO, 1.8V	Bank66 IO4 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 negative.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
163	PL_BB19_LVDS66_L6P	IO_L6P_T0U_N10_AD6P_66	66	BB19	IO, 1.8V	Bank66 IO6 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 positive.
165	PL_BC18_LVDS66_L6N	IO_L6N_T0U_N11_AD6N_66	66	BC18	IO, 1.8V	Bank66 IO6 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 negative.
169	PL_AT20_LVDS66_L14P_GC	IO_L14P_T2L_N2_GC_66	66	AT20	IO, 1.8V	Bank66 IO14 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock Input differential positive.
171	PL_AU20_LVDS66_L14N_GC	IO_L14N_T2L_N3_GC_66	66	AU20	IO, 1.8V	Bank66 IO14 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock Input differential negative.
175	PL_AT19_LVDS66_L13P_GC	IO_L13P_T2L_N0_GC_QBC_66	66	AT19	IO, 1.8V	Bank66 IO13 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock Input differential positive.
177	PL_AU19_LVDS66_L13N_GC	IO_L13N_T2L_N1_GC_QBC_66	66	AU19	IO, 1.8V	Bank66 IO13 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock Input differential negative.
181	PL_BC17_LVDS66_L5N	IO_L5N_T0U_N9_AD14N_66	66	BC17	IO, 1.8V	Bank66 IO5 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input14 negative.
183	PL_BB17_LVDS66_L5P	IO_L5P_T0U_N8_AD14P_66	66	BB17	IO, 1.8V	Bank66 IO5 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 positive.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
122	PL_AN18_LVDS66_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_66	66	AN18	IO, 1.8V	Bank66 IO19 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input9 positive.
124	PL_AN17_LVDS66_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_66	66	AN17	IO, 1.8V	Bank66 IO19 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input9 negative.
126	PL_AW20_LVDS66_L9P	IO_L9P_T1L_N4_AD12P_66	66	AW20	IO, 1.8V	Bank66 IO9 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 positive.
128	PL_AY20_LVDS66_L9N	IO_L9N_T1L_N5_AD12N_66	66	AY20	IO, 1.8V	Bank66 IO9 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 negative.
132	PL_AL17_LVDS66_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_66	66	AL17	IO, 1.8V	Bank66 IO22 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input0 positive.
134	PL_AM17_LVDS66_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_66	66	AM17	IO, 1.8V	Bank66 IO22 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input0 negative.
136	PL_AM16_LVDS66_L21P	IO_L21P_T3L_N4_AD8P_66	66	AM16	IO, 1.8V	PL Bank66 IO21 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input8 positive.
138	PL_AN16_LVDS66_L21N	IO_L21N_T3L_N5_AD8N_66	66	AN16	IO, 1.8V	Bank66 IO21 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input8 negative.
140	PL_AL19_LVDS66_L23P	IO_L23P_T3U_N8_66	66	AL19	IO, 1.8V	Bank66 IO23 differential positive or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
142	PL_AM19_LVDS66_L23N	IO_L23N_T3U_N9_66	66	AM19	IO, 1.8V	Bank66 IO23 differential negative or Single ended I/O.
144	PL_AP18_LVDS66_L17P	IO_L17P_T2U_N8_AD10P_66	66	AP18	IO, 1.8V	Bank66 IO17 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input10 positive.
146	PL_AR18_LVDS66_L17N	IO_L17N_T2U_N9_AD10N_66	66	AR18	IO, 1.8V	Bank66 IO17 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input10 negative.
148	PL_BD18_LVDS66_L3P	IO_L3P_T0L_N4_AD15P_66	66	BD18	IO, 1.8V	Bank66 IO3 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 positive.
150	PL_BE18_LVDS66_L3N	IO_L3N_T0L_N5_AD15N_66	66	BE18	IO, 1.8V	Bank66 IO3 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 negative.
152	PL_BE17_LVDS66_L1P_DBC	IO_L1P_T0L_N0_DBC_66	66	BE17	IO, 1.8V	Bank66 IO1 differential positive or Single ended I/O.
154	PL_BF17_LVDS66_L1N_DBC	IO_L1N_T0L_N1_DBC_66	66	BF17	IO, 1.8V	Bank66 IO1 differential negative or Single ended I/O.
156	PL_AR17_LVDS66_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_66	66	AR17	IO, 1.8V	Bank66 IO16 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input3 positive.
158	PL_AT17_LVDS66_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_66	66	AT17	IO, 1.8V	Bank66 IO16 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input3 negative.
160	PL_BF18_LVDS66_L2N	IO_L2N_T0L_N3_66	66	BF18	IO, 1.8V	Bank66 IO2 differential negative or Single ended I/O.
162	PL_BF19_LVDS66_L2P	IO_L2P_T0L_N2_66	66	BF19	IO, 1.8V	Bank66 IO2 differential positive or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
164	PL_AT18_LVDS66_L15P	IO_L15P_T2L_N4_AD11P_66	66	AT18	IO, 1.8V	Bank66 IO15 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input11 positive.
166	PL_AU17_LVDS66_L15N	IO_L15N_T2L_N5_AD11N_66	66	AU17	IO, 1.8V	Bank66 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
170	PL_AV19_LVDS66_L12P_GC	IO_L12P_T1U_N10_GC_66	66	AV19	IO, 1.8V	Bank66 IO12 differential positive or Single ended I/O Same pin can be configured as GC Global Clock Input differential positive.
172	PL_AW19_LVDS66_L12N_GC	IO_L12N_T1U_N11_GC_66	66	AW19	IO, 1.8V	Bank66 IO12 differential negative or Single ended I/O Same pin can be configured as GC Global Clock Input differential negative.
176	PL_AV18_LVDS66_L11P_GC	IO_L11P_T1U_N8_GC_66	66	AV18	IO, 1.8V	Bank66 IO11 differential positive or Single ended I/O Same pin can be configured as GC Global Clock Input differential positive.
178	PL_AW18_LVDS66_L11N_GC	IO_L11N_T1U_N9_GC_66	66	AW18	IO, 1.8V	Bank66 IO11 differential negative or Single ended I/O Same pin can be configured as GC Global Clock Input differential negative.
182	PL_AY17_LVDS66_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_66	66	AY17	IO, 1.8V	Bank66 IO7 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 positive.
184	PL_BA17_LVDS66_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_66	66	BA17	IO, 1.8V	Bank66 IO7 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 negative.

**IO Type of IOs originating from VU13P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx VU13P FPGA datasheet.*

2.9.2.3 FPGA IOs –HP BANK67

The Virtex UltraScale+ FPGA SOM supports 22 LVDS IOs/44 Single Ended (SE) IOs on Board-to-Board Connector2 from FPGA High Performance (HP) Bank67. Upon these 22 LVDS IOs/44 SE IOs, up to 4 GC Global Clock Inputs and up to 15 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank67 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. By default, IO voltage of Bank67 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Virtex UltraScale+ FPGA datasheet. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for Bank67.

In the Virtex UltraScale+ FPGA SOM, Bank67 signals are routed as LVDS IOs to Board-to-Board Connector2. Even though Bank67 signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

For more details on HP Bank67 pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
75	PL_AV16_LVDS67_L18N	IO_L18N_T2U_N11_AD2N_67	67	AV16	IO, 1.8V	Bank67 IO18 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input2 negative.
77	PL_AU16_LVDS67_L18P	IO_L18P_T2U_N10_AD2P_67	67	AU16	IO, 1.8V	Bank67 IO18 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input2 positive.
83	PL_AR13_LVDS67_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_67	67	AR13	IO, 1.8V	Bank67 IO22 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input0 negative.
85	PL_AP13_LVDS67_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_67	67	AP13	IO, 1.8V	Bank67 IO22 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input0 positive.
87	PL_AR16_LVDS67_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_67	67	AR16	IO, 1.8V	Bank67 IO19 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input9 positive.
89	PL_AR15_LVDS67_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_67	67	AR15	IO, 1.8V	Bank67 IO19 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input9 negative.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
91	PL_AL15_LVDS67_L23P	IO_L23P_T3U_N8_67	67	AL15	IO, 1.8V	Bank67 IO23 differential positive or Single ended I/O.
93	PL_AM15_LVDS67_L23N	IO_L23N_T3U_N9_67	67	AM15	IO, 1.8V	Bank67 IO23 differential negative or Single ended I/O.
95	PL_BD13_LVDS67_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_67	67	BD13	IO, 1.8V	Bank67 IO4 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 positive.
97	PL_BE13_LVDS67_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_67	67	BE13	IO, 1.8V	Bank67 IO4 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input7 negative.
99	PL_AN14_LVDS67_L21P	IO_L21P_T3L_N4_AD8P_67	67	AN14	IO, 1.8V	Bank67 IO21 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input8 positive.
101	PL_AN13_LVDS67_L21N	IO_L21N_T3L_N5_AD8N_67	67	AN13	IO, 1.8V	Bank67 IO21 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input8 negative.
103	PL_AP15_LVDS67_L20P	IO_L20P_T3L_N2_AD1P_67	67	AP15	IO, 1.8V	Bank67 IO20 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input1 positive.
105	PL_AP14_LVDS67_L20N	IO_L20N_T3L_N3_AD1N_67	67	AP14	IO, 1.8V	Bank67 IO20 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input1 negative.
109	PL_AW16_LVDS67_L14P_GC	IO_L14P_T2L_N2_GC_67	67	AW16	IO, 1.8V	Bank67 IO14 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock differential positive.
111	PL_AW15_LVDS67_L14N_GC	IO_L14N_T2L_N3_GC_67	67	AW15	IO, 1.8V	Bank67 IO14 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock differential negative.
115	PL_AY13_LVDS67_L12P_GC	IO_L12P_T1U_N10_GC_67	67	AY13	IO, 1.8V	Bank67 IO12 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock differential positive.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
117	PL_BA13_LVDS67_L12N_GC	IO_L12N_T1U_N11_GC_67	67	BA13	IO, 1.8V	Bank67 IO12 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock differential negative.
121	PL_AY15_LVDS67_L9N	IO_L9N_T1L_N5_AD12N_67	67	AY15	IO, 1.8V	Bank67 IO9 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 negative.
123	PL_AY16_LVDS67_L9P	IO_L9P_T1L_N4_AD12P_67	67	AY16	IO, 1.8V	Bank67 IO9 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input12 positive.
125	PL_BE16_LVDS67_L3N	IO_L3N_T0L_N5_AD15N_67	67	BE16	IO, 1.8V	Bank67 IO3 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 negative.
127	PL_BD16_LVDS67_L3P	IO_L3P_T0L_N4_AD15P_67	67	BD16	IO, 1.8V	Bank67 IO3 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input15 positive.
139	PL_BD15_LVDS67_L5P	IO_L5P_T0U_N8_AD14P_67	67	BD15	IO, 1.8V	Bank67 IO5 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input14 positive.
141	PL_BD14_LVDS67_L5N	IO_L5N_T0U_N9_AD14N_67	67	BD14	IO, 1.8V	Bank67 IO5 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input14 negative.
143	PL_BF15_LVDS67_L2N	IO_L2N_T0L_N3_67	67	BF15	IO, 1.8V	PL Bank67 IO2 differential negative or Single ended I/O.
145	PL_BE15_LVDS67_L2P	IO_L2P_T0L_N2_67	67	BE15	IO, 1.8V	Bank67 IO2 differential positive or Single ended I/O.
80	PL_AY11_LVDS67_L8N	IO_L8N_T1L_N3_AD5N_67	67	AY11	IO, 1.8V	Bank67 IO8 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input5 negative.
82	PL_AY12_LVDS67_L8P	IO_L8P_T1L_N2_AD5P_67	67	AY12	IO, 1.8V	Bank67 IO8 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input5 positive.
84	PL_BF13_LVDS67_L1N	IO_L1N_T0L_N1_DBC_67	67	BF13	IO, 1.8V	Bank67 IO1 differential negative or Single ended I/O.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
86	PL_BF14_LVDS67_L1P	IO_L1P_T0L_N0_DBC_67	67	BF14	IO, 1.8V	Bank67 IO1 differential positive or Single ended I/O.
88	PL_BC14_LVDS67_L6P	IO_L6P_T0U_N10_AD6P_67	67	BC14	IO, 1.8V	Bank67 IO6 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 positive.
90	PL_BC13_LVDS67_L6N	IO_L6N_T0U_N11_AD6N_67	67	BC13	IO, 1.8V	Bank67 IO6 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input6 negative.
92	PL_AU13_LVDS67_L15P	IO_L15P_T2L_N4_AD11P_67	67	AU13	IO, 1.8V	Bank67 IO15 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input11 positive.
94	PL_AV13_LVDS67_L15N	IO_L15N_T2L_N5_AD11N_67	67	AV13	IO, 1.8V	Bank67 IO15 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input11 negative.
96	PL_AV14_LVDS67_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_67	67	AV14	IO, 1.8V	Bank67 IO16 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input3 negative.
98	PL_AU14_LVDS67_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_67	67	AU14	IO, 1.8V	Bank67 IO16 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input3 positive.
100	PL_BB15_LVDS67_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_67	67	BB15	IO, 1.8V	Bank67 IO10 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input4 positive.
102	PL_BB14_LVDS67_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_67	67	BB14	IO, 1.8V	Bank67 IO10 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input4 negative.
104	PL_BA12_LVDS67_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_67	67	BA12	IO, 1.8V	Bank67 IO7 differential positive or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 positive.
106	PL_BB12_LVDS67_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_67	67	BB12	IO, 1.8V	Bank67 IO7 differential negative or Single ended I/O. Same pin can be configured as PLSYSMON differential analog input13 negative.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination*	Description
110	PL_AW14_LVDS67_L13P_GC	IO_L13P_T2L_N0_GC_QBC_67	67	AW14	IO, 1.8V	Bank67 IO13 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock differential positive.
112	PL_AW13_LVDS67_L13N_GC	IO_L13N_T2L_N1_GC_QBC_67	67	AW13	IO, 1.8V	Bank67 IO13 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock differential negative.
116	PL_BA15_LVDS67_L11P_GC	IO_L11P_T1U_N8_GC_67	67	BA15	IO, 1.8V	Bank67 IO11 differential positive or Single ended I/O. Same pin can be configured as GC Global Clock differential positive.
118	PL_BA14_LVDS67_L11N_GC	IO_L11N_T1U_N9_GC_67	67	BA14	IO, 1.8V	Bank67 IO11 differential negative or Single ended I/O. Same pin can be configured as GC Global Clock differential negative.

**IO Type of IOs originating from VU13P FPGA is configurable. Hence for exact IO type configuration options, refer Xilinx VU13P FPGA datasheet.*

2.9.3 Power

The Virtex UltraScale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (pin232) in Board-to-Board Connector1. Also, in Board-to-Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Virtex UltraScale+ FPGA SOM supports VRTC_3V0 coin cell power input from Board-to-Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,14, 15, 16, 17, 18, 19, 20	VCC_5V	NA	NA	NA	I, 5V Power	Supply Voltage.
21, 23, 37, 43, 49, 55, 73, 107, 113, 119, 129, 167, 173, 179, 185, 191, 197, 203, 209, 215, 221, 227, 233, 239, 22, 24, 30, 74, 108, 114, 120, 130, 168, 174, 180, 186, 192, 198, 204, 210, 216, 222, 228, 234, 240	GND	NA	NA	NA	Power	Ground.
68	VRTC_3V0	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.

2.10 Board to Board Connector3

The Virtex UltraScale+ FPGA SOM Board to Board connector3 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector3 are explained in the following sections. The Board-to-Board Connector3 (J5) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A from Samtech

Staking Height - 5mm

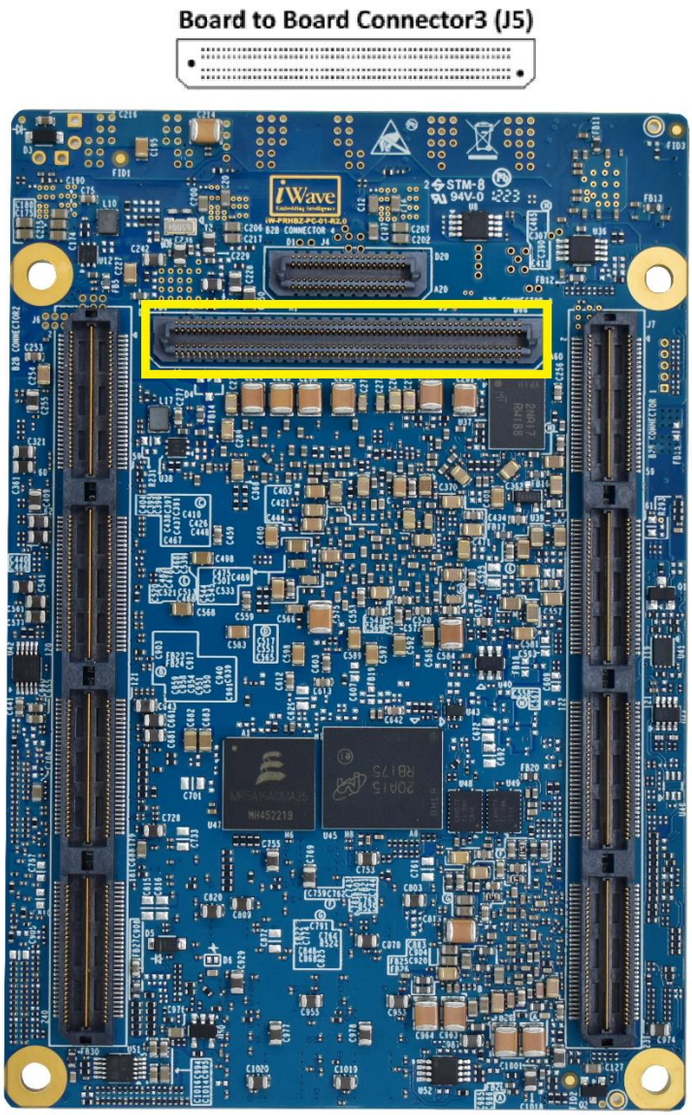


Figure 7: Board to Board Connector3

Table 5: Board to Board Connector3 Pinout

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A1	GTREFCLK1N_232	**B1**	GND	**C1**	NC	**D1**	GND
A2	GTREFCLK1P_232	**B2**	GTYRXN2_230	**C2**	GND	**D2**	B2B_GTREFCLK0P_227
A3	GND	**B3**	GTYRXP2_230	**C3**	GND	**D3**	B2B_GTREFCLK0N_227
A4	GTYRXN0_230	**B4**	GND	**C4**	GTYRXP2_231	**D4**	GND
A5	GTYRXP0_230	**B5**	GND	**C5**	GTYRXN2_231	**D5**	GND
A6	GND	**B6**	GTYRXN3_230	**C6**	GND	**D6**	B2B_GTYRXP3_227
A7	GND	**B7**	GTYRXP3_230	**C7**	GND	**D7**	B2B_GTYRXN3_227
A8	GTYRXN1_230	**B8**	GND	**C8**	GTYRXN0_231	**D8**	GND
A9	GTYRXP1_230	**B9**	GND	**C9**	GTYRXP0_231	**D9**	GND
A10	GND	**B10**	GTYTXN1_230	**C10**	GND	**D10**	GTYRXP2_227
A11	GND	**B11**	GTYTXP1_230	**C11**	GND	**D11**	GTYRXN2_227
A12	GTYTXN3_230	**B12**	GND	**C12**	GTYTXN1_231	**D12**	GND
A13	GTYTXP3_230	**B13**	GND	**C13**	GTYTXP1_231	**D13**	GND
A14	GND	**B14**	GTYTXN0_230	**C14**	GND	**D14**	GTYRXP1_227
A15	GND	**B15**	GTYTXP0_230	**C15**	GND	**D15**	GTYRXN1_227
A16	GTYTXN2_230	**B16**	GND	**C16**	GTREFCLK1N_231	**D16**	GND
A17	GTYTXP2_230	**B17**	GND	**C17**	GTREFCLK1P_231	**D17**	GND
A18	GND	**B18**	GTREFCLK0N_230	**C18**	GND	**D18**	GTYRXP0_227
A19	GND	**B19**	GTREFCLK0P_230	**C19**	GND	**D19**	GTYRXN0_227
A20	GTREFCLK1N_230	**B20**	GND	**C20**	GTREFCLK0P_231	**D20**	GND
A21	GTREFCLK1P_230	**B21**	GND	**C21**	GTREFCLK0N_231	**D21**	GND
A22	GND	**B22**	GTYRXN3_229	**C22**	GND	**D22**	B2B_GTYTXN3_227
A23	GND	**B23**	GTYRXP3_229	**C23**	GND	**D23**	B2B_GTYTXP3_227
A24	GTYRXN2_229	**B24**	GND	**C24**	GTYRXN3_231	**D24**	GND

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A25	GTYRXP2_229	**B25**	GND	**C25**	GTYRXP3_231	**D25**	GND
A26	GND	**B26**	GTYTXP3_229	**C26**	GND	**D26**	GTYTXN2_227
A27	GND	**B27**	GTYTXN3_229	**C27**	GND	**D27**	GTYTXP2_227
A28	GTYTXP2_229	**B28**	GND	**C28**	GTYRXN1_231	**D28**	GND
A29	GTYTXN2_229	**B29**	GND	**C29**	GTYRXP1_231	**D29**	GND
A30	GND	**B30**	GTYTXP1_229	**C30**	GND	**D30**	GTYTXN1_227
A31	GND	**B31**	GTYTXN1_229	**C31**	GND	**D31**	GTYTXP1_227
A32	GTYTXP0_229	**B32**	GND	**C32**	GTYTXN3_231	**D32**	GND
A33	GTYTXN0_229	**B33**	GND	**C33**	GTYTXP3_231	**D33**	GND
A34	GND	**B34**	GTREFCLK1P_229	**C34**	GND	**D34**	GTYTXN0_227
A35	GND	**B35**	GTREFCLK1N_229	**C35**	GND	**D35**	GTYTXP0_227
A36	GTYRXP1_229	**B36**	GND	**C36**	GTYTXN2_231	**D36**	GND
A37	GTYRXN1_229	**B37**	GND	**C37**	GTYTXP2_231	**D37**	GND
A38	GND	**B38**	GTREFCLK0P_229	**C38**	GND	**D38**	GTREFCLK1N_227
A39	GND	**B39**	GTREFCLK0N_229	**C39**	GND	**D39**	GTREFCLK1P_227
A40	GTYRXP0_229	**B40**	GND	**C40**	GTYTXN0_231	**D40**	GND
A41	GTYRXN0_229	**B41**	GND	**C41**	GTYTXP0_231	**D41**	GND
A42	GND	**B42**	GTREFCLK0P_129	**C42**	GND	**D42**	GTYRXN1_232
A43	GND	**B43**	GTREFCLK0N_129	**C43**	GND	**D43**	GTYRXP1_232
A44	GTYTXP0_129	**B44**	GND	**C44**	GTYRXN2_232	**D44**	GND
A45	GTYTXN0_129	**B45**	GND	**C45**	GTYRXP2_232	**D45**	GND
A46	GND	**B46**	GTYTXP1_129	**C46**	GND	**D46**	GTYRXN3_232
A47	GND	**B47**	GTYTXN1_129	**C47**	GND	**D47**	GTYRXP3_232
A48	GTYTXP3_129	**B48**	GND	**C48**	GTREFCLK0P_232	**D48**	GND
A49	GTYTXN3_129	**B49**	GND	**C49**	GTREFCLK0N_232	**D49**	GND

B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name	B2B-3 Pin No	Signal Name
A50	GND	**B50**	GTYRXP0_129	**C50**	GND	**D50**	GTYRXN0_232
A51	GND	**B51**	GTYRXN0_129	**C51**	GND	**D51**	GTYRXP0_232
A52	GTYTXP2_129	**B52**	GND	**C52**	GTYTXP0_232	**D52**	GND
A53	GTYTXN2_129	**B53**	GND	**C53**	GTYTXN0_232	**D53**	GND
A54	GND	**B54**	GTYRXP2_129	**C54**	GND	**D54**	GTYTXP2_232
A55	GND	**B55**	GTYRXN2_129	**C55**	GND	**D55**	GTYTXN2_232
A56	GTYRXP1_129	**B56**	GND	**C56**	GTYTXN1_232	**D56**	GND
A57	GTYRXN1_129	**B57**	GND	**C57**	GTYTXP1_232	**D57**	GND
A58	GND	**B58**	GTYRXP3_129	**C58**	GND	**D58**	GTYTXP3_232
A59	GTREFCLK1N_129	**B59**	GTYRXN3_129	**C59**	GND	**D59**	GTYTXN3_232
A60	GTREFCLK1P_129	**B60**	GND	**C60**	NC	**D60**	GND

2.10.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector3 from Virtex UltraScale+ FPGA is explained in the following section.

2.10.1.1 GTY High Speed Transceivers

The Virtex UltraScale+ FPGA supports 24 GTY transceivers through six transceiver Quad with line rate from 500Mbps to 32.75Gbps based on the speed grade of the FPGA. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

In Virtex UltraScale+ FPGA SOM, on board reference clock to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required peripheral standards on GTY transceivers. Also, on board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommend.

For more details on GTY transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
Bank227 Transceiver Quad Pins						
D2	B2B_GTREFCLK0P_227*	MGTREFCLK0P_227	227	AH11	I, DIFF	GTY Bank227 channel0 High speed differential reference clock0 positive.
D3	B2B_GTREFCLK0N_227*	MGTREFCLK0N_227	227	AH10	I, DIFF	GTY Bank227 channel0 High speed differential reference clock0 negative.
D6	B2B_GTYRXP3_227*	MGTYRXP3_227	227	AF2	I, DIFF	GTY Bank227 channel3 High speed differential receiver positive.
D7	B2B_GTYRXN3_227*	MGTYRXN3_227	227	AF1	I, DIFF	GTY Bank227 channel3 High speed differential receiver negative.
D10	GTYRXP2_227	MGTYRXP2_227	227	AG4	I, DIFF	GTY Bank227 channel2 High speed differential receiver positive.
D11	GTYRXN2_227	MGTYRXN2_227	227	AG3	I, DIFF	GTY Bank227 channel2 High speed differential receiver negative.
D14	GTYRXP1_227	MGTYRXP1_227	227	AH2	I, DIFF	GTY Bank227 channel1 High speed differential receiver positive.
D15	GTYRXN1_227	MGTYRXN1_227	227	AH1	I, DIFF	GTY Bank227 channel1 High speed differential receiver negative.
D18	GTYRXP0_227	MGTYRXP0_227	227	AJ4	I, DIFF	GTY Bank227 channel0 High speed differential receiver positive.
D19	GTYRXN0_227	MGTYRXN0_227	227	AJ3	I, DIFF	GTY Bank227 channel0 High speed differential receiver negative.
D22	B2B_GTYTXN3_227*	MGTYTXN3_227	227	AF6	O, DIFF	GTY Bank227 channel3 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
D23	B2B_GTYTXP3_227*	MGTYTXP3_227	227	AF7	O, DIFF	GTY Bank227 channel3 High speed differential transmitter positive.
D26	GTYTXN2_227	MGTYTXN2_227	227	AG8	O, DIFF	GTY Bank227 channel2 High speed differential transmitter negative.
D27	GTYTXP2_227	MGTYTXP2_227	227	AG9	O, DIFF	GTY Bank227 channel2 High speed differential transmitter positive.
D30	GTYTXN1_227	MGTYTXN1_227	227	AH6	O, DIFF	GTY Bank227 channel1 High speed differential transmitter negative.
D31	GTYTXP1_227	MGTYTXP1_227	227	AH7	O, DIFF	GTY Bank227 channel1 High speed differential transmitter positive.
D34	GTYTXN0_227	MGTYTXN0_227	227	AJ8	O, DIFF	GTY Bank227 channel0 High speed differential transmitter negative.
D35	GTYTXP0_227	MGTYTXP0_227	227	AJ9	O, DIFF	GTY Bank227 channel0 High speed differential transmitter positive.
D38	GTREFCLK1N_227	MGTREFCLK1N_227	227	AF10	I, DIFF	GTY Bank227 channel1 High speed differential reference clock1 negative.
D39	GTREFCLK1P_227	MGTREFCLK1P_227	227	AF11	I, DIFF	GTY Bank227 channel1 High speed differential reference clock1 positive.
Bank229 Transceiver Quad Pins						
A24	GTYRXN2_229	MGTYRXN2_229	229	W3	I, DIFF	GTY Bank229 channel2 High speed differential receiver negative.
A25	GTYRXP2_229	MGTYRXP2_229	229	W4	I, DIFF	GTY Bank229 channel2 High speed differential receiver positive.
A28	GTYTXP2_229	MGTYTXP2_229	229	W9	O, DIFF	GTY Bank229 channel2 High speed differential transmitter positive.
A29	GTYTXN2_229	MGTYTXN2_229	229	W8	O, DIFF	GTY Bank229 channel2 High speed differential transmitter negative.
A32	GTYTXP0_229	MGTYTXP0_229	229	AA9	O, DIFF	GTY Bank229 channel0 High speed differential transmitter positive.
A33	GTYTXN0_229	MGTYTXN0_229	229	AA8	O, DIFF	GTY Bank229 channel0 High speed differential transmitter negative.
A36	GTYRXP1_229	MGTYRXP1_229	229	Y2	I, DIFF	GTY Bank229 channel1 High speed differential receiver positive.
A37	GTYRXN1_229	MGTYRXN1_229	229	Y1	I, DIFF	GTY Bank229 channel1 High speed differential receiver negative.
A40	GTYRXP0_229	MGTYRXP0_229	229	AA4	I, DIFF	GTY Bank229 channel0 High speed differential receiver positive.
A41	GTYRXN0_229	MGTYRXN0_229	229	AA3	I, DIFF	GTY Bank229 channel0 High speed differential receiver negative.
B22	GTYRXN3_229	MGTYRXN3_229	229	V1	I, DIFF	GTY Bank229 channel3 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
B23	GTYRXP3_229	MGTYRXP3_229	229	V2	I, DIFF	GTY Bank229 channel3 High speed differential receiver positive.
B26	GTYTXP3_229	MGTYTXP3_229	229	V7	O, DIFF	GTY Bank229 channel3 High speed differential transmitter positive.
B27	GTYTXN3_229	MGTYTXN3_229	229	V6	O, DIFF	GTY Bank229 channel3 High speed differential transmitter negative.
B30	GTYTXP1_229	MGTYTXP1_229	229	Y7	O, DIFF	GTY Bank229 channel1 High speed differential transmitter positive.
B31	GTYTXN1_229	MGTYTXN1_229	229	Y6	O, DIFF	GTY Bank229 channel1 High speed differential transmitter negative.
B34	GTREFCLK1P_229	MGTREFCLK1P_229	229	V11	I, DIFF	GTY Bank229 channel1 High speed differential reference clock1 positive.
B35	GTREFCLK1N_229	MGTREFCLK1N_229	229	V10	I, DIFF	GTY Bank229 channel1 High speed differential reference clock1 negative.
B38	GTREFCLK0P_229	MGTREFCLK0P_229	229	Y11	I, DIFF	GTY Bank229 channel0 High speed differential reference clock0 positive.
B39	GTREFCLK0N_229	MGTREFCLK0N_229	229	Y10	I, DIFF	GTY Bank229 channel0 High speed differential reference clock0 negative.
Bank230 Transceiver Quad Pins						
A4	GTYRXN0_230	MGTYRXN0_230	230	U3	I, DIFF	GTY Bank230 channel0 High speed differential receiver negative.
A5	GTYRXP0_230	MGTYRXP0_230	230	U4	I, DIFF	GTY Bank230 channel0 High speed differential receiver positive.
A8	GTYRXN1_230	MGTYRXN1_230	230	T1	I, DIFF	GTY Bank230 channel1 High speed differential receiver negative.
A9	GTYRXP1_230	MGTYRXP1_230	230	T2	I, DIFF	GTY Bank230 channel1 High speed differential receiver positive.
A12	GTYTXN3_230	MGTYTXN3_230	230	P6	O, DIFF	GTY Bank230 channel3 High speed differential transmitter negative.
A13	GTYTXP3_230	MGTYTXP3_230	230	P7	O, DIFF	GTY Bank230 channel3 High speed differential transmitter positive.
A16	GTYTXN2_230	MGTYTXN2_230	230	R8	O, DIFF	GTY Bank230 channel2 High speed differential transmitter negative.
A17	GTYTXP2_230	MGTYTXP2_230	230	R9	O, DIFF	GTY Bank230 channel2 High speed differential transmitter positive.
A20	GTREFCLK1N_230	MGTREFCLK1N_230	230	P10	I, DIFF	GTY Bank230 channel1 High speed differential reference clock1 negative.
A21	GTREFCLK1P_230	MGTREFCLK1P_230	230	P11	I, DIFF	GTY Bank230 channel1 High speed differential reference clock1 positive.
B2	GTYRXN2_230	MGTYRXN2_230	230	R3	I, DIFF	GTY Bank230 channel2 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
B3	GTYRXP2_230	MGTYRXP2_230	230	R4	I, DIFF	GTY Bank230 channel2 High speed differential receiver positive.
B6	GTYRXN3_230	MGTYRXN3_230	230	P1	I, DIFF	GTY Bank230 channel3 High speed differential receiver negative.
B7	GTYRXP3_230	MGTYRXP3_230	230	P2	I, DIFF	GTY Bank230 channel3 High speed differential receiver positive.
B10	GTYTXN1_230	MGTYTXN1_230	230	T6	O, DIFF	GTY Bank230 channel1 High speed differential transmitter negative.
B11	GTYTXP1_230	MGTYTXP1_230	230	T7	O, DIFF	GTY Bank230 channel1 High speed differential transmitter positive.
B14	GTYTXN0_230	MGTYTXN0_230	230	U8	O, DIFF	GTY Bank230 channel0 High speed differential transmitter negative.
B15	GTYTXP0_230	MGTYTXP0_230	230	U9	O, DIFF	GTY Bank230 channel0 High speed differential transmitter positive.
B18	GTREFCLK0N_230	MGTREFCLK0N_230	230	T10	I, DIFF	GTY Bank230 channel0 High speed differential reference clock0 negative.
B19	GTREFCLK0P_230	MGTREFCLK0P_230	230	T11	I, DIFF	GTY Bank230 channel0 High speed differential reference clock0 positive.
Bank231 Transceiver Quad Pins						
C4	GTYRXP2_231	MGTYRXP2_231	231	L4	I, DIFF	GTY Bank231 channel2 High speed differential receiver positive.
C5	GTYRXN2_231	MGTYRXN2_231	231	L3	I, DIFF	GTY Bank231 channel2 High speed differential receiver negative.
C8	GTYRXN0_231	MGTYRXN0_231	231	N3	I, DIFF	GTY Bank231 channel0 High speed differential receiver negative.
C9	GTYRXP0_231	MGTYRXP0_231	231	N4	I, DIFF	GTY Bank231 channel0 High speed differential receiver positive.
C12	GTYTXN1_231	MGTYTXN1_231	231	M6	O, DIFF	GTY Bank231 channel1 High speed differential transmitter negative.
C13	GTYTXP1_231	MGTYTXP1_231	231	M7	O, DIFF	GTY Bank231 channel1 High speed differential transmitter positive.
C16	GTREFCLK1N_231	MGTREFCLK1N_231	231	K10	I, DIFF	GTY Bank231 channel1 High speed differential reference clock1 negative.
C17	GTREFCLK1P_231	MGTREFCLK1P_231	231	K11	I, DIFF	GTY Bank231 channel1 High speed differential reference clock1 positive.
C20	GTREFCLK0P_231	MGTREFCLK0P_231	231	M11	I, DIFF	GTY Bank231 channel0 High speed differential reference clock0 positive.
C21	GTREFCLK0N_231	MGTREFCLK0N_231	231	M10	I, DIFF	GTY Bank231 channel0 High speed differential reference clock0 negative.
C24	GTYRXN3_231	MGTYRXN3_231	231	K1	I, DIFF	GTY Bank231 channel3 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
C25	GTYRXP3_231	MGTYRXP3_231	231	K2	I, DIFF	GTY Bank231 channel3 High speed differential receiver positive.
C28	GTYRXN1_231	MGTYRXN1_231	231	M1	I, DIFF	GTY Bank231 channel1 High speed differential receiver negative.
C29	GTYRXP1_231	MGTYRXP1_231	231	M2	I, DIFF	GTY Bank231 channel1 High speed differential receiver positive.
C32	GTYTXN3_231	MGTYTXN3_231	231	K6	O, DIFF	GTY Bank231 channel3 High speed differential transmitter negative.
C33	GTYTXP3_231	MGTYTXP3_231	231	K7	O, DIFF	GTY Bank231 channel3 High speed differential transmitter positive.
C36	GTYTXN2_231	MGTYTXN2_231	231	L8	O, DIFF	GTY Bank231 channel2 High speed differential transmitter negative.
C37	GTYTXP2_231	MGTYTXP2_231	231	L9	O, DIFF	GTY Bank231 channel2 High speed differential transmitter positive.
C40	GTYTXN0_231	MGTYTXN0_231	231	N8	O, DIFF	GTY Bank231 channel0 High speed differential transmitter negative.
C41	GTYTXP0_231	MGTYTXP0_231	231	N9	O, DIFF	GTY Bank231 channel0 High speed differential transmitter positive.
Bank232 Transceiver Quad Pins						
A1	GTREFCLK1N_232	MGTREFCLK1N_232	232	F10	I, DIFF	GTY Bank232 channel1 High speed differential reference clock1 negative.
A2	GTREFCLK1P_232	MGTREFCLK1P_232	232	F11	I, DIFF	GTY Bank232 channel1 High speed differential reference clock1 positive.
C44	GTYRXN2_232	MGTYRXN2_232	232	G3	I, DIFF	GTY Bank232 channel2 High speed differential receiver negative.
C45	GTYRXP2_232	MGTYRXP2_232	232	G4	I, DIFF	GTY Bank232 channel2 High speed differential receiver positive.
C48	GTREFCLK0P_232	MGTREFCLK0P_232	232	H11	I, DIFF	GTY Bank232 channel0 High speed differential reference clock0 positive.
C49	GTREFCLK0N_232	MGTREFCLK0N_232	232	H10	I, DIFF	GTY Bank232 channel0 High speed differential reference clock0 negative.
C52	GTYTXP0_232	MGTYTXP0_232	232	J9	O, DIFF	GTY Bank232 channel0 High speed differential transmitter positive.
C53	GTYTXN0_232	MGTYTXN0_232	232	J8	O, DIFF	GTY Bank232 channel0 High speed differential transmitter negative.
C56	GTYTXN1_232	MGTYTXN1_232	232	H6	O, DIFF	GTY Bank232 channel1 High speed differential transmitter negative.
C57	GTYTXP1_232	MGTYTXP1_232	232	H7	O, DIFF	GTY Bank232 channel1 High speed differential transmitter positive.
D42	GTYRXN1_232	MGTYRXN1_232	232	H1	I, DIFF	GTY Bank232 channel1 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
D43	GTYRXP1_232	MGTYRXP1_232	232	H2	I, DIFF	GTY Bank232 channel1 High speed differential receiver positive.
D46	GTYRXN3_232	MGTYRXN3_232	232	F1	I, DIFF	GTY Bank232 channel3 High speed differential receiver negative.
D47	GTYRXP3_232	MGTYRXP3_232	232	F2	I, DIFF	GTY Bank232 channel3 High speed differential receiver positive.
D50	GTYRXN0_232	MGTYRXN0_232	232	J3	I, DIFF	GTY Bank232 channel0 High speed differential receiver negative.
D51	GTYRXP0_232	MGTYRXP0_232	232	J4	I, DIFF	GTY Bank232 channel0 High speed differential receiver positive.
D54	GTYTXP2_232	MGTYTXP2_232	232	G9	O, DIFF	GTY Bank232 channel2 High speed differential transmitter positive.
D55	GTYTXN2_232	MGTYTXN2_232	232	G8	O, DIFF	GTY Bank232 channel2 High speed differential transmitter negative.
D58	GTYTXP3_232	MGTYTXP3_232	232	F7	O, DIFF	GTY Bank232 channel3 High speed differential transmitter positive.
D59	GTYTXN3_232	MGTYTXN3_232	232	F6	O, DIFF	GTY Bank232 channel3 High speed differential transmitter negative.
Bank129 Transceiver Quad Pins						
A59	GTREFCLK1N_129	MGTREFCLK1N_129	129	AA37	I, DIFF	GTY Bank129 channel1 High speed differential reference clock1 negative.
A60	GTREFCLK1P_129	MGTREFCLK1P_129	129	AA36	I, DIFF	GTY Bank129 channel1 High speed differential reference clock1 positive.
B55	GTYRXN2_129	MGTYRXN2_129	129	W46	I, DIFF	GTY Bank129 channel2 High speed differential receiver negative.
B54	GTYRXP2_129	MGTYRXP2_129	129	W45	I, DIFF	GTY Bank129 channel2 High speed differential receiver positive.
B42	GTREFCLK0P_129	MGTREFCLK0P_129	129	AC36	I, DIFF	GTY Bank129 channel0 High speed differential reference clock0 positive.
B43	GTREFCLK0N_129	MGTREFCLK0N_129	129	AC37	I, DIFF	GTY Bank129 channel0 High speed differential reference clock0 negative.
A44	GTYTXP0_129	MGTYTXP0_129	129	AA40	O, DIFF	GTY Bank129 channel0 High speed differential transmitter positive.
A45	GTYTXN0_129	MGTYTXN0_129	129	AA41	O, DIFF	GTY Bank129 channel0 High speed differential transmitter negative.
B47	GTYTXN1_129	MGTYTXN1_129	129	Y39	O, DIFF	GTY Bank129 channel1 High speed differential transmitter negative.
B46	GTYTXP1_129	MGTYTXP1_129	129	Y38	O, DIFF	GTY Bank129 channel1 High speed differential transmitter positive.
A57	GTYRXN1_129	MGTYRXN1_129	129	Y44	I, DIFF	GTY Bank129 channel1 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
A56	GTYRXP1_129	MGTYRXP1_129	129	Y43	I, DIFF	GTY Bank129 channel1 High speed differential receiver positive.
B59	GTYRXN3_129	MGTYRXN3_129	129	V44	I, DIFF	GTY Bank129 channel3 High speed differential receiver negative.
B58	GTYRXP3_129	MGTYRXP3_129	129	V43	I, DIFF	GTY Bank129 channel3 High speed differential receiver positive.
B51	GTYRXN0_129	MGTYRXN0_129	129	AA46	I, DIFF	GTY Bank129 channel0 High speed differential receiver negative.
B50	GTYRXP0_129	MGTYRXP0_129	129	AA45	I, DIFF	GTY Bank129 channel0 High speed differential receiver positive.
A52	GTYTXP2_129	MGTYTXP2_129	129	W40	O, DIFF	GTY Bank129 channel2 High speed differential transmitter positive.
A53	GTYTXN2_129	MGTYTXN2_129	129	W41	O, DIFF	GTY Bank129 channel2 High speed differential transmitter negative.
A48	GTYTXP3_129	MGTYTXP3_129	129	V38	O, DIFF	GTY Bank129 channel3 High speed differential transmitter positive.
A49	GTYTXN3_129	MGTYTXN3_129	129	V39	O, DIFF	GTY Bank129 channel3 High speed differential transmitter negative.

Important Note: Optionally, one GTY transceiver channel3 link from Bank 227 is connected to on-SOM PCIe.

2.10.2 Power

The Virtex UltraScale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector3, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
A3, A6, A7, A10, A11, A14, A15, A18, A19, A22, A23, A26, A27, A30, A31, A34, A35, A38, A39, A42, A43, A46, A47, A50, A51, A54, A55, A58, B1, B4, B5, B8, B9, B12, B13, B16, B17, B20, B21, B24, B25, B28, B29, B32, B33, B36, B37, B40, B41, B44, B45, B48, B49, B52, B53, B56, B57, B60, C2, C3, C6, C7, C10, C11, C14, C15, C18, C19, C22, C23, C26, C27, C30, C31, C34, C35, C38, C39, C42, C43, C46, C47, C50, C51, C54, C55, C58, C59, D1, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, D24, D25, D28, D29, D32, D33, D36, D37, D40, D41, D44, D45, D48, D49, D52, D53, D56, D57, D60,	GND	NA	NA	NA	Power	Ground.

2.11 Board to Board Connector4

The Virtex UltraScale+ FPGA SOM Board to Board connector4 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector4 are explained in the following sections. The Board-to-Board Connector4 (J4) is physically located on bottom side of the SOM as shown below.

Number of Pins - 80

Connector Part Number - ADM6-20-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-20-03.5-L-4-2-A from Samtech

Staking Height - 5mm

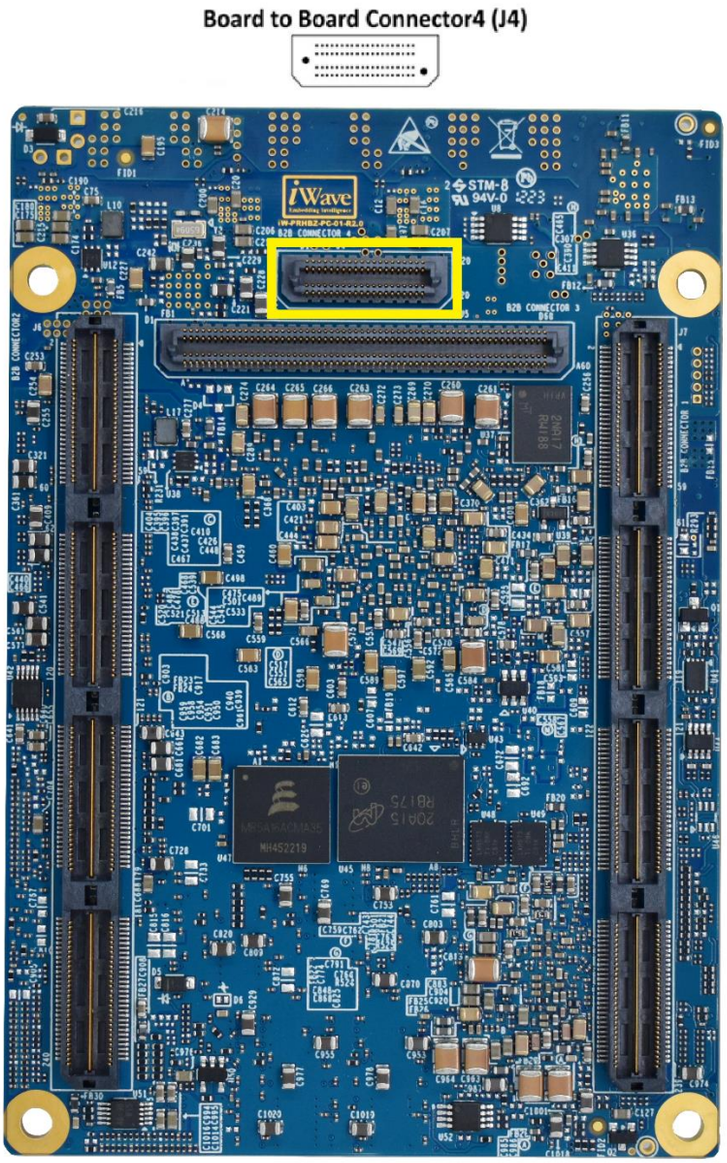


Figure 8: Board to Board Connector4

Table 6: Board to Board Connector4 Pinout

B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name	B2B-4 Pin No	Signal Name
A1	GND	**B1**	GTREFCLK1N_226	**C1**	GND	**D1**	NC
A2	GTYRXN1_226	**B2**	GTREFCLK1P_226	**C2**	GTYTXP0_126	**D2**	GND
A3	GTYRXP1_226	**B3**	GND	**C3**	GTYTXN0_126	**D3**	GND
A4	GND	**B4**	GTYRXN3_226	**C4**	GND	**D4**	GTYTXP1_126
A5	GND	**B5**	GTYRXP3_226	**C5**	GND	**D5**	GTYTXN1_126
A6	GTREFCLK0P_226	**B6**	GND	**C6**	GTYTXP3_126	**D6**	GND
A7	GTREFCLK0N_226	**B7**	GND	**C7**	GTYTXN3_126	**D7**	GND
A8	GND	**B8**	GTYRXN2_226	**C8**	GND	**D8**	GTREFCLK0N_126
A9	GND	**B9**	GTYRXP2_226	**C9**	GND	**D9**	GTREFCLK0P_126
A10	GTYTXP0_226	**B10**	GND	**C10**	GTYTXN2_126	**D10**	GND
A11	GTYTXN0_226	**B11**	GND	**C11**	GTYTXP2_126	**D11**	GND
A12	GND	**B12**	GTYTXP3_226	**C12**	GND	**D12**	GTYRXN1_126
A13	GND	**B13**	GTYTXN3_226	**C13**	GND	**D13**	GTYRXP1_126
A14	GTYTXP1_226	**B14**	GND	**C14**	GTYRXP2_126	**D14**	GND
A15	GTYTXN1_226	**B15**	GND	**C15**	GTYRXN2_126	**D15**	GND
A16	GND	**B16**	GTYRXN0_226	**C16**	GND	**D16**	GTYRXP3_126
A17	GND	**B17**	GTYRXP0_226	**C17**	GND	**D17**	GTYRXN3_126
A18	GTYTXP2_226	**B18**	GND	**C18**	GTYRXN0_126	**D18**	GND
A19	GTYTXN2_226	**B19**	GND	**C19**	GTYRXP0_126	**D19**	GTREFCLK1N_126
A20	GND	**B20**	NC	**C20**	GND	**D20**	GTREFCLK1P_126

2.11.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector4 from Virtex UltraScale+ FPGA's PL is explained in the following section.

2.11.1.1 GTY High Speed Transceivers

The Virtex UltraScale+ FPGA supports 8 GTY transceivers through two transceiver Quad with line rate from 500Mbps to 32.75Gbps based on the speed grade of the FPGA. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

In Virtex UltraScale+ FPGA SOM, on board reference clock to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required peripheral standards on GTY transceivers. Also, on board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommend.

For more details on GTY transceiver pinouts on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector4 Signal Name	FPGA Pin Name	FPGA Pin Name	FPGA Pin Name	Signal Type/ Termination	Description
Bank226 Transceiver Quad Pins						
A2	GTYRXN1_226	MGTYRXN1_226	226	AM1	I, DIFF	GTY Bank226 channel1 High speed differential receiver negative.
A3	GTYRXP1_226	MGTYRXN1_226	226	AH1	I, DIFF	GTY Bank226 channel1 High speed differential receiver positive.
A6	GTREFCLK0P_226	MGTREFCLK0P_226	226	AM11	I, DIFF	GTY Bank226 channel0 High speed differential reference clock0 positive.
A7	GTREFCLK0N_226	MGTREFCLK0N_226	226	AM10	I, DIFF	GTY Bank226 channel0 High speed differential reference clock0 negative.
A10	GTYTXP0_226	MGTYTXP0_226	226	AN9	O, DIFF	GTY Bank226 channel0 High speed differential transmitter positive.
A11	GTYTXN0_226	MGTYTXN0_226	226	AN8	O, DIFF	GTY Bank226 channel0 High speed differential transmitter negative.
A14	GTYTXP1_226	MGTYTXP1_226	226	AM7	O, DIFF	GTY Bank226 channel1 High speed differential transmitter positive.
A15	GTYTXN1_226	MGTYTXN1_226	226	AM6	O, DIFF	GTY Bank226 channel1 High speed differential transmitter negative.
A18	GTYTXP2_226	MGTYTXP2_226	226	AL9	O, DIFF	GTY Bank226 channel2 High speed differential transmitter positive.
A19	GTYTXN2_226	MGTYTXN2_226	226	AL8	O, DIFF	GTY Bank226 channel2 High speed differential transmitter negative.
B1	GTREFCLK1N_226	MGTREFCLK1N_226	226	AK10	I, DIFF	GTY Bank226 channel1 High speed differential reference clock1 negative.

B2B-4 Pin No	B2B Connector4 Signal Name	FPGA Pin Name	FPGA Pin Name	FPGA Pin Name	Signal Type/ Termination	Description
B2	GTREFCLK1P_226	MGTREFCLK1P_226	226	AK11	I, DIFF	GTY Bank226 channel1 High speed differential reference clock1 positive.
B4	GTYRXN3_226	MGTYRXN3_226	226	AK1	I, DIFF	GTY Bank226 channel3 High speed differential receiver negative.
B5	GTYRXP3_226	MGTYRXP3_226	226	AK2	I, DIFF	GTY Bank226 channel3 High speed differential receiver positive.
B8	GTYRXN2_226	MGTYRXN2_226	226	AL3	I, DIFF	GTY Bank226 channel2 High speed differential receiver negative.
B9	GTYRXP2_226	MGTYRXP2_226	226	AL4	O, DIFF	GTY Bank226 channel2 High speed differential receiver positive.
B12	GTYTXP3_226	MGTYTXP3_226	226	AK7	O, DIFF	GTY Bank226 channel3 High speed differential transmitter positive.
B13	GTYTXN3_226	MGTYTXN3_226	226	AK6	O, DIFF	GTY Bank226 channel3 High speed differential transmitter negative.
B16	GTYRXN0_226	MGTYRXN0_226	226	AN3	I, DIFF	GTY Bank226 channel0 High speed differential receiver negative.
B17	GTYRXP0_226	MGTYRXP0_226	226	AN4	I, DIFF	GTY Bank226 channel0 High speed differential receiver positive.
Bank126 Transceiver Quad Pins						
D12	GTYRXN1_126	MGTYRXN1_126	126	AM44	I, DIFF	GTY Bank126 channel1 High speed differential receiver negative.
D13	GTYRXP1_126	MGTYRXP1_126	126	AM43	I, DIFF	GTY Bank126 channel1 High speed differential receiver positive.
D9	GTREFCLK0P_126	MGTREFCLK0P_126	126	AR36	I, DIFF	GTY Bank126 channel0 High speed differential reference clock0 positive.
D8	GTREFCLK0N_126	MGTREFCLK0N_126	126	AR37	I, DIFF	GTY Bank126 channel0 High speed differential reference clock0 negative.
C2	GTYTXP0_126	MGTYTXP0_126	126	AN41	O, DIFF	GTY Bank126 channel0 High speed differential transmitter positive.
C3	GTYTXN0_126	MGTYTXN0_126	126	AN40	O, DIFF	GTY Bank126 channel0 High speed differential transmitter negative.
D4	GTYTXP1_126	MGTYTXP1_126	126	AM38	O, DIFF	GTY Bank126 channel1 High speed differential transmitter positive.
D5	GTYTXN1_126	MGTYTXN1_126	126	AM39	O, DIFF	GTY Bank126 channel1 High speed differential transmitter negative.
C11	GTYTXP2_126	MGTYTXP2_126	126	AL40	O, DIFF	GTY Bank126 channel2 High speed differential transmitter positive.
C10	GTYTXN2_126	MGTYTXN2_126	126	AL41	O, DIFF	GTY Bank126 channel2 High speed differential transmitter negative.
D19	GTREFCLK1N_126	MGTREFCLK1N_126	126	AN37	I, DIFF	GTY Bank126 channel1 High speed differential reference clock1 negative.

B2B-4 Pin No	B2B Connector4 Signal Name	FPGA Pin Name	FPGA Pin Name	FPGA Pin Name	Signal Type/ Termination	Description
D20	GTREFCLK1P_126	MGTREFCLK1P_126	126	AN36	I, DIFF	GTY Bank126 channel1 High speed differential reference clock1 positive.
D17	GTYRXN3_126	MGTYRXN3_126	126	AK44	I, DIFF	GTY Bank126 channel3 High speed differential receiver negative.
D16	GTYRXP3_126	MGTYRXP3_126	126	AK43	I, DIFF	GTY Bank126 channel3 High speed differential receiver positive.
C15	GTYRXN2_126	MGTYRXN2_126	126	AL46	I, DIFF	GTY Bank126 channel2 High speed differential receiver negative.
C14	GTYRXP2_126	MGTYRXP2_126	126	AL45	O, DIFF	GTY Bank126 channel2 High speed differential receiver positive.
C6	GTYTXP3_126	MGTYTXP3_126	126	AK38	O, DIFF	GTY Bank126 channel3 High speed differential transmitter positive.
C7	GTYTXN3_126	MGTYTXN3_126	126	AK39	O, DIFF	GTY Bank126 channel3 High speed differential transmitter negative.
C18	GTYRXN0_126	MGTYRXN0_126	126	AN46	I, DIFF	GTY Bank126 channel0 High speed differential receiver negative.
C19	GTYRXP0_126	MGTYRXP0_126	126	AN45	I, DIFF	GTY Bank126 channel0 High speed differential receiver positive.

2.11.2 Power

The Virtex UltraScale+ FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector4, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector4 Pin Name	FPGA Pin Name	FPGA Pin Name	FPGA Pin Name	Signal Type/ Termination	Description
A1, A4, A5, A8, A9, A12, A13, A16, A17, A20, B3, B6, B7, B10, B11, B14, B15, B18, B19, C1, C4, C5, C8, C9, C12, C13, C16, C17, C20, D2, D3, D6, D7, D10, D11, D14, D15, D18,	GND	NA	NA	NA	Power	Ground.

2.12 LS1021A Processor Pin Multiplexing on Board-to-Board Connectors

The Virtex UltraScale+ FPGA SOM's LS1021A Processor IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of IO pins can be configured as GPIO if required. The below table provides the details of LS1021A processor's pin connections on Virtex UltraScale+ FPGA SOM with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring LS1021A Datasheet and Reference manual. To know the complete available alternate functions, refer the LS1021A Reference manual.

Table 7: LS1021A IOMUX on Virtex UltraScale+ FPGA SOM

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
Integrated Flash Controller	NA	IFC_A16/QSPI_CS_A0	IFC_A16	QSPI_CS_A0						
	NA	IFC_A17/QSPI_CS_A1	IFC_A17	QSPI_CS_A1						
	NA	IFC_A18/QSPI_CK_A	IFC_A18	QSPI_CK_A						
	NA	IFC_A19/QSPI_CS_B0	IFC_A19	QSPI_CS_B0						
	NA	IFC_A20/QSPI_CS_B1	IFC_A20	QSPI_CS_B1						
	NA	IFC_A21/QSPI_CK_B/cfg_dram_type	IFC_A21	QSPI_CK_B	cfg_dram_type					
	NA	IFC_A22/QSPI_DIO_A0/IFC_WP1_B	IFC_A22	QSPI_DIO_A0		IFC_WP1_B				
	NA	IFC_A23/QSPI_DIO_A1/IFC_WP2_B	IFC_A23	QSPI_DIO_A1		IFC_WP2_B				
	NA	IFC_A24/QSPI_DIO_A2/IFC_WP3_B	IFC_A24	QSPI_DIO_A2		IFC_WP3_B				
	NA	IFC_A25/GPIO2_25/QSPI_DIO_A3/FTM5_CH0/IFC_RB2_B/IFC_CS4_B	IFC_A25	GPIO2_25	QSPI_DIO_A3	IFC_RB2_B	IFC_CS4_B	FTM5_CH0		
	NA	IFC_A26/GPIO2_26/FTM5_CH1/IFC_RB3_B/IFC_CS5_B	IFC_A26	GPIO2_26		IFC_RB3_B	IFC_CS5_B	FTM5_CH1		
	NA	IFC_A27/GPIO2_27/FTM5_EXTCLK/IFC_CS6_B	IFC_A27	GPIO2_27			IFC_CS6_B	FTM5_EXTCLK		
	NA	IFC_AD00/cfg_gpinput0	IFC_AD00		cfg_gpinput0					
	NA	IFC_AD01/cfg_gpinput1	IFC_AD01		cfg_gpinput1					
	NA	IFC_AD02/cfg_gpinput2	IFC_AD02		cfg_gpinput2					
	NA	IFC_AD03/cfg_gpinput3	IFC_AD03		cfg_gpinput3					
	NA	IFC_AD04/cfg_gpinput4	IFC_AD04		cfg_gpinput4					

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	IFC_AD05/cfg_gpinput5	IFC_AD05		cfg_gpinput5					
	NA	IFC_AD06/cfg_gpinput6	IFC_AD06		cfg_gpinput6					
	NA	IFC_AD07/cfg_gpinput7	IFC_AD07		cfg_gpinput7					
	NA	IFC_AD08/cfg_rcw_src0/SPI1_PCS1	IFC_AD08	SPI1_PCS1	cfg_rcw_src0					
	NA	IFC_AD09/cfg_rcw_src1/SPI1_PCS2	IFC_AD09	SPI1_PCS2	cfg_rcw_src1					
	NA	IFC_AD10/cfg_rcw_src2/SPI1_PCS3	IFC_AD10	SPI1_PCS3	cfg_rcw_src2					
	NA	IFC_AD11/cfg_rcw_src3/SPI1_PCS4	IFC_AD11	SPI1_PCS4	cfg_rcw_src3					
	NA	IFC_AD12/cfg_rcw_src4/SPI1_PCS5	IFC_AD12	SPI1_PCS5	cfg_rcw_src4					
	NA	IFC_AD13/cfg_rcw_src5/SPI1_SOUT	IFC_AD13	SPI1_SOUT	cfg_rcw_src5					
	NA	IFC_AD14/cfg_rcw_src6	IFC_AD14		cfg_rcw_src6					
	NA	IFC_AD15/cfg_rcw_src7	IFC_AD15		cfg_rcw_src7					
	NA	IFC_AVD	IFC_AVD							
	NA	IFC_BCTL	IFC_BCTL							
	NA	IFC_CLE/cfg_rcw_src8	IFC_CLE		cfg_rcw_src8					
	NA	IFC_CLK0	IFC_CLK0							
	NA	IFC_CLK1	IFC_CLK1							
	NA	IFC_CS0_B	IFC_CS0_B							
	NA	IFC_CS1_B/GPIO2_10/SPI1_PCS0/ FTM7_CH0	IFC_CS1_B	GPIO2_10	SPI1_PCS0		FTM7_CH0			
	NA	IFC_CS2_B/GPIO2_11/ SPI1_SCK/FTM7_CH1/ IIC3_SCL	IFC_CS2_B	GPIO2_11	SPI1_SCK		FTM7_CH1	IIC3_SCL		
	NA	IFC_CS3_B /GPIO2_12/ QSPI_DIO_B3/IIC3_SDA/ FTM7_EXTCLK	IFC_CS3_B	GPIO2_12	IIC3_SDA	QSPI_DIO_B3	FTM7_EXTCLK			

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	IFC_NDDDR_CLK	IFC_NDDDR_CLK							
	NA	IFC_NDDQS	IFC_NDDQS							
	NA	IFC_OE_B/cfg_eng_use1	IFC_OE_B		cfg_eng_use1					
	NA	IFC_PAR0/GPIO2_13/QSPI_DIO_B0/FTM6_CH0	IFC_PAR0	GPIO2_13		QSPI_DIO_B0	FTM6_CH0			
	NA	IFC_PAR1/GPIO2_14/QSPI_DIO_B1/FTM6_CH1	IFC_PAR1	GPIO2_14		QSPI_DIO_B1	FTM6_CH1			
	NA	IFC_PERR_B/GPIO2_15/QSPI_DIO_B2/FTM6_EXTCLK	IFC_PERR_B	GPIO2_15		QSPI_DIO_B2	FTM6_EXTCLK			
	NA	IFC_RB0_B	IFC_RB0_B							
	NA	IFC_RB1_B/SPI1_SIN	IFC_RB1_B		SPI1_SIN					
	NA	IFC_TE/cfg_ifc_te	IFC_TE		cfg_ifc_te					
	NA	IFC_WE0_B/cfg_eng_use0	IFC_WE0_B		cfg_eng_use0					
	NA	IFC_WP0_B/cfg_eng_use2	IFC_WP0_B		cfg_eng_use2					
RGMII1	NA	EC1_GTX_CLK/GPIO3_07/ EC1_TX_CLK/ SAI2_TX_BCLK/ FTM1_EXTCLK	EC1_GTX_CLK	GPIO3_07		SAI2_TX_BCLK	EC1_TX_CLK			FTM1_EXTCLK
	NA	EC1_GTX_CLK125/ GPIO3_08/EC1_RX_ER/ EXT_AUDIO_MCLK2	EC1_GTX_CLK125	GPIO3_08	EXT_AUDIO_MCLK2		EC1_RX_ER			
	NA	EC1_RX_CLK/GPIO3_13/ SAI1_RX_BCLK/ FTM1_QD_PHA	EC1_RX_CLK	GPIO3_13		SAI1_RX_BCLK				FTM1_QD_PHA
	NA	EC1_RX_DV/GPIO3_14/ SAI2_RX_BCLK/ FTM1_QD_PHB	EC1_RX_DV	GPIO3_14		SAI2_RX_BCLK				FTM1_QD_PHB
	NA	EC1_RXD0/GPIO3_12/ SAI2_RX_SYNC/FTM1_CH0	EC1_RXD0	GPIO3_12		SAI2_RX_SYNC				FTM1_CH0
	NA	EC1_RXD1/GPIO3_11/ SAI1_RX_SYNC/FTM1_CH1	EC1_RXD1	GPIO3_11		SAI1_RX_SYNC				FTM1_CH1

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	EC1_RXD2/GPIO3_10/ CAN1_RX/SAI2_RX_DATA/ FTM1_CH6	EC1_RXD2	GPIO3_10	CAN1_RX	SAI2_RX_DATA				FTM1_CH6
	NA	EC1_RXD3/GPIO3_09/ CAN2_RX/SAI1_RX_DATA/ FTM1_CH4	EC1_RXD3	GPIO3_09	CAN2_RX	SAI1_RX_DATA				FTM1_CH4
	NA	EC1_TX_EN/GPIO3_06/ SAI1_TX_BCLK/FTM1_FAULT	EC1_TX_EN	GPIO3_06		SAI1_TX_BCLK				FTM1_FAULT
	NA	EC1_TXD0/GPIO3_05/ SAI2_TX_SYNC/FTM1_CH2	EC1_TXD0	GPIO3_05		SAI2_TX_SYNC				FTM1_CH2
	NA	EC1_TXD1/GPIO3_04/ SAI1_TX_SYNC/FTM1_CH3	EC1_TXD1	GPIO3_04		SAI1_TX_SYNC				FTM1_CH3
	NA	EC1_TXD2/GPIO3_03/ CAN1_TX/SAI2_TX_DATA/ FTM1_CH7	EC1_TXD2	GPIO3_03	CAN1_TX	SAI2_TX_DATA				FTM1_CH7
	NA	EC1_TXD3/GPIO3_02/ CAN2_TX/SAI1_TX_DATA/ FTM1_CH5	EC1_TXD3	GPIO3_02	CAN2_TX	SAI1_TX_DATA				FTM1_CH5
RGMII3	NA	EC3_GTX_CLK/GPIO4_01/ EC2_TX_ER/FTM3_CH0/ EC3_TX_CLK	EC3_GTX_CLK	GPIO4_01			EC2_TX_ER	EC3_TX_CLK		FTM3_CH0
	NA	EC3_GTX_CLK125GPIO4_02/EC2_ COL/ USB2_DRVVBUS/ EC3_RX_ER	EC3_GTX_CLK125	GPIO4_02		USB2_DRVVBUS	EC2_COL	EC3_RX_ER		
	NA	EC3_RX_CLK/GPIO4_07/ TSEC_1588_CLK_IN/ FTM3_QD_PHA	EC3_RX_CLK	GPIO4_07					TSEC_1588_CLK_IN	FTM3_QD_PHA
	NA	EC3_RX_DV/GPIO4_08/ TSEC_1588_TRIG_IN1/ FTM3_QD_PHB	EC3_RX_DV	GPIO4_08					TSEC_1588_TRIG_IN1	FTM3_QD_PHB
	NA	EC3_RXD0/GPIO4_06/ TSEC_1588_TRIG_IN2/ EC2_CRS/FTM3_CH2	EC3_RXD0	GPIO4_06			EC2_CRS		TSEC_1588_TRIG_IN2	FTM3_CH2

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	EC3_RXD1/GPIO4_05/ TSEC_1588_PULSE_OUT1/ FTM3_CH3	EC3_RXD1	GPIO4_05					TSEC_1588_PULSE_OUT1	FTM3_CH3
	NA	EC3_RXD2/GPIO4_04/ EC1_COL/FTM3_EXTCLK	EC3_RXD2	GPIO4_04			EC1_COL			FTM3_EXTCLK
	NA	EC3_RXD3/GPIO4_03/ EC1_CRS/FTM3_FAULT	EC3_RXD3	GPIO4_03			EC1_CRS			FTM3_FAULT
	NA	EC3_TX_EN/GPIO4_00/ EC1_TX_ER/FTM3_CH1	EC3_TX_EN	GPIO4_00			EC1_TX_ER			FTM3_CH1
	NA	EC3_TXD0/GPIO3_31/ TSEC_1588_PULSE_OUT2/ FTM3_CH4	EC3_TXD0	GPIO3_31					TSEC_1588_PULSE_OUT2	FTM3_CH4
	NA	EC3_TXD1/GPIO3_30/ TSEC_1588_CLK_OUT/ FTM3_CH5	EC3_TXD1	GPIO3_30					TSEC_1588_CLK_OUT	FTM3_CH5
	NA	EC3_TXD2/GPIO3_29/ TSEC_1588_ALARM_OUT1/ FTM3_CH6	EC3_TXD2	GPIO3_29					TSEC_1588_ALARM_OUT1	FTM3_CH6
	NA	EC3_TXD3/GPIO3_28/ TSEC_1588_ALARM_OUT2/ FTM3_CH7	EC3_TXD3	GPIO3_28					TSEC_1588_ALARM_OUT2	FTM3_CH7
Ethernet Management Interface 1	212	EMI1_MDC/GPIO3_00	EMI1_MDC	GPIO3_00						
	214	EMI1_MDIO/GPIO3_01	EMI1_MDIO	GPIO3_01						
Programmable Interrupt Controller	NA	EVT9_B/GPIO2_24	EVT9_B	GPIO2_24						
	NA	IRQ0	IRQ0							
	NA	IRQ1	IRQ1							
	NA	IRQ2	IRQ2							
	NA	IRQ3/GPIO1_23	IRQ3	GPIO1_23	Ethernet INT					
	NA	IRQ4/GPIO1_24/SDHC_VS	IRQ4	GPIO1_24		SDHC_VS				
LPUART Interface	NA	SDHC_CLK/GPIO2_09/ LPUART3_CTS_B/ LPUART6_SIN	SDHC_CLK	GPIO2_09	LPUART6_SIN	LPUART3_CTS_B				

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	SDHC_DAT3/GPIO2_08/ LPUART3_RTS_B/ LPUART6_SOUT	SDHC_DAT3	GPIO2_08	LPUART6_SOUT	LPUART3_RTS_B				
SPI2	NA	UART1_CTS_B/GPIO1_21/ UART3_SIN/LPUART2_SIN/ SPI2_SIN/2D-ACE_VSYNC	UART1_CTS_B	GPIO1_21	LPUART2_SIN		UART3_SIN	SPI2_SIN	2D-ACE_VSYNC	
	NA	UART1_RTS_B/GPIO1_19/ UART3_SOUT/ LPUART2_SOUT/ SPI2_SOUT/2D-ACE_HSYNC	UART1_RTS_B	GPIO1_19	LPUART2_SOUT		UART3_SOUT	SPI2_SOUT	2D-ACE_HSYNC	
	NA	UART2_CTS_B/GPIO1_22/ UART4_SIN/SPI2_SCK/LPUART1_ CTS_B/ LPUART4_SIN	UART2_CTS_B	GPIO1_22	LPUART1_CTS_B	LPUART4_SIN	UART4_SIN	SPI2_SCK		
	NA	UART2_SIN/GPIO1_18/ LPUART1_SIN/SPI2_PCS1	UART2_SIN	GPIO1_18	LPUART1_SIN			SPI2_PCS1		
	NA	UART2_SOUT/GPIO1_16/ SPI2_PCS0/LPUART1_SOUT	UART2_SOUT	GPIO1_16	LPUART1_SOUT			SPI2_PCS0		
GPIO	NA	EC2_GTX_CLK/GPIO3_20/ EC2_TX_CLK/USB2_CLK/ FTM2_EXTCLK	EC2_GTX_CLK	GPIO3_20		USB2_CLK	EC2_TX_CLK			FTM2_EXTCLK
	NA	EC2_GTX_CLK125GPIO3_21/EC2_ RX_ER/ USB2_PWRFAULT	EC2_GTX_CLK125	GPIO3_21		USB2_PWRFAULT	EC2_RX_ER			
	NA	EC2_RX_CLK/GPIO3_26/ USB2_DIR/FTM2_QD_PHA	EC2_RX_CLK	GPIO3_26		USB2_DIR				FTM2_QD_PHA
	NA	EC2_RX_DV/GPIO3_27/ USB2_NXT/FTM2_QD_PHB	EC2_RX_DV	GPIO3_27		USB2_NXT				FTM2_QD_PHB
	NA	EC2_RXD0/GPIO3_25/ USB2_D0/FTM2_CH0	EC2_RXD0	GPIO3_25		USB2_D0				FTM2_CH0
	NA	EC2_RXD2/GPIO3_23/ CAN3_RX/USB2_D2/ FTM2_CH6	EC2_RXD2	GPIO3_23	CAN3_RX	USB2_D2				FTM2_CH6

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	NA	IRQ5/GPIO1_25/ SDHC_CLK_SYNC_IN/ SPI2_PCS5	IRQ5	GPIO1_25	SPI2_PCS5	SDHC_CLK_SYNC_IN				
	NA	SDHC_DAT4/GPIO4_23/ SDHC_CLK_SYNC_OUT	SDHC_DAT4	GPIO4_23		SDHC_CLK_SYNC_OUT				
	NA	CLK10/GPIO4_20/BRGO3/ SAI3_RX_SYNC/ FTM4_QD_PHB/2D-ACE_D11	CLK10	GPIO4_20	BRGO3		SAI3_RX_SYNC	2D-ACE_D11	FTM4_QD_PHB	
	NA	CLK11/GPIO4_21/BRGO4/ SAI4_RX_SYNC/ FTM8_CH0/2D-ACE_DE	CLK11	GPIO4_21	BRGO4		SAI4_RX_SYNC	2D-ACE_DE	FTM8_CH0	
	NA	CLK12/GPIO4_22/BRGO1/ FTM8_CH1/2DACE_ CLK_OUT	CLK12	GPIO4_22	BRGO1			2D-ACE_CLK_OUT	FTM8_CH1	
	NA	TDMA_RQ/GPIO4_13/ UC1_CDB_RXER/ EXT_AUDIO_MCLK1/ FTM4_CH3/2D-ACE_D04	TDMA_RQ	GPIO4_13		UC1_CDB_RXER	EXT_AUDIO_MCLK1	2D-ACE_D04	FTM4_CH3	
	NA	TDMA_RSYNC/GPIO4_10/ UC1_CTSB_RXDV/ SAI3_TX_BCLK/ FTM4_CH6/2D-ACE_D01	TDMA_RSYNC	GPIO4_10		UC1_CTSB_RXDV	SAI3_TX_BCLK	2D-ACE_D01	FTM4_CH6	
	NA	TDMA_TXD/GPIO4_11/ UC1_TXD7/SAI3_TX_DATA/ FTM4_CH5/2D-ACE_D02	TDMA_TXD	GPIO4_11		UC1_TXD7	SAI3_TX_DATA	2D-ACE_D02	FTM4_CH5	
Board to Board Connectorr1 Interfaces from LS1021A										
GPIO	32	EC2_RXD1/GPIO3_24/ USB2_D1/FTM2_CH1	EC2_RXD1	GPIO3_24		USB2_D1				FTM2_CH1
	18	EC2_RXD3/GPIO3_22/ CAN4_RX/USB2_D3/ FTM2_CH4	EC2_RXD3	GPIO3_22	CAN4_RX	USB2_D3				FTM2_CH4
	38	EC2_TX_EN/GPIO3_19/ USB2_STP/FTM2_FAULT	EC2_TX_EN	GPIO3_19		USB2_STP				FTM2_FAULT
	28	EC2_TXD0/GPIO3_18/ USB2_D4/FTM2_CH2	EC2_TXD0	GPIO3_18		USB2_D4				FTM2_CH2

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	30	EC2_TXD1/GPIO3_17/ USB2_D5/FTM2_CH3	EC2_TXD1	GPIO3_17		USB2_D5				FTM2_CH3
	34	TDMA_RXD/GPIO4_09/ UC1_RXD7/SAI3_RX_DATA/ FTM4_CH7/2D-ACE_D00	TDMA_RXD	GPIO4_09		UC1_RXD7	SAI3_RX_DATA	2D-ACE_D00	FTM4_CH7	
Board to Board Connector2 Interfaces from LS1021A										
I2C	48	IIC1_SCL	IIC1_SCL							
	46	IIC1_SDA	IIC1_SDA							
	76	IIC2_SCL/GPIO4_27/ SDHC_CD_B/SPI2_PCS3	IIC2_SCL	GPIO4_27	SPI2_PCS3	SDHC_CD_B				
	78	IIC2_SDA/GPIO4_28/ SDHC_WP/SPI2_PCS4	IIC2_SDA	GPIO4_28	SPI2_PCS4	SDHC_WP				
LPUART	50	SDHC_CMD/GPIO2_04/ LPUART3_SOUT	SDHC_CMD	GPIO2_04	LPUART3_SOUT					
	52	SDHC_DAT0/GPIO2_05/ LPUART3_SIN	SDHC_DAT0	GPIO2_05	LPUART3_SIN					
	81	SDHC_DAT1/GPIO2_06/ LPUART2_RTS_B/ LPUART5_SOUT	SDHC_DAT1	GPIO2_06	LPUART5_SOUT	LPUART2_RTS_B				
	79	SDHC_DAT2/GPIO2_07/ LPUART2_CTS_B/ LPUART5_SIN	SDHC_DAT2	GPIO2_07	LPUART5_SIN	LPUART2_CTS_B				
Data UART	56	UART1_SIN/GPIO1_17	UART1_SIN	GPIO1_17						
	54	UART1_SOUT/GPIO1_15	UART1_SOUT	GPIO1_15						
GPIO	32	EC2_TXD2/GPIO3_16/ CAN3_TX/USB2_D6/ FTM2_CH7	EC2_TXD2	GPIO3_16	CAN3_TX	USB2_D6				FTM2_CH7
	61	EC2_TXD3/GPIO3_15/ CAN4_TX/USB2_D7/ FTM2_CH5	EC2_TXD3	GPIO3_15	CAN4_TX	USB2_D7				FTM2_CH5
	72	SDHC_DAT5/GPIO4_24/ SDHC_CMD_DIR	SDHC_DAT5	GPIO4_24		SDHC_CMD_DIR				

Interface/ Function	B2B Connector Pin Number	LS1021A Processor's Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
	65	SDHC_DAT6/GPIO4_25/ USB1_DRVVBUS/ SDHC_DAT0_DIR	SDHC_DAT6	GPIO4_25	USB1_DRVVBUS	SDHC_DAT0_DIR				
	42	SDHC_DAT7/GPIO4_26/ USB1_PWRFAULT/ SDHC_DAT123_DIR	SDHC_DAT7	GPIO4_26	USB1_PWRFAULT	SDHC_DAT123_DIR				
	62	CLK09/GPIO4_19/BRGO2/ SAI3_RX_BCLK/ FTM4_QD_PHA/2D-ACE_D10	CLK09	GPIO4_19	BRGO2		SAI3_RX_BCLK	2D-ACE_D10	FTM4_QD_PHA	
	71	TDMA_TSYNC/GPIO4_12/ UC1_RTSB_TXEN/ SAI3_TX_SYNC/ FTM4_CH4/2D-ACE_D03	TDMA_TSYNC	GPIO4_12		UC1_RTSB_TXEN	SAI3_TX_SYNC	2D-ACE_D03	FTM4_CH4	
	69	TDMB_RQ/GPIO4_18/ UC3_CDB_RXER/ SPDIF_EXTCLK/ SAI4_RX_BCLK/ FTM4_EXTCLK/2D-ACE_D09	TDMB_RQ	GPIO4_18	SPDIF_EXTCLK	UC3_CDB_RXER	SAI4_RX_BCLK	2D-ACE_D09	FTM4_EXTCLK	
	66	TDMB_RSYNC/GPIO4_15/ UC3_CTSB_RXDV/ SPDIF_PLOCK/ SAI4_TX_BCLK/ FTM4_CH1/2D-ACE_D06	TDMB_RSYNC	GPIO4_15	SPDIF_PLOCK	UC3_CTSB_RXDV	SAI4_TX_BCLK	2D-ACE_D06	FTM4_CH1	
	64	TDMB_RXD/GPIO4_14/ UC3_RXD7/SPDIF_IN/ SAI4_RX_DATA/ FTM4_CH2/2D-ACE_D05	TDMB_RXD	GPIO4_14	SPDIF_IN	UC3_RXD7	SAI4_RX_DATA	2D-ACE_D05	FTM4_CH2	
	44	TDMB_TXD/GPIO4_16/ UC3_TXD7/SPDIF_OUT/ SAI4_TX_DATA/ FTM4_CH0/2D-ACE_D07	TDMB_TXD	GPIO4_16	SPDIF_OUT	UC3_TXD7	SAI4_TX_DATA	2D-ACE_D07	FTM4_CH0	

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Virtex UltraScale+ FPGA SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Virtex UltraScale+ FPGA SOM.

Table 8: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[2]	0V	3V	3.15V	±20mV

[1] Virtex UltraScale+ FPGA SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector2.

[2] Virtex UltraScale+ FPGA SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

The Virtex UltraScale+ FPGA SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOMPWR_EN signal from Board to Board Connector1 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board to Board Connector1 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

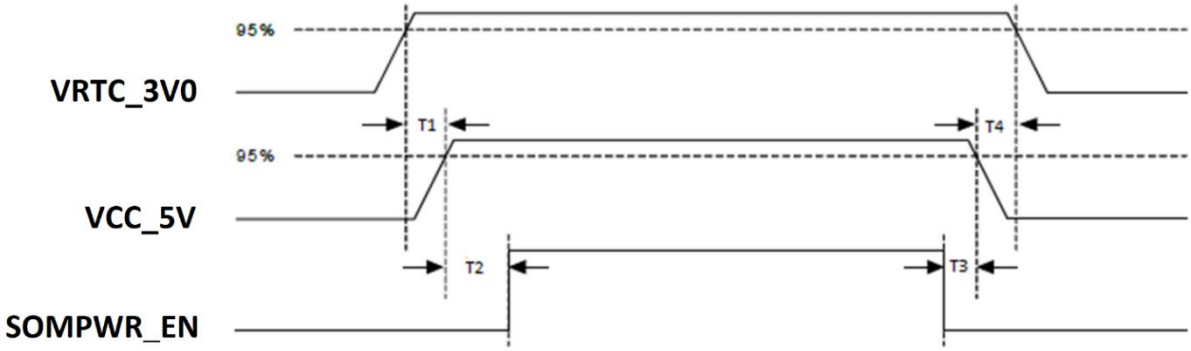


Figure 9: Power Input Sequencing

Table 9: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] *VRTC_3V0 is the RTC Battery backup supply. This is an optional power.*

3.1.3 Power Consumption

The Virtex UltraScale+ FPGA SOM power consumption is considered by calculating power required for both Virtex UltraScale+ FPGA device and LS1021A processor.

The CPU power consumption is calculated based on LS1021A Datasheet power requirement. The Virtex UltraScale+ FPGA power is calculated using the Xilinx Power Estimation (XPE) tool.

For more accurate power estimation, iWave recommends to use Xilinx Power Estimator (XPE) tool and calculate the Virtex UltraScale+ FPGA power as per the design requirement. Also add extra 6A for other On-SOM CPU and other peripherals power.

For reference, we have calculated the Virtex UltraScale+ FPGA (VU13P) Theoretical Power Estimation by using Xilinx Power Estimator (XPE) tool with various FPGA utilisation and ambient temperature as shown below.

FPGA Utilisation (%)	SOM Theoretical Power Estimation @ 5V			
	25° C (Ambient)		60° C	
	TYP	Max	TYP	Max
50	22.534A/112.67W	23.315A/116.575W	30.801A/154.005W	31.813A/159.065W
80	29.739A/148.695W	30.721A/153.605W	41.073A/205.365W	42.368A/211.84W
100	36.79A/183.95W	37.977A/189.885W	46.084A/230.42W	47.528A/237.64W

Note: This calculation is based on VU13P device with maximum Process @ -3 Speed Grade

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Virtex UltraScale+ FPGA SOM.

Table 10: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS2 Compliance

iWave's Virtex UltraScale+ FPGA SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

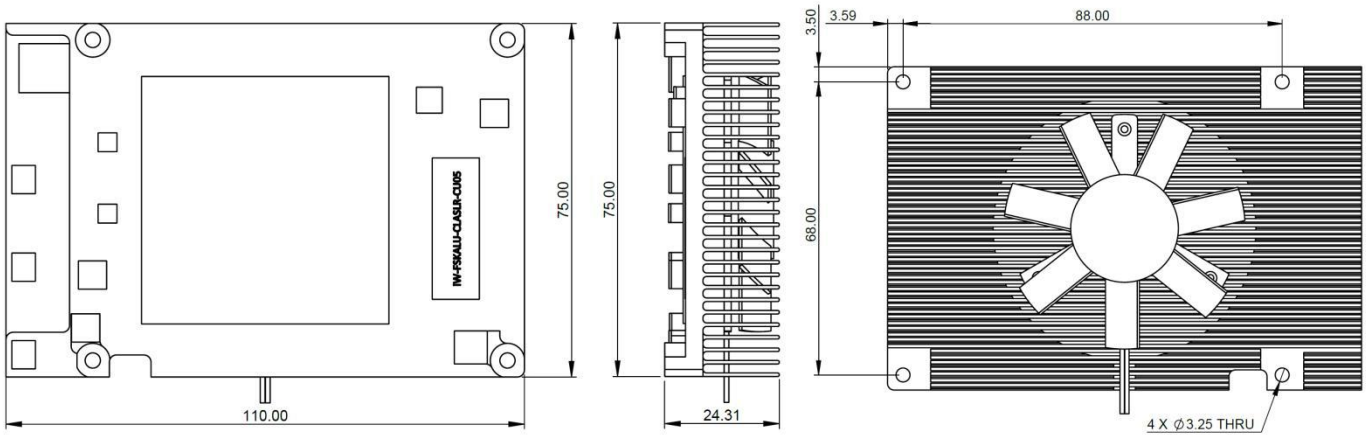
3.2.3 Electrostatic Discharge

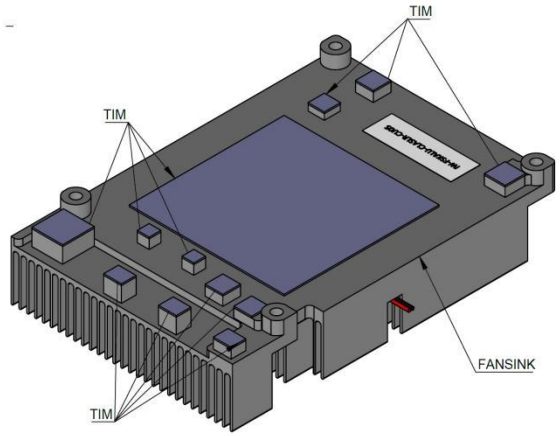
iWave's Virtex UltraScale+ FPGA SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System on Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.





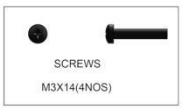


TABLE 1.1: FAN SPECIFICATIONS	
PART NO.	T056010BHZC0U3aR
DIMENSIONS	60X60X10.5mm
AIR FLOW	18.14CFM 0.51m3/min
STATIC PRESSURE	3.00mmH2O
RATED VOLTAGE	5V
LIFE EXPECTANCY	50,000hours at 40°C (WITH 15~65% RH)
ROHS	YES
CONNECTOR PART NO	510210200
CABLE LENGTH	150mm

TABLE1.2: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
THERMAL CONDUCTIVITY	6.5W/mK
FLAME RATING	UL 94 V-0
HARDNESS	27 Shore 00
WORKING TEMP.	-40~+160 °C
ROHS	YES

Figure 10: Heat Sink

3.3 Mechanical Characteristics

3.3.1 Virtex UltraScale+ FPGA SOM Mechanical Dimensions

Virtex UltraScale+ FPGA SOM PCB size is 110mm x 75mm x 2.64mm and weight is 125g. SOM mechanical dimension is shown below.

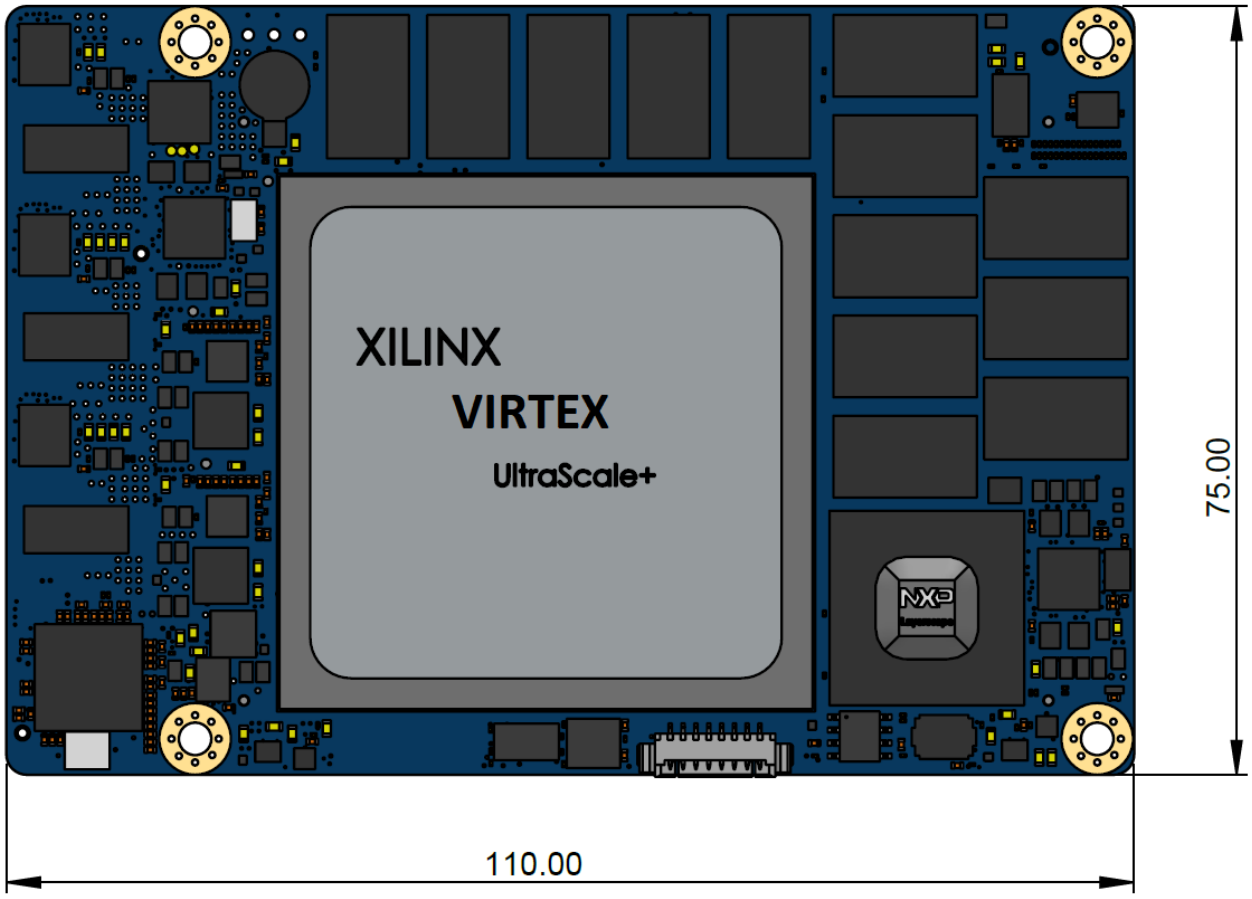


Figure 11: Mechanical dimension of Virtex UltraScale+ FPGA SOM - Top View

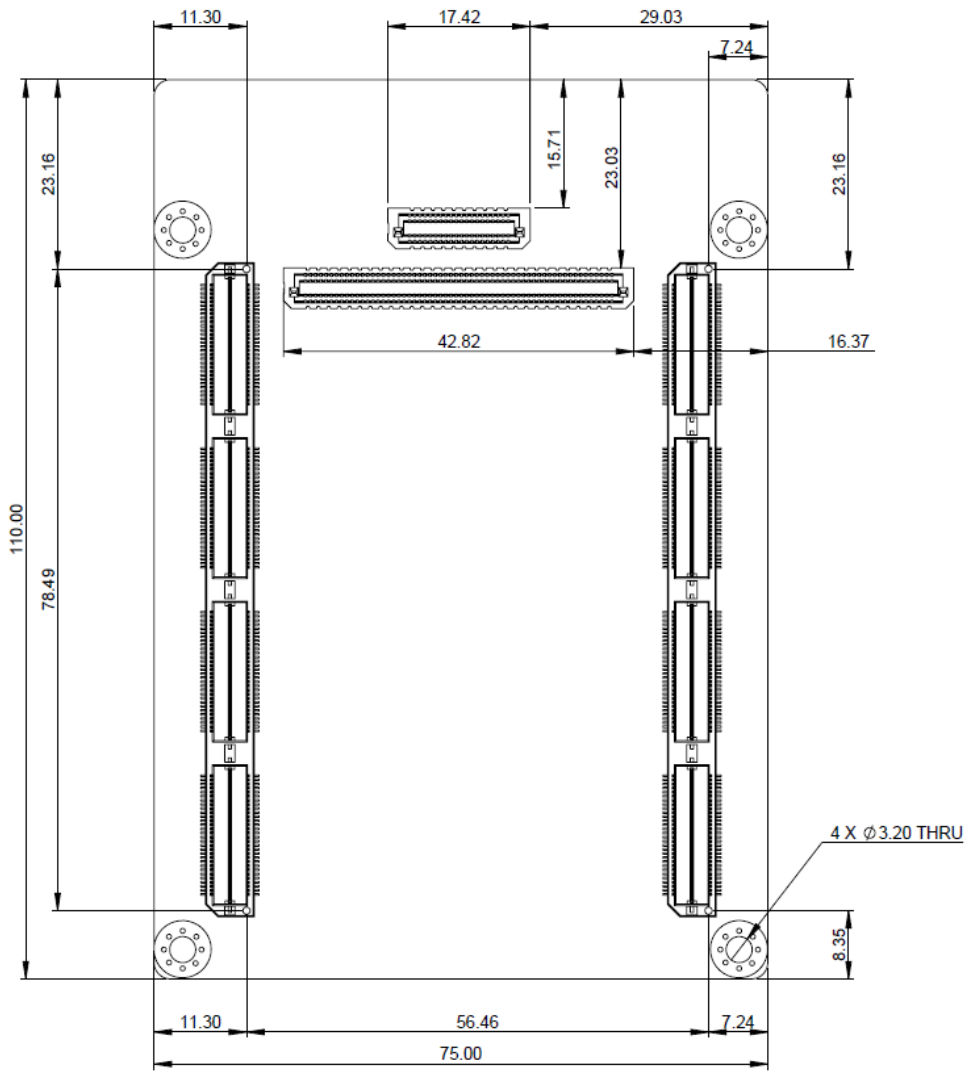


Figure 12: Mechanical dimension of Virtex UltraScale+ FPGA SOM - Bottom View

Virtex UltraScale+ FPGA PCB thickness is 2.64mm±0.1mm, top side maximum height component is Inductors L1, L2, L3 (6mm) and bottom side maximum height component is Board to Board connector 1 & 2 (4.27mm) followed by Board-to-Board connector 3(4.02mm). Please refer the below figure which gives height details of the Virtex UltraScale+ FPGA SOM.

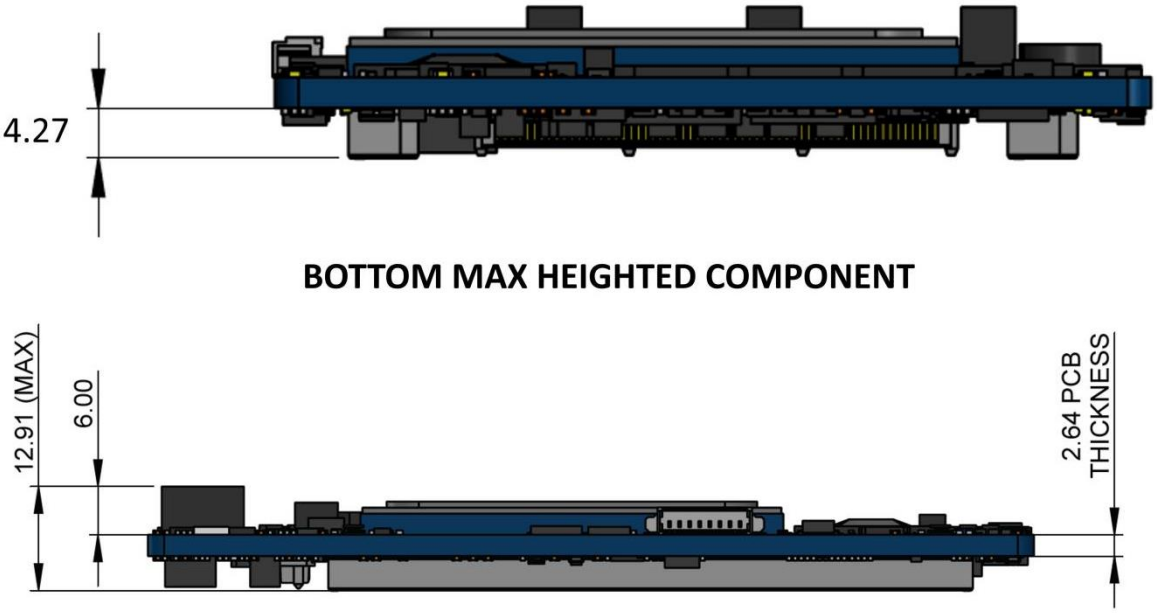


Figure 13: Mechanical dimension of Virtex UltraScale+ FPGA SOM - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Virtex UltraScale+ FPGA SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 11: Orderable Product Part Numbers

Product Part Number	Description	Temperature
VU07P FPGA based SOM		
iW-G47M-V07P-4E008G-Q128M-LEB	Virtex UltraScale+ VU07P(-1) FPGA (XCVU7P-1FLVB2104E) with Dual 4GB FPGA DDR4,128MB QSPI Flash and LS1021A CPU with 2GB DDR4, 256MB NOR Flash -SOM with Linux	Extended
VU13P FPGA based SOM		
iW-G47M-V13P-4E008G-Q128M-LEB	Virtex UltraScale+ VU13P(-1) FPGA (XCVU13P-1FHGB2104E) with Dual 4GB FPGA DDR4,128MB QSPI Flash and LS1021A CPU with 2GB DDR4, 256MB NOR Flash -SOM with Linux	Extended

5. APPENDIX

5.1 Virtex UltraScale+ FPGA SOM Development Platform

iWave Systems supports iW-RainboW-G47D–Virtex UltraScale+ FPGA SOM Development Platform which is targeted for quick validation of Virtex UltraScale+ FPGA based SOM. iWave's Virtex UltraScale+ FPGA Development Board incorporates Virtex UltraScale+ FPGA SOM and High-performance Carrier board with complete BSP support.

Contact us for more details on Virtex UltraScale+ FPGA SOM Development Platform.

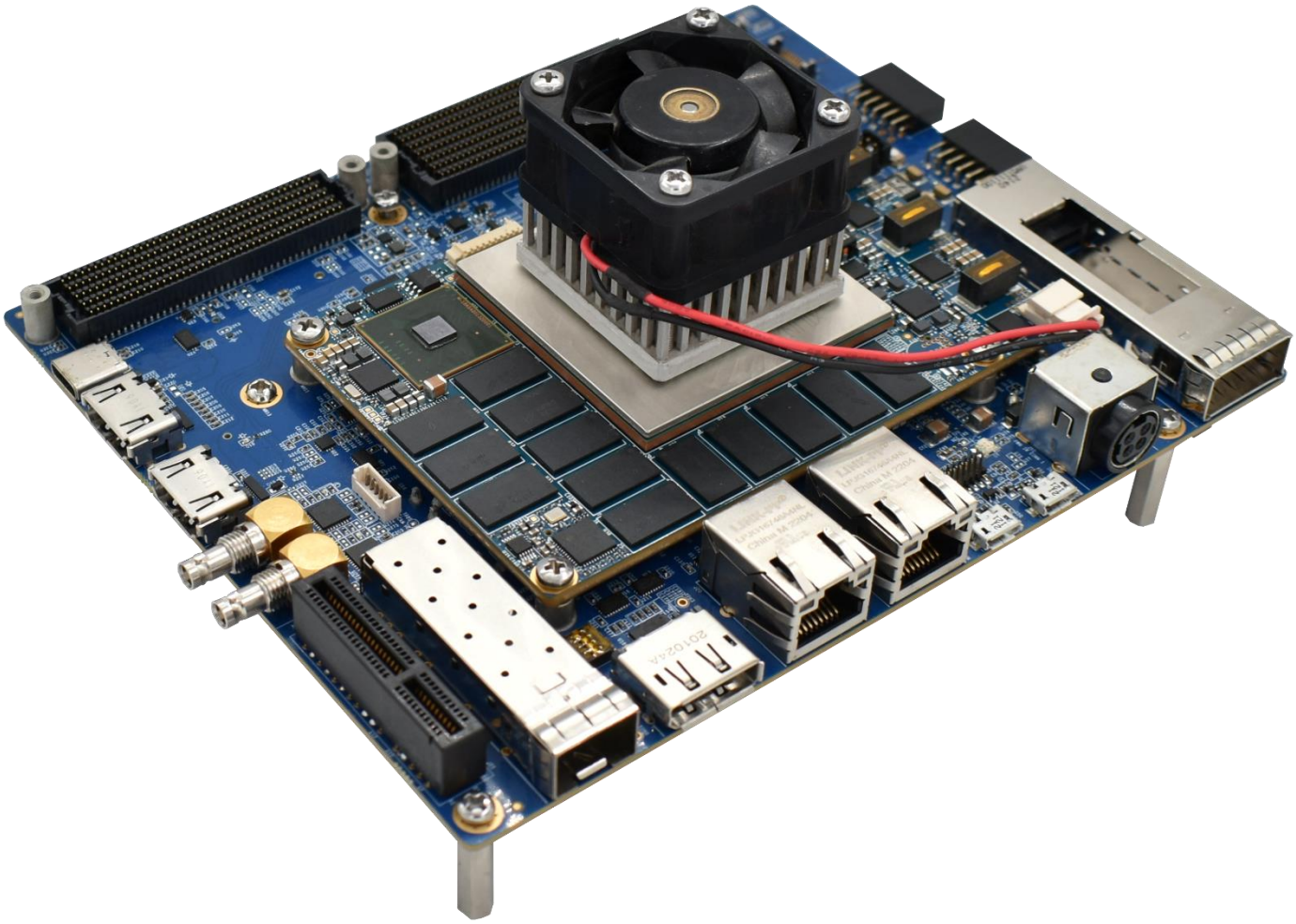


Figure 14 Virtex UltraScale+ FPGA Development Platform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