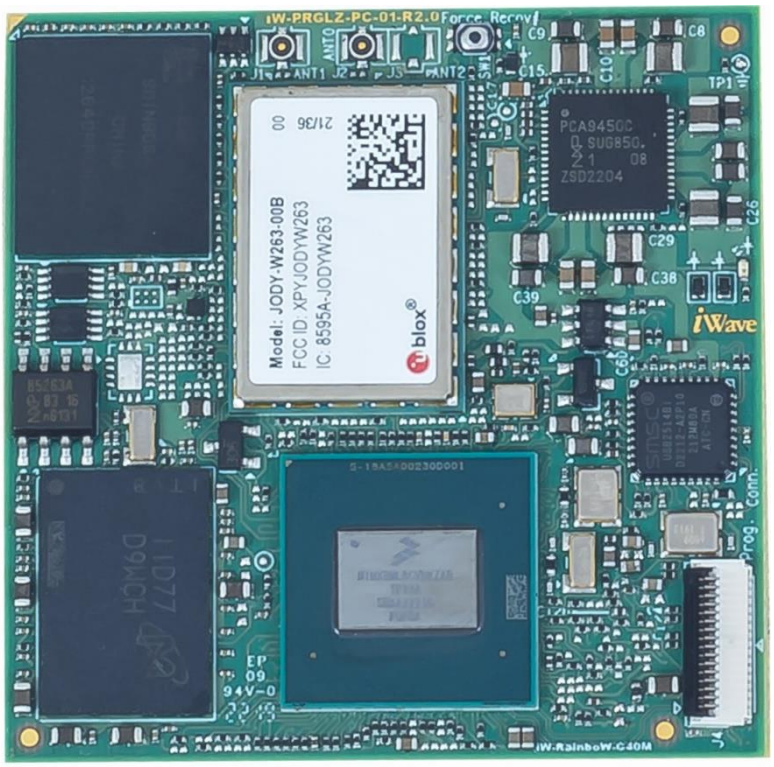
iW-RainboW-G40M
i.MX 8M Plus Quad/Quad Lite/Dual OSM-Size LF LGA Module Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the NXP's i.MX 8M Plus (Quad/Quad Lite/Dual) Application processor based OSM V1.0 specification compatible LGA module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8M Plus OSM Module from a Hardware Systems perspective.

1.2 OSM LGA Module Overview

The OSM V1.0 ("Open Standard Modules™") is a future proof and versatile standard for small size, low-cost embedded computer modules. Combining the following key characteristics like completely machine processible during soldering, assembly and testing, LGA package for direct PCB soldering without connector.

The OSM Module definition targeting application that requires low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 8M Plus SoC based OSM LGA Module is rich with i.MX 8M Plus features along with on-Board LPDDR4, eMMC, USB2.0 Hub, Wi-Fi and BT module and comes in compact 45mm x 45mm form factor (Size L). The Module PCB has 662 contacts which can be mounted as LGA on carrier card.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card

Acronyms	Abbreviations
FLEXCAN	Flexible Control Area Network
FlexSPI	Flexible Serial Peripheral Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LGA	Land Grid Array
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OSM	Open Standard Module
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDIO	Secure Digital Input Output
SoC	System on Chip
SPDIF	The Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPU	Video Processing Unit
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
HCSL	High speed Current Steering Logic
LVDS	Low Voltage Differential Signal
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
GBE	Gigabit Ethernet Signal
PCIe	PCIe differential pair signals
SATA	Serial Advanced Technology Attachment differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-OSM.

1.5 References

- IMX8MPxEC_Rev_x.pdf
- iMX_8M_Plus_RM_Revx.pdf
- OSM Specification V1.0

1.6 Important Note

In this document, wherever i.MX 8M Plus SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "Functionality Name"

  Example: ENET1_RGMII_TXC

  In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8M Plus OSM-LF LGA Module and Hardware architecture with high level block diagram.

2.1 i.MX 8M Plus OSM LGA Module Block Diagram

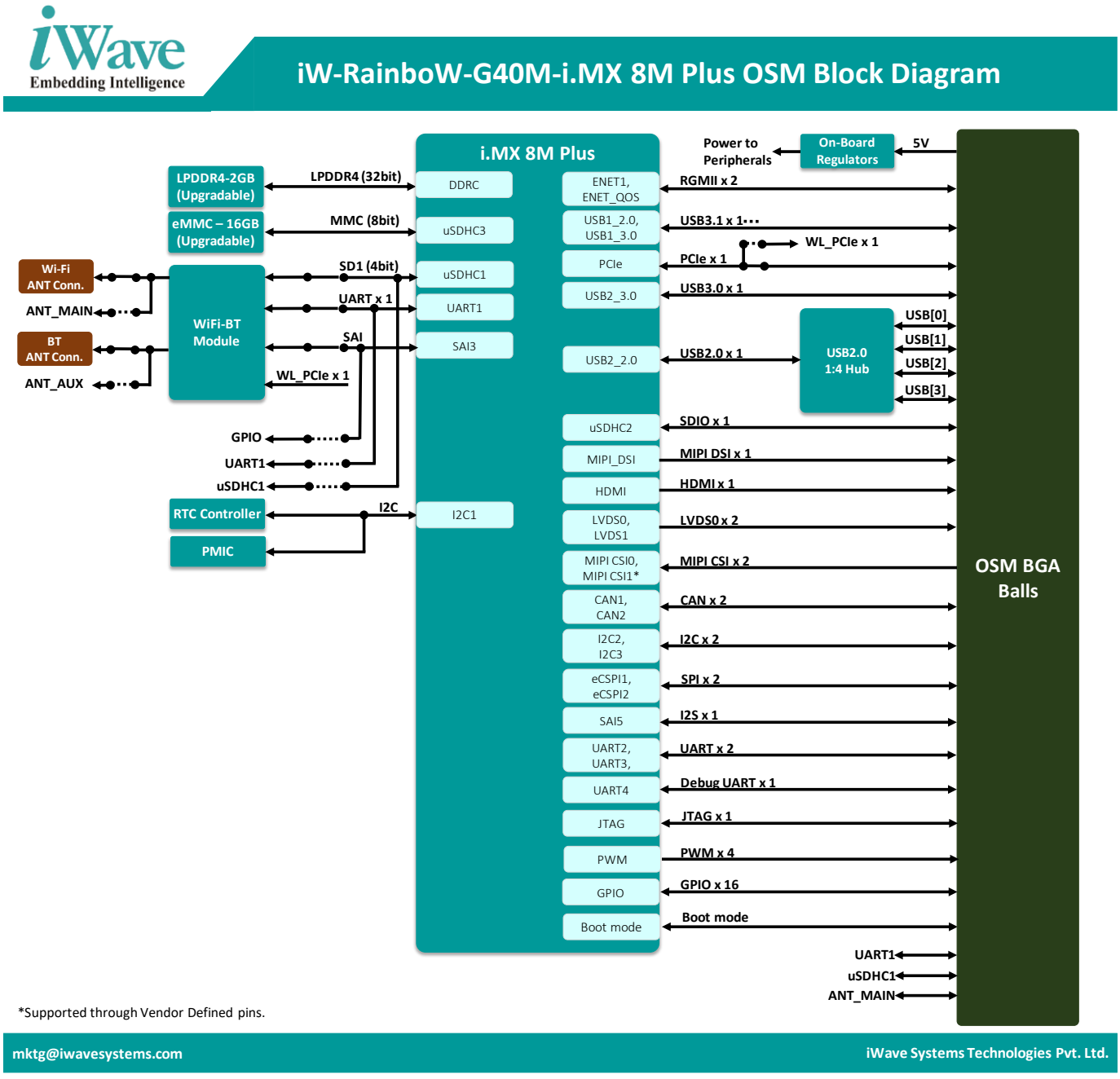

Figure 1: i.MX 8M Plus OSM-LF LGA Module Block Diagram

2.2 i.MX 8M Plus OSM Features

i.MX 8M Plus OSM LGA Module supports the following features.

SoC

- i.MX 8M Plus Applications Processor[1]
  - i.MX 8M Plus Quad : 4 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP
  - i.MX 8M Plus Quad Lite : 4 x Cortex-A53, 1 x Cortex-M7 & GPU
  - i.MX 8M Plus Dual : 2 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP

Power

- PCA9450C PMIC

Memory

- LPDDR4 - 2GB (Expandable up to 8GB)
- eMMC Flash - 16GB (Expandable)[2]

Other On-Board Features

- IEEE 802.11 a/b/g/n/ac/ax Wi-Fi & BT 5.0 (ax is optional)
- USB 2.0, 4-Port Hub
- RTC Controller
- Programming Header

OSM LGA Interfaces

- RGMII x 2
- SDIO x 1 (4-bit x 1)
- SDIO x 1 (8-bit x 1) (Optional)[3]
- USB 3.0 x 2
- USB 2.0 x 2
- PCIe Gen3 x 1
- HDMI 2.0 Transmitter x 1
- MIPI DSI 4 lane x 1
- LVDS x 2 Channel
- SAI/I2S (Audio Interface) x 1
- SPI x 2 Port
- Data UART (with CTS & RTS) x 2 (1 is optional) [4]
- Data UART (without CTS & RTS) x 1
- Debug UART x 1
- OSM GPIOs

- CAN FD x 2
- I2C x 2

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 45mm X 45mm (OSM V1.0 Specification)

1. *There are six configurations of i.MX 8M Plus SoC supported by NXP, hence in this document i.MX 8M Plus Q/QL/D/DL/S/SL is used to represent either of one based on SBC Part Number.*
2. *Memory Size will differ based on iWave's OSM Product Part Number.*
3. *In default configuration, If on OSM Wi-Fi module is used, SD1 will not be supported on OSM LGA.*
4. *In default configuration, UART1 interface of i.MX 8M Plus is connected to on Board Bluetooth module. One more UART with CTS and RTS can be supported, if Bluetooth is not supported.*

2.3 i.MX 8M Plus SoC

iW-RainboW-G40M OSM LGA Module can support i.MX 8M Plus SoCs from NXP. The i.MX 8M Plus Family consists of three processors: i.MX 8M Plus Quad, i.MX 8M Plus Quad Lite and i.MX 8M Plus Dual. The major Difference between i.MX 8M Plus SoCs are:

- i.MX 8M Plus Quad : 4 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP
- i.MX 8M Plus Quad Lite : 4 x Cortex-A53, 1 x Cortex-M7 & GPU
- i.MX 8M Plus Dual : 2 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi4 Audio DSP

The i.MX 8M Plus processors along with ARM core supports integrated NPU of 2.3 TOPs, OpenCL 1.2 GPU, Image Signal Processor, 1080p60 video encode and decode capable VPU, 3 x display controllers, multiple display output options, including MIPI_DSI, HDMI 2.0, and LVDS. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, SD 3.0 and a wide range of peripheral I/Os such as PCIe Gen3 provide wide flexibility.

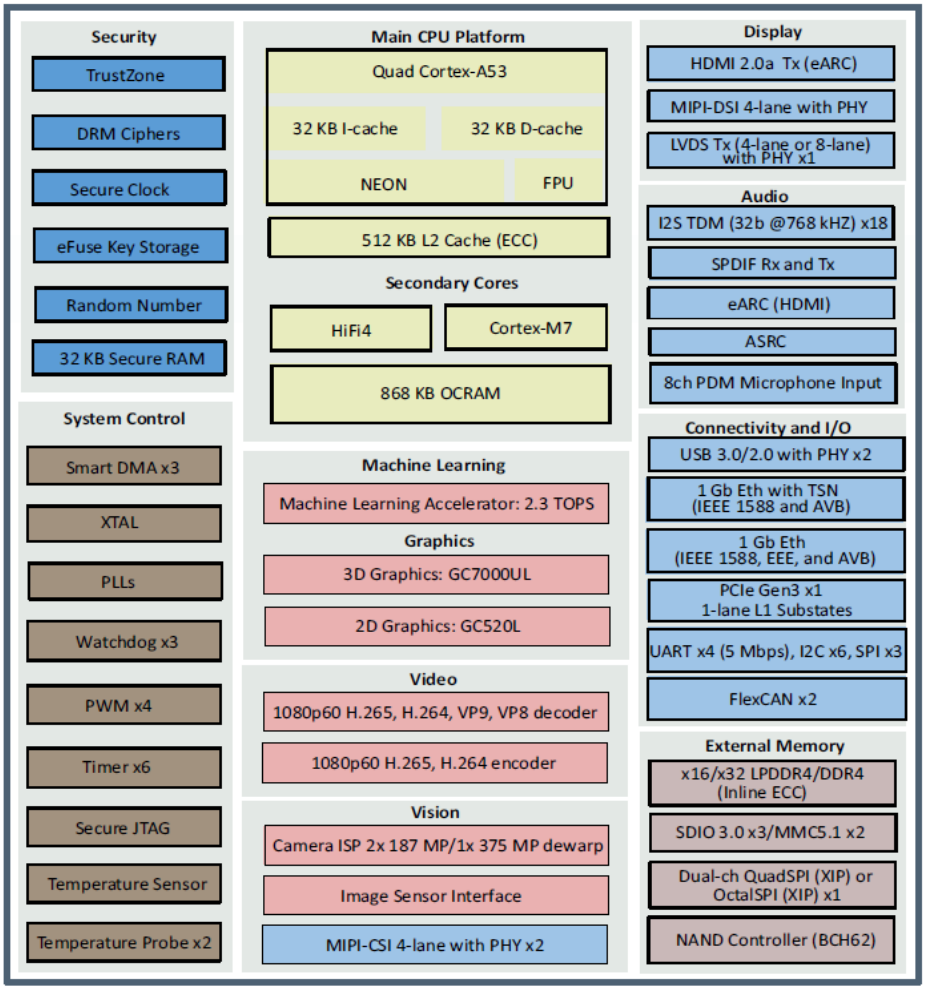

Figure 2: i.MX 8M Plus Block Diagram

Note: The i.MX 8M Plus processor offers numerous advanced features, please refer the latest i.MX 8M Plus Datasheet and Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PCA9450C PMIC

The i.MX 8M Plus OSM LGA Module uses one PCA9450C PMIC (U3) for module power management. The PCA9450C features six high efficiency step-down regulators and five linear regulators. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PCA9450C PMIC comes in 56pin 7x7 QFN package and is placed on the top side of the Module.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX 8M Plus OSM LGA Module supports 2GB LPDDR4 RAM memory by default using 32bit DDR_CH0 channel of i.MX 8M Plus SoC to support LPDDR4 up to 2GHz. LPDDR4 part U12 is placed on top side of the Module. The RAM size can be expandable up to maximum of 8GB (if chips are available). To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 8M Plus OSM LGA Module supports 16GB eMMC as default boot and storage device. This is directly connected to uSDHC3 controller of the i.MX 8M Plus SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) voltage levels.

The eMMC flash memory (U2) is physically located on top side of the Module. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.6 Network and Communiation

2.6.1 Wi-Fi and Bluetooth Interface

The i.MX 8M Plus OSM LGA Module is integrated with u-blox's "JODY-W263" or "JODY-W374/JODY-W377" based Wi-Fi and Bluetooth module. The JODY-W2 series are compact modules based on the NXP 88W8987 AEC-Q100 compliant chipset and JODY-W3 series are based on the NXP 88W9098 chipset. They enable Wi-Fi, Bluetooth, and Bluetooth low energy communication.

The JODY-W2 modules can be operated in the following modes:

• Wi-Fi 1x1 802.11a/b/g/n/ac in 2.4 GHz or 5 GHz.

• Dual-mode Bluetooth 5.2, including audio, can be operated fully simultaneous with Wi-Fi.

The JODY-W2 undergoes extended automotive qualification according to ISO 16750-4 and is manufactured in line with ISO/TS 16949. Connection to a host processor is through SDIO, or High-Speed UART interfaces. The i.MX 8M Plus OSM LGA Module uses processor's UART1 interface for Bluetooth and USDHC3 interface for Wi-Fi in a default configuration.

The JODY-W3 modules can be operated in the following modes:

• Wi-Fi 1x1 802.11a/b/g/n/ac/ax in 2.4 GHz and 5 GHz.

• Concurrent Dual Wi-Fi operation with independent MACs, supporting simultaneous Wi-Fi network operation at two different frequency bands.

• Dual-mode Bluetooth 5.3, can be operated fully simultaneous with Wi-Fi.

JODY-W3 modules undergo extended qualification testing in accordance with u-blox Qualification Policy based on AEC-Q104 and are manufactured in line with ISO/TS 16949 AEC-Q104. Host processor connections are made through various interfaces, including PCIe or SDIO for Wi-Fi and highspeed UART for Bluetooth. For 802.11ax, the i.MX 8M Plus OSM LGA Module uses processor's PCIe interface for Wi-Fi6.

In the OSM module, antenna pins of JODY-W2/W3 Bluetooth and Wi-Fi are connected to J1, J2 connectors and optionally connected to A16th and A20th pin of OSM. J3 connector is optionally provided to support Bluetooth independently in JODY-W3.

Note: In default configuration, 802.11ax (Wi-Fi 6) is not supported, but 802.11ax can be supported by changing Wi-Fi module from JODY-W2 to JODY-W3 and some additional changes. Contact iWave Support Team for further information.

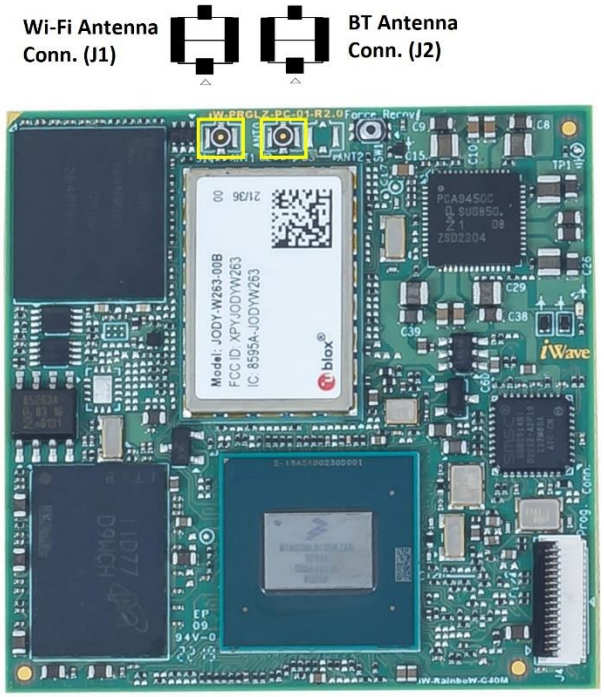

Figure 3: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : RECE-20449-001E-01 from Taoglas Limited / MM4829-2702RA4 from Murata.

Antenna Part Number - : FXP830.24.0100B from Taoglas Limited / 2042811100 from Molex.

2.6.2 RTC Controller

The i.MX 8M Plus OSM LGA Module by supports external RTC Controller “PCF85263” On-OSM for Real time clock support. This external RTC Controller is connected to i.MX 8M Plus SoC through I2C3 Interface and operates at 1.8V voltage level. In OSM power off condition, this device will take power from OSM ball #W17 (VRTC_3V0) coin cell power and continues to keep the current time.

2.7 OSM LGA Contacts

OSM LGA (J5) has standard pinout as per OSM Specification V1.0. The interfaces which are available at 662 contacts are explained in the following sections.

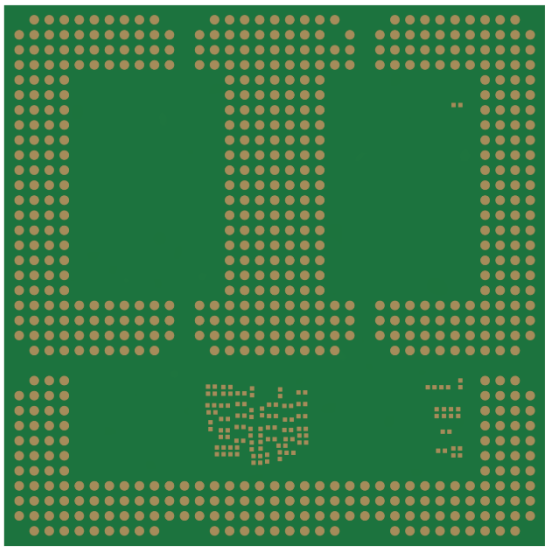

Figure 4: OSM LGA Contacts

Number of contacts - : 662 (Size L)

Table 3: i.MX 8M Plus OSM LGA Module Pinouts

OSM Pins	Signal
SIZE 0	
M18	NC
N18	NC
U19	BOOT_SEL#
AB17	FLEXCAN1_RX(SAI5_RXD2)
AC17	FLEXCAN1_TX(SAI5_RXD1)
AB19	FLEXCAN2_RX(SAI5_MCLK)
AC19	FLEXCAN2_TX(SAI5_RXD3)
V17	CARRIER_PWR_ON
A15	GND
A16	OSM_ANT0
A17	GND
A18	GND
A19	GND
A20	OSM_ANT1
A21	GND
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
C15	NC
C17	NC
C19	NC
C21	NC
AC18	JTAG_MOD*
F15	NC
E16	NC
R15	ENET_QOS_RGMII_RXC
M15	ENET_QOS_RGMII_RX_CTL
L16	NC
N15	ENET_QOS_RGMII_RD2
P15	ENET_QOS_RGMII_RD3
J15	ENET_QOS_RGMII_TXC
K16	ENET_QOS_RGMII_TX_CTL
H16	ENET_QOS_RGMII_TD2
G16	ENET_QOS_RGMII_TD3
K15	ENET_QOS_RGMII_RD0

OSM Pins	Signal
L15	ENET_QOS_RGMII_RD1
H15	ENET_QOS_RGMII_TD0
G15	ENET_QOS_RGMII_TD1
N16	NC
T16	ENET_QOS_MDC
T15	ENET_QOS_MDIO
D18	GND
E15	GND
E21	GND
F16	GND
F20	GND
J16	GND
J20	GND
L18	GND
M16	GND
M20	GND
P18	GND
R16	GND
R20	GND
V16	GND
V20	GND
Y18	GND
AA14	GND
AA17	GND
AA19	GND
AA22	GND
AB15	GND
AB21	GND
D17	OSM_GPIO_A_0(SAI1_TXD6_GPIO4_18)
E17	OSM_GPIO_A_1(SAI1_TXD7_GPIO4_19)
F17	OSM_GPIO_A_2(SAI1_RXFS_GPIO4_0)
G17	OSM_GPIO_A_3(SAI1_RXC_GPIO4_1)
H17	OSM_GPIO_A_4(SAI1_RXD0_GPIO4_2)
J17	OSM_GPIO_A_5(SAI5_RXC_GPIO3_20)
K17	OSM_GPIO_A_6(SAI2_RXC_GPIO4_22)
L17	OSM_GPIO_A_7(SAI2_RXFS_GPIO4_21)
D19	OSM_GPIO_B_0(SAI3_RXFS_GPIO4_28)
E19	OSM_GPIO_B_1(SAI1_RXD1_GPIO4_3)
F19	OSM_GPIO_B_2(SAI5_RXFS_GPIO3_21)
G19	OSM_GPIO_B_3(SPDIF1_EXT_CLK_GPIO5_5)
H19	OSM_GPIO_B_4(NAND_DQS_GPIO3_21)

OSM Pins	Signal
J19	OSM_GPIO_B_5(GPIO1_IO6)
K19	OSM_GPIO_B_6(GPIO1_IO00)
L19	OSM_GPIO_B_7(GPIO1_IO9)
AA15	I2C2_SCL
AA16	I2C2_SDA
AA20	I2C1_SCL
AA21	I2C1_SDA
V21	SAI2_RX_DATA0(SAI2_RXD0)
W21	SAI2_TX_DATA0(SAI2_TXD0)
V19	NC
W19	NC
W20	SAI2_TX_BCLK(SAI2_TXC)
W18	SAI2_TX_SYNC(SAI2_TXFS)
V18	SAI2_MCLK
R19	JTAG_NTRST
P19	NC
N17	JTAG_TCK
P17	JTAG_TDI
R17	JTAG_TDO
N19	JTAG_TMS
E18	PWM1_OUT(I2C4_SDA)
F18	NC
G18	NC
H18	NC
J18	NC
K18	NC
R18	NC
T17	NC
T18	NC
T19	NC
Y13	NC
Y14	NC
AA13	NC
W17	VRTC_3V0
J21	SD2_CD_B
F21	SD2_CLK
E20	SD2_CMD
G20	SD2_DATA0
G21	SD2_DATA1
H20	SD2_DATA2
H21	SD2_DATA3

OSM Pins	Signal
C20	NVCC_SD2
D21	SD2_PWR_EN(SD2_RESET_B_GPIO2_19)
D20	SD2_WP
T21	SD1_CD#
K20	SD1_CLK
K21	SD1_CMD
L20	SD1_DATA0
L21	SD1_DATA1
M21	SD1_DATA2
N20	SD1_DATA3
N21	SD1_DATA4
P20	SD1_DATA5
P21	SD1_DATA6
R21	SD1_DATA7
T20	NVCC_SD1
U21	NC
U20	SD1_WP
W15	NC
W16	NC
Y15	ECSPI1_SS0
U16	ECSPI1_SCLK
U15	ECSPI1_MISO
V15	ECSPI1_MOSI
AA23	ECSPI2_SS0
Y21	ECSPI2_SCLK
Y22	ECSPI2_MISO(I2C4_SCL)
Y23	ECSPI2_MOSI
U17	PMIC_RST_B
C18	NC
C14	UART2_RTS_B(SAI3_RXD)
C13	UART2_CTS_B(SAI3_RXC)
A14	UART2_RXD
B13	UART2_TXD
D16	UART1_RTS_B*
D15	UART1_CTS_B*
D14	UART1_RX*
D13	UART1_TX*
A22	UART3_RX(NAND_ALE)
B23	UART3_TX(NAND_CE0_B)
D22	UART4_RXD
D23	UART4_TXD

OSM Pins	Signal
C22	NC
C23	NC
AB13	USB_HUB2OUT_DM
AC14	USB_HUB2OUT_DP
AC16	USB_HUB2OUT_PWR_EN
AB14	NC
AC15	USB_HUB2_OC
AB16	NC
AB23	USB_HUB3OUT_DM
AC22	USB_HUB3OUT_DP
AC20	USB_HUB3OUT_PWR_EN
AB22	NC
AC21	USB_HUB3_OC
AB20	USB_B_VBUS
AA18	V_BAT
AB18	V_BAT
M17	VDD_3V3
M19	NVCC_SD2
Y16	VDD_ARM_0V85
Y20	NVCC_SNVS_1V8
Y19	VCC_IN_3V3
Y17	VCC_IN_5V
U18	VCC_OUT_IO
B22	VDD_ENET0*
C16	EARC_AUX
P16	FORCE_RECOV#
SIZE S	
C2	CAMERA_CCMCLKO1(ECSPI2_MISO)
G3	OSM_GPIO_C_6(GPIO1_IO15)
G4	OSM_GPIO_C_7(GPIO1_IO10)
B3	MIPI_CSI1_CLK_N
B4	MIPI_CSI1_CLK_P
C1	MIPI_CSI1_D0_N
B1	MIPI_CSI1_D0_P
A2	MIPI_CSI1_D1_N
A3	MIPI_CSI1_D1_P
A5	MIPI_CSI1_D2_N
A6	MIPI_CSI1_D2_P
B6	MIPI_CSI1_D3_N
B7	MIPI_CSI1_D3_P
AB8	MIPI_DSI0_CLK_N

OSM Pins	Signal
AB7	MIPI_DSI0_CLK_P
AB11	MIPI_DSI0_D0_N
AB10	MIPI_DSI0_D0_P
AC9	MIPI_DSI0_D1_N
AC8	MIPI_DSI0_D1_P
AC6	MIPI_DSI0_D2_N
AC5	MIPI_DSI0_D2_P
AB5	MIPI_DSI0_D3_N
AB4	MIPI_DSI0_D3_P
AA3	NC
E1	NC
D2	NC
P1	ENET1_RGMII_RXC(SAI1_TXC)
L1	ENET1_RGMII_RX_CTL(SAI1_TXFS)
K2	NC
M1	ENET1_RGMII_RD2(SAI1_RXD6)
N1	ENET1_RGMII_RD3(SAI1_RXD7)
H1	ENET1_RGMII_TXC(SAI1_TXD5)
J2	ENET1_RGMII_TX_CTL(SAI1_TXD4)
G2	ENET1_RGMII_TD2(SAI1_TXD2)
F2	ENET1_RGMII_TD3(SAI1_TXD3)
J1	ENET1_RGMII_RD0(SAI1_RXD4)
K1	ENET1_RGMII_RD1(SAI1_RXD5)
G1	ENET1_RGMII_TD0(SAI1_TXD0)
F1	ENET1_RGMII_TD1(SAI1_TXD1)
M2	NC
P4	GND
D8	GND
B5	GND
AC10	GND
AC7	GND
AC4	GND
AB9	GND
AB6	GND
AB3	GND
AA11	GND
AA10	GND
AA8	GND
AA7	GND
AA4	GND
A4	GND

OSM Pins	Signal
A7	GND
A10	GND
B2	GND
B8	GND
B9	GND
C11	GND
D1	GND
D5	GND
E2	GND
H2	GND
H4	GND
L2	GND
L4	GND
P2	GND
U2	GND
U4	GND
V1	GND
W3	GND
Y2	GND
AA1	GND
R1	GND
D3	OSM_GPIO_C_0(GPIO1_IO7)
D4	OSM_GPIO_C_1(GPIO1_IO11)
E3	OSM_GPIO_C_2(SAI1_MCLK_GPIO4_20)
E4	NC
F3	NC
F4	NC
C4	I2C3_SCL
C3	I2C3_SDA
AB2	PCIE_RXN_N
AB1	PCIE_RXN_P
AC3	PCIE_TXN_N
AC2	PCIE_TXN_P
V2	OSM_PCIE_RST
W2	OSM_PCIE_PRST
Y1	PCIE_REFCLK_DM
W1	PCIE_REFCLK_DP
R2	GPIO_PCIE_SM_ALERT#(SAI3_MCLK_GPIO5_02)
T1	I2C2_SCL
U1	I2C2_SDA
T2	OSM_PCIE_WAKE

OSM Pins	Signal
AA9	CPU_ON_OFF
M4	NA
R4	NA
R3	NA
P3	NA
N3	NA
N4	NA
M3	NA
H3	NA
J4	NA
K4	NA
W4	NA
V3	NA
V4	NA
U3	NA
T3	NA
T4	NA
K3	NA
Y7	NA
AA6	NA
Y6	NA
AA5	NA
Y5	NA
Y4	NA
J3	NA
L3	NA
N2	NA
AA2	NA
D11	USB_OTG1_DM
D10	USB_OTG1_DP
C10	OSM_USB1_OTG_EN
D9	OSM_USB_OTG1_ID
C8	PU to VDD_3V3
B11	USB1_RX_N
B10	USB1_RX_P
A9	USB1_TX_N
A8	USB1_TX_P
C9	VBUS_OTG1
Y3	VDD_1V8
C5	NVCC_DRAM_1V1
Y9	VCC_IN_5V

OSM Pins	Signal
Y8	VCC_IN_5V
Y11	VCC_IN_5V
Y10	VCC_IN_5V
C6	ENET1_MDC(SAI1_RXD2)
C7	ENET1_MDIO(SAI1_RXD3)
D6	EARC_P_UTIL
D7	EARC_N_HPD
SIZE M	
AA31	MIPI_CSI2_D3_P
AA30	MIPI_CSI2_D3_N
AA29	USB_HUB4OUT_DM
Y31	MIPI_CSI2_D2_P
Y30	MIPI_CSI2_D2_N
Y29	USB_HUB4OUT_DP
Y27	VCC_IN_5V
Y26	VCC_IN_5V
Y25	VCC_IN_5V
Y28	VCC_IN_5V
B29	VDDA_1V8
AA33	VDD_SOC_0V85
C27	NC
A27	USB2_TX_P
A28	USB2_TX_N
B25	USB2_RX_P
B26	USB2_RX_N
C28	USB_HUB1_OC
D27	NC
C26	USB_HUB1OUT_PWR_EN
D25	USB_HUB1OUT_DP
D26	USB_HUB1OUT_DM
AB29	NC
AB30	NC
AC28	NC
AC29	NC
AB32	NC
AB33	NC
AC31	NC
AC32	NC
AB27	NC
AC26	NC
D30	NC

OSM Pins	Signal
C29	NC
D29	NC
C30	NC
AB26	NC
AB25	NC
T33	NC
T32	NC
R33	NC
R32	NC
P34	NC
P33	NC
P32	NC
N33	NC
N32	NC
M33	NC
M32	NC
L32	NC
K32	NC
J32	NC
K33	NC
L33	NC
K35	NC
L35	NC
L34	NC
M34	NC
Y33	NC
Y32	NC
W33	NC
W32	NC
V33	NC
V32	NC
U33	NC
U32	NC
AC33	GND
AC30	GND
AC27	GND
AB34	GND
AB31	GND
AB28	GND
AA32	GND
A29	GND

OSM Pins	Signal
A32	GND
B27	GND
B28	GND
B30	GND
B33	GND
C25	GND
C32	GND
C35	GND
D28	GND
D34	GND
F33	GND
F35	GND
G34	GND
H32	GND
J33	GND
J35	GND
K34	GND
M35	GND
N34	GND
AA28	GND
AA27	GND
AA26	GND
AA25	GND
W34	GND
T34	GND
A26	GND
R34	NC
AA35	NC
Y35	NC
U35	NC
V35	NC
AA34	NC
Y34	NC
V34	NC
N35	NC
P35	NC
R35	NC
U34	NC
T35	NC
W35	NC
AC34	NC

OSM Pins	Signal
AB35	NC
H34	NC
J34	NC
G35	NC
H35	NC
E34	NC
F34	NC
D35	NC
E35	NC
E33	NC
G32	NC
E32	NC
F32	NC
G33	NC
H33	NC
B34	HDMI_TX_CLK_P
B35	HDMI_TX_CLK_N
A33	HDMI_TX_D0_P
A34	HDMI_TX_D0_N
B31	HDMI_TX_D1_P
B32	HDMI_TX_D1_N
A30	HDMI_TX_D2_P
A31	HDMI_TX_D2_N
C31	HDMI_TX_CEC
D33	HDMI_TX_HPD
D31	NC
D32	NC
C33	HDMI_TX_DDC_SCL
C34	HDMI_TX_DDC_SDA
SIZE L	
AF3	NC
AE3	NC
AP1	NC
AL1	NC
AK2	NC
AM1	NC
AN1	NC
AH1	NC
AJ2	NC
AG2	NC
AF2	NC

OSM Pins	Signal
AJ1	NC
AK1	NC
AF1	NC
AG1	NC
AM2	NC
AR2	NC
AN4	NC
AN10	NC
AR8	NC
AP7	NC
AR9	NC
AR10	NC
AR5	NC
AP6	NC
AP3	NC
AP4	NC
AR6	NC
AR7	NC
AR3	NC
AR4	NC
AP9	NC
AP25	GND
AP28	GND
AP31	GND
AP34	GND
AR14	GND
AP19	GND
AR20	GND
AR26	GND
AR29	GND
AR32	GND
AP22	GND
AP16	GND
AE2	GND
AP13	GND
AP8	GND
AE34	GND
AP5	GND
AP2	GND
AN33	GND
AN21	GND

OSM Pins	Signal
AN18	GND
AR17	GND
AN15	GND
AF35	GND
AG3	GND
AH2	GND
AH34	GND
AJ35	GND
AK3	GND
AL2	GND
AL34	GND
AM13	GND
AM16	GND
AM19	GND
AM22	GND
AN11	GND
AN9	GND
AN6	GND
AN3	GND
AM35	GND
AF32	NC
AF33	NC
AG32	NC
AG33	NC
AH32	NC
AH33	NC
AJ32	NC
AJ33	NC
AN12	LVDS0_CLK_N
AN13	LVDS0_CLK_P
AP17	LVDS0_D0_N
AP18	LVDS0_D0_P
AR15	LVDS0_D1_N
AR16	LVDS0_D1_P
AP14	LVDS0_D2_N
AP15	LVDS0_D2_P
AP11	LVDS0_D3_N
AP12	LVDS0_D3_P
AN16	LVDS1_CLK_N
AN17	LVDS1_CLK_P
AM20	LVDS1_D0_N

OSM Pins	Signal
AM21	LVDS1_D0_P
AN19	LVDS1_D1_N
AN20	LVDS1_D1_P
AM17	LVDS1_D2_N
AM18	LVDS1_D2_P
AM14	LVDS1_D3_N
AM15	LVDS1_D3_P
AN23	LCD0_BKLT_EN(NAND_DATA01_GPIO3_7)
AN22	PWM2_OUT(SAI5_RXD0)
AM11	I2C5_SCL(SPDIF_TX)
AM12	I2C5_SDA(SPDIF_RX)
AN14	LCD0_VDD_EN(NAND_DATA02_GPIO3_8)
AP32	NC
AP33	NC
AP35	NC
AN35	NC
AL35	NC
AK35	NC
AH35	NC
AG35	NC
AR33	NC
AR34	NC
AN34	NC
AM34	NC
AK34	NC
AJ34	NC
AG34	NC
AF34	NC
AE33	NC
AE32	NC
AR18	NC
AR19	NC
AR21	NC
AR22	NC
AP26	NC
AP27	NC
AP29	NC
AP30	NC
AP20	NC
AP21	NC
AP23	NC

OSM Pins	Signal
AP24	NC
AR27	NC
AR28	NC
AR30	NC
AR31	NC
AN32	NC
AN31	NC
AL3	NC
AL4	NC
AM3	NC
AM4	NC
AM5	NC
AM6	NC
AM7	NC
AM8	NC
AM9	NC
AM10	NC
AM23	NC
AM24	NC
AM25	NC
AM26	NC
AM27	NC
AM28	NC
AM29	NC
AM30	NC
AM31	NC
AN2	NC
AN5	NC
AN7	NC
AN8	NC
AN24	NC
AN25	NC
AN26	NC
AN27	NC
AN28	NC
AN29	NC
AN30	NC
AP10	NC
AE4	VCC_IN_5V
AF4	VCC_IN_5V
AG4	VCC_IN_5V

OSM Pins	Signal
AH3	VCC_IN_5V
AH4	VCC_IN_5V
AJ3	VCC_IN_5V
AJ4	VCC_IN_5V
AK4	VCC_IN_5V
AK32	MIPI_CSI2_CLK_N
AK33	MIPI_CSI2_CLK_P
AL32	MIPI_CSI2_D0_N
AL33	MIPI_CSI2_D0_P
AM32	MIPI_CSI2_D1_N
AM33	MIPI_CSI2_D1_P

** Optional feature, by default not supported.*

2.7.1 RGMII Interface

The i.MX 8M Plus OSM LGA Module supports two RGMII interface. i.MX 8M Plus provides two Ethernet Interfaces ENET and ENET_QOS with TSN support. The two RGMII lanes are connected to OSM LGA. Connection of the i.MX 8M Plus to the world wide web or a local area network (LAN) is possible using the GbE PHY which is off the module. The PHY can be selected which operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

For more details on ENET_QOS pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
H15	ETH_A_(S)(R)(G)MII_TXD0	ENET_QOS_RGMII_TD0	ENET_TD0/AC25	O 1.8V CMOS/0E Series	Transmit data bit 0 (transmitted first) port A
G15	ETH_A_(S)(R)(G)MII_TXD1	ENET_QOS_RGMII_TD1	ENET_TD1/AE26	O 1.8V CMOS/0E Series	Transmit data bit 1 port A
H16	ETH_A_(R)(G)MII_TXD2	ENET_QOS_RGMII_TD2	ENET_TD2/ AF26	O 1.8V CMOS/0E Series	Transmit data bit 2 port A
G16	ETH_A_(R)(G)MII_TXD3	ENET_QOS_RGMII_TD3	ENET_TD3/ AD24	O 1.8V CMOS/0E Series	Transmit data bit 3 port A
K16	ETH_A_(R)(G)MII_TX_EN(_ER)	ENET_QOS_RGMII_TX_CTL	ENET_TX_CTL/ AF24	O 1.8V CMOS/0E Series	Transmit enable (Error) port A
J15	ETH_A_(R)(G)MII_TX_CLK	ENET_QOS_RGMII_TXC	ENET_TXC/ AE24	O 1.8V CMOS/0E Series	Transmit clock port A
K15	ETH_A_(S)(R)(G)MII_RXD0	ENET_QOS_RGMII_RD0	ENET_RD0/AG29	I 1.8V CMOS	Receive data bit 0 (received first) port A
L15	ETH_A_(S)(R)(G)MII_RXD1	ENET_QOS_RGMII_RD1	ENET_RD1/AG28	I 1.8V CMOS	Receive data bit 1 port A
N15	ETH_A_(R)(G)MII_RXD2	ENET_QOS_RGMII_RD2	ENET_RD2/AF29	I 1.8V CMOS	Receive data bit 2 port A
P15	ETH_A_(R)(G)MII_RXD3	ENET_QOS_RGMII_RD3	ENET_RD3/AF28	I 1.8V CMOS	Receive data bit 3 port A
M15	ETH_A_(R)(G)MII_RX_DV(_ER)	ENET_QOS_RGMII_RX_CTL	ENET_RX_CTL/AE28	I 1.8V CMOS	Receive data valid port A
R15	ETH_A_(R)(G)MII_RX_CLK	ENET_QOS_RGMII_RXC	ENET_RXC/AE29	I 1.8V CMOS	Receive clock port A
T15	ETH_MDIO	ENET_QOS_MDIO	ENET_MDIO/AH29	I/O 1.8V CMOS	Management data
T16	ETH_MDC	ENET_QOS_MDC	ENET_MDC/AH28	O 1.8V CMOS/0E Series	Management data clock
B22	VENDOR DEFINED1	NC	NA	O, 1.8V/3.3V	ENET IO Voltage is optionally connected.

For more details on ENET pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
G1	ETH_B_(S)(R)(G)MII_TXD0	ENET1_RGMII_TD0(SAI1_TXD0)	SAI1_TXD0/ AJ11	O 1.8V CMOS/0E Series	Transmit data bit0 (transmitted first) port B
F1	ETH_B_(S)(R)(G)MII_TXD1	ENET1_RGMII_TD1(SAI1_TXD1)	SAI1_TXD1/AJ10	O 1.8V CMOS/0E Series	Transmit data bit1 port B
G2	ETH_B_(R)(G)MII_TXD2	ENET1_RGMII_TD2(SAI1_TXD2)	SAI1_TXD2/ AH11	O 1.8V CMOS/0E Series	Transmit data bit 2 port B
F2	ETH_B_(R)(G)MII_TXD3	ENET1_RGMII_TD3(SAI1_TXD3)	SAI1_TXD3/ AD12	O 1.8V CMOS/0E Series	Transmit data bit 3 port B
H1	ETH_B_(R)(G)MII_TX_CLK	ENET1_RGMII_TXC(SAI1_TXD5)	SAI1_TXD5/ AH14	O 1.8V CMOS/0E Series	Transmit clock port B
J2	ETH_B_(R)(G)MII_TX_EN(_ER)	ENET1_RGMII_TX_CTL(SAI1_TXD4)	SAI1_TXD4/AH13	O 1.8V CMOS/0E Series	Transmit enable (Error) port B
J1	ETH_B_(S)(R)(G)MII_RXD0	ENET1_RGMII_RD0(SAI1_RXD4)	SAI1_RXD4/AD10	I 1.8V CMOS	Receive data bit 0 (received first) port B
K1	ETH_B_(S)(R)(G)MII_RXD1	ENET1_RGMII_RD1(SAI1_RXD5)	SAI1_RXD5/AE10	I 1.8V CMOS	Receive data bit1 port B
M1	ETH_B_(R)(G)MII_RXD2	ENET1_RGMII_RD2(SAI1_RXD6)	SAI1_RXD6/AH10	I 1.8V CMOS	Receive data bit 2 port B
N1	ETH_B_(R)(G)MII_RXD3	ENET1_RGMII_RD3(SAI1_RXD7)	SAI1_RXD7/AH12	I 1.8V CMOS	Receive data bit 3 port B
P1	ETH_B_(R)(G)MII_RX_CLK	ENET1_RGMII_RXC(SAI1_TXC)	SAI1_TXC/AJ12	I 1.8V CMOS	Receive clock port B
L1	ETH_B_(R)(G)MII_RX_DV(_ER)	ENET1_RGMII_RX_CTL(SAI1_TXFS)	SAI1_TXFS /AF12	I 1.8V CMOS	Receive data valid port B
C7	VENDOR DEFINED5	ENET1_MDIO(SAI1_RXD3)	SAI1_RXD3 /AJ8	I/O 1.8V CMOS/0E Series	Management data
C6	VENDOR DEFINED4	ENET1_MDC(SAI1_RXD2)	SAI1_RXD2/AH9	O 1.8V CMOS/0E Series	Management data clock

2.7.2 USB3.0 OTG Interface

The i.MX 8M Plus SoC supports two USB controllers and PHYs that support USB 3.0, which can operate in 2.0 mode.

The i.MX 8M Plus OSM LGA Module supports one USB 3.0 OTG interface. i.MX 8M Plus SoC's USB1 controller is used for USB 3.0 OTG interface and directly connected to USB_C of OSM. This USB3.0 OTG is compliant with the Universal Serial Bus (USB) 3.0 Specifications which supports USB dual-role operation and can be configured as host or device. It supports Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps).

For more details on USB pinouts near OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
C9	USB_C_VBUS	VBUS_OTG1	USB1_VBUS/A11	5V, Power	USB 3.0 OTG VBUS power for detection. *Note: Same power is also connected to 10thpin of Programming Header*
A8	USB_C_SSTX_P	USB1_TX_P	USB1_TX_P/A10	O, USB SS/0E	USB 3.0 OTG Super Speed Transmit Positive. *Should be AC coupled off module.*
A9	USB_C_SSTX_N	USB1_TX_N	USB1_TX_N/B10	O, USB SS/0E	USB 3.0 OTG Super Speed Transmit Negative. *Should be AC coupled off module.*
B10	USB_C_SSRX_P	USB1_RX_P	USB1_RX_P/A9	I, USB SS	USB 3.0 OTG Super Speed Receive Positive. *Should be AC coupled off module.*
B11	USB_C_SSRX_N	USB1_RX_N	USB1_RX_N/B9	I, USB SS	USB 3.0 OTG Super Speed Receive Negative. *Should be AC coupled off module.*
D10	USB_C_D_P	USB_OTG1_DP	USB1_D_P/D10	IO, USB	USB 2.0 OTG Data Positive. *Note: Same signal is also connected to 8thpin of Programming Header*
D11	USB_C_D_N	USB_OTG1_DM	USB1_D_N/E10	IO, USB	USB 2.0 OTG Data Negative. *Note: Same signal is also connected to 7thpin of Programming Header*

2.7.3 USB3.0 Host Interface

The i.MX 8M Plus OSM LGA Module supports one USB 3.0 Host interface on OSM LGA. i.MX 8M Plus SoC's USB OTG2 controller with integrated USB3.0 MAC and PHY is used for USB3.0 Host interface and directly connected to USB_D of OSM LGA. This USB3.0 OTG controller is compliant with the Universal Serial Bus (USB) 3.0 Specifications which supports

USB dual-role operation but configured as host only to match the OSM specification of USB2 port. It supports Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps).

To support USB 2.0 Host interface on this USB3.0 Host interface port, i.MX 8M Plus SoC's USB OTG2 controller with integrated USB 2.0 MAC and PHY is used. This USB2.0 PHY output is connected to USB_D port of OSM LGA through four-port USB hub "USB2514" from Microchip. The Hub is used to support more USB2.0 Host Ports on OSM LGA.

For more details on USB 3.0 Host pinouts, refer the below table.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D26	USB_D_D_N	USB_HUB1OUT_DM	NA	IO, USB	USB 2.0 Data Positive. *Note: This pin is connected from 4port USB Hub Out1.*
D25	USB_D_D_P	USB_HUB1OUT_DP	NA	IO, USB	USB 2.0 Port2 Data Negative. *Note: This pin is connected from 4port USB Hub Out1.*
C28	USB_D_OC#	USB_HUB1_OC	NA	I, OD 3.3V CMOS/10K PU	Over Current Indicator. *Note: This pin is connected to USB Hub.*
C26	USB_D_EN	USB_HUB1OUT_PWR_EN	NA	O, 3.3V CMOS	USB Power Enable. *Note: This pin is connected to USB Hub.*
A27	USB_D_SSTX_P	USB2_TX_P	USB2_TX_P/ A13	O, USB SS/0E	USB 3.0 Port 2 Transmit Positive. *Should be AC coupled off module.*
A28	USB_D_SSTX_N	USB2_TX_N	USB2_TX_N/ B13	O, USB SS/0E	USB 3.0 Port 2 Transmit Negative. *Should be AC coupled off module.*
B25	USB_D_SSRX_P	USB2_RX_P	USB2_RX_P/ A12	I, USB SS	USB 3.0 Port2 Receive Positive. *Should be AC coupled off module.*
B26	USB_D_SSRX_N	USB2_RX_N	USB2_RX_N/ B12	I, USB SS	USB 3.0 Port2 Receive Negative. *Should be AC coupled off module.*

2.7.4 USB 2.0 Host Interface

The i.MX 8M Plus OSM LGA Module supports three USB2.0 Host interface on OSM LGA. To support USB2.0 Host interfaces, module includes four-port USB hub "USB2514" from Microchip. This Hub is interfaced with i.MX 8M Plus SoC using USB OTG2 controller (with integrated PHY) which supports USB2.0 High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) transfer. This Hub output is directly connected to USB_A, USB_B port, USB_D and Vendor defined pins of OSM LGA.

For more details on USB 2.0 Host pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC14	USB_A_D_P	USB_HUB2OUT_DP	NA	IO, USB	USB 2.0 PortA Data Positive. *Note: This pin is connected from 4port USB Hub Out2.*
AB13	USB_A_D_N	USB_HUB2OUT_DM	NA	IO, USB	USB 2.0 PortA Data Negative. *Note: This pin is connected from 4port USB Hub Out2.*
AC15	USB_A_OC#	USB_HUB2_OC	NA	I, OD CMOS/ 10K PU	USB 2.0 PortA Over Current Indicator. *Note: This pin is connected to USB Hub.*
AC16	USB_A_EN	USB_HUB2OUT_PWR_EN	NA	O, 3.3V CMOS	USB Power Enable for PortA. *Note: This pin is connected to USB Hub.*
AB23	USB_B_D_N	USB_HUB3OUT_DM	NA	IO, USB	USB 2.0 PortBData Negative. *Note: This pin is connected from 4port USB Hub Out3.*
AC22	USB_B_D_P	USB_HUB3OUT_DP	NA	IO, USB	USB 2.0 PortB Data Positive. *Note: This pin is connected from 4port USB Hub Out3.*
AC21	USB_B_OC#	USB_HUB3_OC	NA	I, OD CMOS / 10K PU	USB 2.0 PortB Over Current Indicator. *Note: This pin is connected to USB Hub OCS3 pin.*
AC20	USB_B_EN	USB_HUB3OUT_PWR_EN	NA	O, 3.3V CMOS/10K PU	USB Power Enable for PortB. *Note: This pin is connected to USB Hub.*
Y29	Vendor Defined8	USB_HUB4OUT_DP	NA	IO, USB	USB 2.0 Data Positive. *Note: This pin is connected from 4port USB Hub Out4.*
AA29	Vendor Defined11	USB_HUB4OUT_DM	NA	IO, USB	USB 2.0 Data Negative. *Note: This pin is connected from 4port USB Hub Out4.*

2.7.5 PCIe Interface

The i.MX 8M Plus OSM LGA Module supports one PCIe Gen3 lane on OSM LGA. i.MX 8M Plus SoC supports one single lane PCIe Gen3 with integrated PHY and Dual Mode operation to function as root complex or endpoint and is directly connected to PCIe Link A port of OSM LGA. By default, internal PCIe reference clock is used. 100MHz external clock

oscillator output option is also available connected to SoC and OSM LGA for PCIe reference clock. Also, PCIe reset and PCIe wake are supported on OSM LGA from i.MX 8M Plus SoC IOs GPIO1_12 and GPIO1_14 respectively.

Note: When using PCIe differential clock lines from external clock oscillator no external termination is required as they are having On-OSM termination resistors.

For more details on PCIe pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB1	PCIE_A_HSI0_P	PCIE_RXN_P	PCIE_RXN_P/ A14	I, PCIe	PCIe Channel-A Receive Positive.
AB2	PCIE_A_HSI0_N	PCIE_RXN_N	PCIE_RXN_N/B 14	I, PCIe	PCIe Channel-A Receive Negative.
AC2	PCIE_A_HSO0_P	PCIE_TXN_P	PCIE_TXN_P/A 15	O, PCIe/0E	PCIe Channel-A Transmit Positive.
AC3	PCIE_A_HSO0_N	PCIE_TXN_N	PCIE_TXN_N/B 15	O, PCIe /0E	PCIe Channel-A Transmit Negative.
W1	PCIE_REFCLK_P	PCIE_REFCLK_DP	PCIE_REF_PAD _CLK_P/D16	O, PCIe	PCIe Channel-A Clock Positive. *Note: Internal Reference clock.*
Y1	PCIE_REFCLK_N	PCIE_REFCLK_DM	PCIE_REF_PAD _CLK_N/E16	O, PCIe	PCIe Channel-A Clock Negative. *Note: Internal Reference clock.*
V2	PCIE_A_PERST#	OSM_PCIE_RST	GPIO1_IO12/A 5	O, 3.3V CMOS	PCIe Channel-A Reset Out.
R2	PCIE_SM_ALERT#	GPIO_PCIe_SM_A LERT#(SAI3_MCLK _GPIO5_02)	SAI3_MCLK/AJ 20	I, OD CMOS/ 10K PU	SMBus Alert# (interrupt) signal.
T2	PCIE_WAKE#	OSM_PCIe_Wake	GPIO1_IO14/A 4	I, 3.3V CMOS/ 10K PU	PCIe wake up interrupt to host.
W2	PCIE_A_PRSNT#	OSM_PCIE_PRST	NA	I, 3.3V CMOS/ 10K PU	PCIe Port A present input

2.7.6 MIPI CSI Interface

The i.MX 8M Plus SoC supports two 4-lane camera interfaces, the CSI-2 Rx Controller Core is compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The i.MX 8M Plus OSM LGA Module supports 4 lane MIPI CSI camera interface along with the other controlling signals. Here all CSI2 lane [3:0] are connected to OSM LGA through vendor defined pins.

For more details on MIPI CSI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
C1	CSI_DATA0_N	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N/E18	I, MIPI	MIPI CSI1 differential data lane 0 negative.
B1	CSI_DATA0_P	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P/D18	I, MIPI	MIPI CSI1 differential data lane 0 positive.
A2	CSI_DATA1_N	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N/E20	I, MIPI	MIPI CSI1 differential data lane 1 negative.
A3	CSI_DATA1_P	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P / D20	I, MIPI	MIPI CSI1 differential data lane 1 positive.
A5	CSI_DATA2_N	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N / E24	I, MIPI	MIPI CSI1 differential data lane 2negative.
A6	CSI_DATA2_P	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P/D24	I, MIPI	MIPI CSI1 differential data lane 2 positive.
B6	CSI_DATA3_N	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N/E26	I, MIPI	MIPI CSI1 differential data lane 3 negative.
B7	CSI_DATA3_P	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P/D26	I, MIPI	MIPI CSI1 differential data lane 3 positive.
B3	CSI_CLOCK_N	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ E22	I, MIPI	MIPI CSI1 differential Clock negative.
B4	CSI_CLOCK_P	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/ D22	I, MIPI	MIPI CSI1 differential Clock positive.
C2	CAM_MCK	CAMERA_CCMCLKO1(ECSPI2_MISO)	ECSPI2_MISO/AH20	O, 1.8V CMOS	Master Clock for Camera.
C3	I2C_CAM_SDA / CSI_TX_N	I2C3_SDA	I2C3_SDA/AJ6	IO, 1.8V CMOS/ 4.7K PU	MIPI CSI1 I2C Data.
C4	I2C_CAM_SCL / CSI_TX_P	I2C3_SCL	I2C3_SCL/AJ7	IO, 1.8V CMOS/ 4.7K PU	MIPI CSI1 I2C Clock.

For more details on MIPI CSI2 OSM pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AL32	Vendor Defined16	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N/ B25	I, MIPI	MIPI CSI2 differential data lane 0 negative.
AL33	Vendor Defined17	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P/ A25	I, MIPI	MIPI CSI2 differential data lane 0 positive.
AM32	Vendor Defined18	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N/ B24	I, MIPI	MIPI CSI2 differential data lane 1 negative.
AM33	Vendor Defined19	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P/ A24	I, MIPI	MIPI CSI2 differential data lane 1 positive.
Y30	Vendor Defined9	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N/ B22	I, MIPI	MIPI CSI2 differential data lane 2negative.
Y31	Vendor Defined10	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P/ A22	I, MIPI	MIPI CSI2 differential data lane 2 positive.
AA30	Vendor	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N/	I, MIPI	MIPI CSI2 differential data

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
	Defined12		B21		lane 3 negatives.
AA31	Vendor Defined13	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P/ A21	I, MIPI	MIPI CSI2 differential data lane 3 positive.
AK32	Vendor Defined14	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N /B23	I, MIPI	MIPI CSI1 differential Clock negative.
AK33	Vendor Defined15	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P /A23	I, MIPI	MIPI CSI1 differential Clock positive.

2.7.7 HDMI TX Interface

The i.MX 8M Plus OSM LGA Module supports one HDMI Interface on OSM LGA. It supports dedicated DDC interface on OSM LGA for HDMI EDID read and to carry the HDCP and SCDC commands. i.MX 8M Plus SoC supports HDMI 2.0a Specification. The SoC inbuilt PHY also supports 32 channel audio output support. The HDMI TX PHY of the i.MX 8M Plus SoC supports video pixel rated from 25MHz up to 297MHz.

For more details on HDMI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A30	eDP_A_LANE0_P	HDMI_TX_D2_P	HDMI_TX2_P/AH 27	O, HDMI	HDMI differential data lane 2 Positive
A31	eDP_A_LANE0_N	HDMI_TX_D2_N	HDMI_TX2_N/AJ2 7	O, HDMI	HDMI differential data lane 2 Negative
B31	eDP_A_LANE1_P	HDMI_TX_D1_P	HDMI_TX1_P/AH 26	O, HDMI	HDMI differential data lane 1 Positive
B32	eDP_A_LANE1_N	HDMI_TX_D1_N	HDMI_TX1_N/AJ2 6	O, HDMI	HDMI differential data lane 1 Negative
A33	eDP_A_LANE2_P	HDMI_TX_D0_P	HDMI_TX0_P/AH 25	O, HDMI	HDMI differential data lane 0 Positive
A34	eDP_A_LANE2_N	HDMI_TX_D0_N	HDMI_TX0_N/AJ2 5	O, HDMI	HDMI differential data lane 0 Negative
B34	eDP_A_LANE3_P	HDMI_TX_CLK_P	HDMI_TXC_P/AH 24	O, HDMI	HDMI differential CLK Positive
B35	eDP_A_LANE3_N	HDMI_TX_CLK_N	HDMI_TXC_N/AJ2 4	O, HDMI	HDMI differential CLK Negative
D33	eDP_A_BL_HPD	HDMI_TX_HPD	HDMI_HPD/AE22	I, 1.8V CMOS/ 1M PD	HDMI Hot Plug Detect
C33	eDP_A_AUX_P	HDMI_TX_DDC_S CL	HDMI_DDC_SCL/ AC22	IO, 1.8V CMOS/100K PU	HDMI DDC I2C Clock
C34	eDP_A_AUX_N	HDMI_TX_DDC_S DA	HDMI_DDC_SDA/ AF22	IO, 1.8V CMOS/100K PU	HDMI DDC I2C Data
C31	eDP_A_BL_PWM	HDMI_TX_CEC	HDMI_CEC/AD22	O,1.8V CMOS	CEC lane

2.7.8 LVDS Display Interface

OSM Specification supports two LVDS display interfaces over LGA, which are present in size L. The i.MX 8M Plus SoC supports two LVDS display channels. Each channel has one clock pair and four data pairs. For 4-lane LVDS, channel 0 or channel 1 can be used.

For more details on LVDS0 and LVDS1 pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AN13	LVDS_A_CLK_P	LVDS0_CLK_P	LVDS0_CLK_P/F29	O, LVDS	LVDS0 differential Clock positive
AN12	LVDS_A_CLK_N	LVDS0_CLK_N	LVDS0_CLK_N/G28	O, LVDS	LVDS0 differential Clock negative
AP18	LVDS_A_LANE0_P	LVDS0_D0_P	LVDS0_D0_P/D29	O, LVDS	LVDS0 differential data lane 0 positive
AP17	LVDS_A_LANE0_N	LVDS0_D0_N	LVDS0_D0_N/E28	O, LVDS	LVDS0 differential data Lane 0 negative
AR16	LVDS_A_LANE1_P	LVDS0_D1_P	LVDS0_D1_P/E29	O, LVDS	LVDS0 differential data lane 1 positive
AR15	LVDS_A_LANE1_N	LVDS0_D1_N	LVDS0_D1_N/F28	O, LVDS	LVDS0 differential data lane 1 negative
AP15	LVDS_A_LANE2_P	LVDS0_D2_P	LVDS0_D2_P/G29	O, LVDS	LVDS0 differential data lane 2 positive
AP14	LVDS_A_LANE2_N	LVDS0_D2_N	LVDS0_D2_N/H28	O, LVDS	LVDS0 differential data lane 2 negative
AP12	LVDS_A_LANE3_P	LVDS0_D3_P	LVDS0_D3_P/H29	O, LVDS	LVDS0 differential data lane 3 positive
AP11	LVDS_A_LANE3_N	LVDS0_D3_N	LVDS0_D3_N/J28	O, LVDS	LVDS0 differential data lane 3 negative
AN17	LVDS_B_CLK_P	LVDS1_CLK_P	LVDS1_CLK_P/A28	O, LVDS	LVDS1 differential Clock positive
AN16	LVDS_B_CLK_N	LVDS1_CLK_N	LVDS1_CLK_N/B28	O, LVDS	LVDS1 differential Clock negative
AM21	LVDS_B_LANE0_P	LVDS1_D0_P	LVDS1_D0_P/A26	O, LVDS	LVDS1 differential data lane 0 positive
AM20	LVDS_B_LANE0_N	LVDS1_D0_N	LVDS1_D0_N/B26	O, LVDS	LVDS1 differential data Lane 0 negative
AN20	LVDS_B_LANE1_P	LVDS1_D1_P	LVDS1_D1_P/A27	O, LVDS	LVDS1 differential data lane 1 positive
AN19	LVDS_B_LANE1_N	LVDS1_D1_N	LVDS1_D1_N/B27	O, LVDS	LVDS1 differential data lane 1 negative
AM18	LVDS_B_LANE2_P	LVDS1_D2_P	LVDS1_D2_P/ B29	O, LVDS	LVDS1 differential data lane 2 positive
AM17	LVDS_B_LANE2_N	LVDS1_D2_N	LVDS1_D2_N/ C28	O, LVDS	LVDS1 differential data lane 2 negative
AM15	LVDS_B_LANE3_P	LVDS1_D3_P	LVDS1_D3_P/ C29	O, LVDS	LVDS1 differential data lane 3 positive
AM14	LVDS_B_LANE3_N	LVDS1_D3_N	LVDS1_D3_N/	O, LVDS	LVDS1 differential data lane

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
			D28		3 negative
AN14	LVDS_VDD_EN	LCD0_VDD_EN (NAND_DATA02_GPIO3_8)	NAND_DATA02/ L24	O, 1.8V CMOS	LCD Power Enable
AN23	LVDS_BL_EN	LCD0_BKLT_EN(NAND_DATA01_GPIO3_7)	NAND_DATA01/ L25	O, 1.8V CMOS	LCD Backlight Enable
AN22	LVDS_BL_PWM	PWM2_OUT(SAI5_RXD0)	SAI5_RXD0/ AE16	O, 1.8V CMOS	LCD Back Light Brightness control PWM
AM11	LVDS_I2C_CLK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/ AE18	O, OD 1.8V CMOS/ 4.7K PU	I2C CLK
AM12	LVDS_I2C_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/ AD18	IO, OD 1.8V CMOS/ 4.7K PU	I2C Data

2.7.9 MIPI DSI Interface

The i.MX 8M Plus OSM LGA Module supports one 4-lane MIPI DSI display. Maximum resolution ranges up to WQHD (2560x1440). The MIPI D-PHY core IP is a flexible, low power and high-speed serial interface that connects a display driver or a camera sensor to a host processor. The D-PHY provides a synchronous connection between Master and Slave with clock signal originating at the Master and terminating at the Slave. The main operation modes are HS mode (High Speed Mode) and LP mode (Low Power Mode). The D-PHY is v1.2 spec compatible.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB11	DSI_DATA0_N	MIPI_DSI0_D0_N	MIPI_DSI1_D0_N/ B16	O, MIPI	DSI differential output
AB10	DSI_DATA0_P	MIPI_DSI0_D0_P	MIPI_DSI1_D0_P/ A16	O, MIPI	DSI differential output
AC9	DSI_DATA1_N	MIPI_DSI0_D1_N	MIPI_DSI1_D1_N/ B17	O, MIPI	DSI differential output
AC8	DSI_DATA1_P	MIPI_DSI0_D1_P	MIPI_DSI1_D1_P/ A17	O, MIPI	DSI differential output
AC6	DSI_DATA2_N	MIPI_DSI0_D2_N	MIPI_DSI1_D2_N/ B19	O, MIPI	DSI differential output
AC5	DSI_DATA2_P	MIPI_DSI0_D2_P	MIPI_DSI1_D2_P/ A19	O, MIPI	DSI differential output
AB5	DSI_DATA3_N	MIPI_DSI0_D3_N	MIPI_DSI1_D3_N/ B20	O, MIPI	DSI differential output
AB4	DSI_DATA3_P	MIPI_DSI0_D3_P	MIPI_DSI1_D3_P/ A20	O, MIPI	DSI differential output
AB8	DSI_CLOCK_N	MIPI_DSI0_CLK_N	MIPI_DSI1_CLK_N /B18	O, MIPI	DSI differential output
AB7	DSI_CLOCK_P	MIPI_DSI0_CLK_P	MIPI_DSI1_CLK_P /A18	O, MIPI	DSI differential output

2.7.10 Audio Interface

The i.MX 8M Plus OSM LGA Module supports I2S_A of OSM LGA from SoC's SAI2 channel. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including transmitter with independent bit clock and frame sync, each date line can support a maximum frame size of 32 words, Word size from 8-bits to 32-bits and supports 49.152 MHz BCLK. Only Transmitter Clock and Transmitter Left-Right Clock (LRCK) is supported as per OSM specification.

In i.MX 8M Plus OSM LGA Module the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on Audio interface pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
V18	I2S_MCLK	SAI2_MCLK	SAI2_MCLK/ AJ15	O, 1.8V CMOS/33E Series	Master Clock for Audio codec
W21	I2S_A_DATA_OUT	SAI2_TX_DATA0(SAI2_TXD0)	SAI2_TXD0/ AH16	O, 1.8V CMOS	Serial Audio Interface Data Output
V21	I2S_A_DATA_IN	SAI2_RX_DATA0(SAI2_RXD0)	SAI2_RXD0/ AJ14	I, 1.8V CMOS	Serial Audio Interface Data Input
W20	I2S_BITCLK	SAI2_TX_BCLK(SAI2_TXC)	SAI2_TXC/ AH15	IO, 1.8V CMOS/ 33E Series	Serial Audio Interface Clock
W18	I2S_LRCLK	SAI2_TX_SYNC(SAI2_TXFS)	SAI2_TXFS/AJ17	O, 1.8V CMOS	Serial Audio Interface Frame Sync

2.7.11 SPI Interface

The i.MX 8M Plus SoC supports Enhanced Configurable Serial Peripheral Interface (ECSPI) module that supports an efficient interface to an SPI bus as a master/slave with maximum data rate of 52 Mbits/s. The i.MX 8M Plus OSM LGA Module supports SPI0 and SPI1 channels of the OSM using ECSPI1 and ECSPI2 of SoC.

For more details on SPI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y15	SPI_A_CS#	ECSPI1_SS0	ECSPI1_SS0/ AE20	O, 1.8V CMOS	SPI1 Chip Select 0 *Note: 10K pullup option is provided.*
U16	SPI_A_SCK	ECSPI1_SCLK	ECSPI1_SCLK/ AF20	O, 1.8V CMOS/ 33E Series	SPI1 Clock
U15	SPI_A_SDI_(IO0)	ECSPI1_MISO	ECSPI1_MISO/ AD20	I, 1.8V CMOS	SPI1 Master IN Slave Out

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
V15	SPI_A_SDO_(IO1)	ECSPI1_MOSI	ECSPI1_MOSI/ AC20	O, 1.8V CMOS	SPI1 Master Out Slave In
AA23	SPI_B_CS#	ECSPI2_SS0	ECSPI2_SS0/ AJ22	O, 1.8V CMOS	SPI2 Chip Select 0 *Note: 10K pullup option is provided*.
Y21	SPI_B_SCK	ECSPI2_SCLK	ECSPI2_SCLK/ AH21	O, 1.8V CMOS/ 33E Series	SPI2 Clock
Y22	SPI_B_SDI	ECSPI2_MISO(I2C4_SCL)	I2C4_SCL/ AF8	I, 1.8V CMOS	SPI2 Master IN Slave Out
Y23	SPI_B_SDO	ECSPI2_MOSI	ECSPI2_MOSI/ AJ21	O, 1.8V CMOS	SPI2 Master Out Slave In

2.7.12 Data UART

OSM V1.0 supports five UART channels where two channels UART_A and UART_B are with CTS and RTS and two channels UART_C and UART_D are without and a console UART port. UART2 and UART3 from i.MX 8M Plus SoC is connected to UART_A and UART_C channels of OSM LGA respectively. Whereas UART1 of i.MX 8M Plus SoC is optionally connected to UART B channel of OSM LGA. In default configuration UART1 is connected to on OSM Bluetooth module. UART4 is the debug UART and connected to UART Console port of OSM.

For more details on UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A14	UART_A_RX	UART2_RXD	UART2_RXD/AF6	I, 1.8V CMOS	UART2 Receiver.
B13	UART_A_TX	UART2_TXD	UART2_TXD/AH4	O, 1.8V CMOS	UART2 Transmitter.
C13	UART_A_RTS	UART2_CTS_B(SAI3_RXC)	SAI3_RXC/AJ18	O, 1.8V CMOS	UART2 Clear to Send.
C14	UART_A_CTS	UART2_RTS_B(SAI3_RXD)	SAI3_RXD/AF18	I, 1.8V CMOS	UART2 Request to Send.
A22	UART_C_RX	UART3_RX(NAND_ALE)	NAND_ALE/N25	I, 1.8V CMOS	UART3 Receiver.
B23	UART_C_TX	UART3_TX(NAND_CE0_B)	NAND_CE0_B/L26	O, 1.8V CMOS	UART3 Transmitter.
D22	UART_CON_RX	UART4_RXD	UART4_RXD/AJ5	I, 1.8V CMOS	Debug UART Transmitter. *Also connected to 12th pin of on-OSM programming header.*
D23	UART_CON_TX	UART4_TXD	UART4_TXD/AH5	O, 1.8V CMOS	Debug UART Receiver. *Also connected to 13th pin of on-OSM programming header.*

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D14	UART_B_RX	NC	UART1_RXD/AD6	I, 1.8V CMOS	NC. *Note: By default, connected to on- OSM Bluetooth module. Optionally connected to OSM.*
D13	UART_B_TX	NC	UART1_TXD/AJ3	O, 1.8V CMOS	NC. *Note: By default, connected to on- OSM Bluetooth module. Optionally connected to OSM.*
D15	UART_B_RTS	NC	UART3_RXD/AE6	O, 1.8V CMOS	NC. *Note: By default, connected to on- OSM Bluetooth module. Optionally connected to OSM.*
D16	UART_B_CTS	NC	UART3_TXD/AJ4	I,1.8V CMOS	NC. *Note: By default, connected to on- OSM Bluetooth module. Optionally connected to OSM.*

2.7.13 SD Interface

The i.MX 8M Plus OSM LGA Module supports 4bit SD and optionally supports 8-bit SD interface over OSM LGA which can be used to connect SD card as Mass storage or optional boot device. uSDHC2 controller of the i.MX 8M Plus SoC is used to support 4bit SD interface and uSDHC1 is used to optionally support 8bit SD interface. By default, uSDHC1 is used for on-SOM Wi-Fi module. uSDHC2 and uSDHC1 can operate in both 3.3V and 1.8V IO level and supports card bus clock frequency up to 208 MHz. The i.MX 8M Plus OSM supports configurable I/O voltage levels for USDHC1 and USDHC2 lines through GPIO1_IO03 and GPIO1_IO04 respectively. If the GPIO is set to low, then 3.3V IO level is selected and if the GPIO is set to high, then 1.8V IO level is selected. Controlling GPIOs like Write Protect and Card detect signals also operates at both 1.8V and 3.3V IO level.

For more details on SD pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
F21	SDIO_A_CLK	SD2_CLK	SD2_CLK/AB29	O, 1.8/3.3V, 33E Series	SD Clock *Note: 10K pullup option is provided.*
E20	SDIO_A_CMD	SD2_CMD	SD2_CMD/AB20	IO, 1.8/3.3V	SD command

				CMOS	*Note: 10K pullup option is provided.*
G20	SDIO_A_D0	SD2_DATA0	SD2_DATA0/AC28	IO, 1.8/3.3V CMOS	SD data 0 *Note: 10K pullup option is provided.*
G21	SDIO_A_D1	SD2_DATA1	SD2_DATA1/AC29	IO, 1.8/3.3V CMOS	SD data 1 *Note: 10K pullup option is provided.*
H20	SDIO_A_D2	SD2_DATA2	SD2_DATA2/AA26	IO, 1.8/3.3V CMOS	SD data 2 *Note: 10K pullup option is provided.*
H21	SDIO_A_D3	SD2_DATA3	SD2_DATA3/AA25	IO, 1.8/3.3V CMOS	SD data 3 *Note: 10K pullup option is provided.*
J21	SDIO_A_CD#	SD2_CD_B	SD2_CD_B/AD29	I, 1.8V/3.3V CMOS	SD Card Detect *Note: 10K pullup option is provided.*
D20	SDIO_A_WP	SD2_WP	SD2_WP/AC26	I, 1.8/3.3V CMOS	SD write protect *Note: 10K pullup option is provided.*
D21	SDIO_A_PWR_EN	SD2_PWR_EN(SD2_RESET_B_GPIO2_19)	SD2_RESET_B/AD28	O, 3.3V CMOS	SD Power enable *Note: 10K pullup option is provided.*
C20	SDIO_A_IOPWR	NVCC_SD2	NVCC_SD2/W24	Power 1.8/3.3V	SD IO Voltage
K20	SDIO_B_CLK	SD1_CLK	SD1_CLK/W28	O, 1.8/3.3V, 33E Series	SD Clock
K21	SDIO_B_CMD	SD1_CMD	SD1_CMD/W29	IO, 1.8/3.3V	SD command
L20	SDIO_B_D0	SD1_DATA0	SD1_DATA0/Y29	CMOS	SD data 0
L21	SDIO_B_D1	SD1_DATA1	SD1_DATA1/Y28	IO, 1.8/3.3V	SD data 1
M21	SDIO_B_D2	SD1_DATA2	SD1_DATA2/V29	CMOS	SD data 2
N20	SDIO_B_D3	SD1_DATA3	SD1_DATA3/V28	IO, 1.8/3.3V	SD data 3
N21	SDIO_B_D4	SD1_DATA4	SD1_DATA4/U26	CMOS	SD data 4
P20	SDIO_B_D5	SD1_DATA5	SD1_DATA5/AA29	IO, 1.8/3.3V	SD data 5
P21	SDIO_B_D6	SD1_DATA6	SD1_DATA6/AA28	CMOS	SD data 6
R21	SDIO_B_D7	SD1_DATA7	SD1_DATA7/U25	IO, 1.8/3.3V	SD data 7
T21	SDIO_B_CD#	SD1_CD#	SD1_RESET_B/W25	I, 1.8V/3.3V CMOS	SD Card Detect
U20	SDIO_B_WP	SD1_WP	SD1_STROBE/W26	I, 1.8V/3.3V CMOS	SD write protect

2.7.14 CAN Interface

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0B protocol specifications. The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames and long payloads.

The i.MX 8M Plus SoC Supports two CAN interface and both are connected to the OSM LGA.

For more details of CAN pinouts on OSM LGA, refer below table:

OSM Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC17	CAN_A_TX	FLEXCAN1_TX(SAI5_RXD1)	SAI5_RXD1/AD16	O, 1.8V CMOS	CAN 1 Transmitter.
AB17	CAN_A_RX	FLEXCAN1_RX(SAI5_RXD2)	SAI5_RXD2/AF16	I, 1.8V CMOS	CAN 1 Receiver.
AC19	CAN_B_TX	FLEXCAN2_TX(SAI5_RXD3)	SAI5_RXD3/AE14	O, 1.8V CMOS	CAN 2 Transmitter.
AB19	CAN_B_RX	FLEXCAN2_RX(SAI5_MCLK)	SAI5_MCLK/AF14	I, 1.8V CMOS	CAN 2 Receiver.

2.7.15 I2C Interface

OSM Specification V1.0 supports two general purpose I2C, one serial camera I2C, one for PCIe system management and one for LVDS. The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

For more details of I2C pinouts on OSM, refer below table:

OSM Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA15	I2C_A_SCL	I2C2_SCL	I2C2_SCL/AH6	O OD, 1.8V CMOS 4.7K PU	General Purpose I2C Clock. *Note: Also shared with PCIe SM Clock.*
AA16	I2C_A_SDA	I2C2_SDA	I2C2_SDA/AE8	IO OD, 1.8V CMOS 4.7K PU	General Purpose I2C Data. *Note: Also shared with PCIe SM Data.*
AA20	I2C_B_SCL	I2C1_SCL	I2C1_SCL/AC8	O OD, 1.8V CMOS 4.7K PU	General Purpose I2C Clock *Note: Also connected to PMIC (Addr: 0x25)*
AA21	I2C_B_SDA	I2C1_SDA	I2C1_SDA/AH7	IO OD, 1.8V CMOS 4.7K PU	General Purpose I2C Clock *Note: Also connected to PMIC (Addr: 0x25)*
C4	I2C_CAM_SCL / CSI_TX_P	I2C3_SCL	I2C3_SCL/AJ7	O OD, 1.8V CMOS 4.7K PU	Primary Camera I2C Clock. *Note: Also connected to on-OSM RTC Controller (Addr: 0x51)*
C3	I2C_CAM_SDA / CSI_TX_N	I2C3_SDA	I2C3_SDA/AJ6	IO, 1.8V CMOS 4.7K PU	Primary Camera I2C data. *Note: Also connected to on-OSM RTC Controller (Addr: 0x51)*
AM11	LVDS_I2C_CLK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/AE18	O OD, 1.8V CMOS 4.7K PU	LVDS I2C Clock.
AM12	LVDS_I2C_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/AD18	IO, 1.8V CMOS 4.7K PU	LVDS I2C data.
T1	PCIE_SMCLK	I2C2_SCL	I2C2_SCL/AH6	O OD, 1.8V CMOS	PCIe SM Clock.

				4.7K PU	*Note: Also shared with I2C_A_SCL*
U1	PCIE_SMDAT	I2C2_SDA	I2C2_SDA/AE8	IO OD, 1.8V CMOS 4.7K PU	PCIe SM Data. *Note: Also shared with I2C_A_SDA*

2.7.16 JTAG Interface

The i.MX 8M Plus OSM supports JTAG interface for SoC debug purpose. The Secure JTAG Controller (SJC) provides BSR (Boundary Scan Register) standard support, designed to be compatible with IEEE1149.1 and IEEE 1149.6 standards.

For more details on JTAG pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
N17	JTAG_TCK(SWCLK)	JTAG_TCK	JTAG_TCK/G18	I CMOS ,1V8	JTAG test Clock.
N19	JTAG_TMS(SWDIO)	JTAG_TMS	JTAG_TMS/G14	I CMOS ,1V8	JTAG test mode select.
P17	JTAG_TDI	JTAG_TDI	JTAG_TDI/G16	I CMOS ,1V8	JTAG test data input.
R17	JTAG_TDO(SWO)	JTAG_TDO	JTAG_TDO/F14	O CMOS ,1V8	JTAG test data output.
R19	JTAG_NTRST	JTAG_NTRST	POR_B/J29	I CMOS ,1V8/100K PU	Test Reset, Active Low
AC18	DEBUG_EN	NC	JTAG_MOD/G20	O CMOS ,1V8/10K PD	NC. JTAG mode selection pin.

2.7.17 OSM GPIOs

The i.MX 8M Plus OSM supports GPIOs on OSM LGA as per OSM V1.0. i.MX 8M Plus SoC's GPIO (general-purpose input/output) provides dedicated general-purpose pins that can be configured as either inputs or outputs.

For more details of GPIO pinouts on OSM, refer below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D17	GPIO_A_0	OSM_GPIO_A_0(SAI1_TXD6_GPIO4_18)	SAI1_TXD6/AC12	IO, 1.8V CMOS	OSM General Purpose Input/output A0.
E17	GPIO_A_1	OSM_GPIO_A_1(SAI1_TXD7_GPIO4_19)	SAI1_TXD7/AJ13	IO, 1.8V CMOS	OSM General Purpose Input/output A1.
F17	GPIO_A_2	OSM_GPIO_A_2(SAI1_RXFS_GPIO4_0)	SAI1_RXFS/AJ9	IO, 1.8V CMOS	OSM General Purpose Input/output A2.
G17	GPIO_A_3	OSM_GPIO_A_3(SAI1_RXC_GPIO4_1)	SAI1_RXC/AH8	IO, 1.8V CMOS	OSM General Purpose Input/output A3.
H17	GPIO_A_4	OSM_GPIO_A_4(SAI1_RXD0_GPIO4_2)	SAI1_RXD0/AC10	IO, 1.8V CMOS	OSM General Purpose Input/output A4.
J17	GPIO_A_5	OSM_GPIO_A_5(SAI5_RXC_GPIO3_20)	SAI5_RXC/AD14	IO, 1.8V CMOS	OSM General Purpose Input/output A5.
K17	GPIO_A_6	OSM_GPIO_A_6(SAI2_RXC_GPIO4_22)	SAI2_RXC/AJ16	IO, 1.8V CMOS	OSM General Purpose Input/output A6.
L17	GPIO_A_7	OSM_GPIO_A_7(SAI2_RXFS_GPIO4_21)	SAI2_RXFS/AH17	IO, 1.8V CMOS	OSM General Purpose Input/output A7.

D19	GPIO_B_0	OSM_GPIO_B_0(SAI3_RXFS_GPIO4_28)	SAI3_RXFS/AJ19	IO, 1.8V CMOS	OSM General Purpose Input/output B0.
E19	GPIO_B_1	OSM_GPIO_B_1(SAI1_RXD1_GPIO4_3)	SAI1_RXD1/AF10	IO, 1.8V CMOS	OSM General Purpose Input/output B1.
F19	GPIO_B_2	OSM_GPIO_B_2(SAI5_RXFS_GPIO3_21)	SAI5_RXFS/AC14	IO, 1.8V CMOS	OSM General Purpose Input/output B2.
G19	GPIO_B_3	OSM_GPIO_B_3(SPDIF1_EXT_CLK_GPIO5_5)	SPDIF_EXT_CLK/ AC18	IO, 1.8V CMOS	OSM General Purpose Input/output B3.
H19	GPIO_B_4	OSM_GPIO_B_4(NAND_DQS_GPIO3_21)	NAND_DQS/ R26	IO, 1.8V CMOS	OSM General Purpose Input/output B4.
J19	GPIO_B_5	OSM_GPIO_B_5(GPIO1_IO6)	GPIO1_IO06/ A3	IO, 1.8V CMOS	OSM General Purpose Input/output B5.
K19	GPIO_B_6	OSM_GPIO_B_6(GPIO1_IO00)	GPIO1_IO00/A7	IO, 1.8V CMOS	OSM General Purpose Input/output B6.
L19	GPIO_B_7	OSM_GPIO_B_7(GPIO1_IO9)	GPIO1_IO09/B8	IO, 1.8V CMOS	OSM General Purpose Input/output B7.
D3	GPIO_C_0	OSM_GPIO_C_0(GPIO1_IO7)	GPIO1_IO07/F6	IO, 1.8V CMOS	OSM General Purpose Input/output C0.
D4	GPIO_C_1	OSM_GPIO_C_1(GPIO1_IO11)	GPIO1_IO11/D8	IO, 1.8V CMOS	OSM General Purpose Input/output C1.
E3	GPIO_C_2	OSM_GPIO_C_2(SAI1_MCLK_GPIO4_20)	SAI1_MCLK/ AE12	IO, 1.8V CMOS/0E Series	OSM General Purpose Input/output C2.
G3	CAM_PWR / GPIO_C_6	OSM_GPIO_C_6(GPIO1_IO15)	GPIO1_IO15/B5	IO, 1.8V CMOS	OSM General Purpose Input/output C6. *Note: Optionally connected to PCIE_CLKREQ# of on-OSM Wi-F/BT Module.*
G4	CAM_RST# / GPIO_C_7	OSM_GPIO_C_7(GPIO1_IO10)	GPIO1_IO10/B7	IO, 1.8V CMOS	OSM General Purpose Input/output C7.

2.7.18 Control Signals

OSM V1.0 specification supports control Signals, for more details on OSM Control Signals pinouts on OSM LGA, refer below table:

OSM Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U17	SYS_RST#	PMIC_RST_B	NA	I, 1.8V CMOS/ 100K PU	Hard RESET Input to OSM.
AA9	PWR_BTN#	CPU_ON_OFF	ONOFF/ G22	I, 1.8V CMOS/ 100K PU	Power ON /OFF Input to OSM.
V17	CARRIER_PWR_EN	CARRIER_PWR_ON	NA	O, 1.8V CMOS/ 8.2K PU, 10K PD	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.

2.7.19 Boot Select

The i.MX 8M Plus OSM LGA Module supports one Boot Select pins as per OSM V1.0 specification. i.MX 8M Plus OSM LGA Module supports booting from On-OSM eMMC and OSM SD (from carrier board). Any of these boot media can selected by properly setting the Boot Select Pins status from the carrier board as mentioned below.

BOOT_SEL#	Description
Float	eMMC Flash (uSDHC3)
GND	OSM SD (uSDHC2)

Also, i.MX 8M Plus OSM LGA Module supports active low FORCE_RECOV# functionality using one of the vendor-defined pins in OSM LGA. By pulling low on this pin puts i.MX 8M Plus SoC goes to serial download mode where the SoC boot media can be programmed through i.MX 8M Plus SoC's USB1 controller USB 3.0 interface which is connected to USB3 port of OSM LGA.

OSM Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U19	BOOT_SEL#	BOOT_SEL#	BOOT_MODE0 /G10	I, 1.8V CMOS 10K PU	Boot Media Select bit 0
P16	VENDOR DEFINED3	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Active low Force Recovery Input. *Note: Also connected to 16th pin of on-OSM programming header & on-OSM push button SW1.*

2.7.20 Power and GND

The i.MX 8M Plus OSM LGA Module works with 5V power input (VCC) from OSM LGA and generates all other required powers internally On-OSM itself. i.MX 8M Plus OSM LGA Module also supports coin cell power input (VDD_RTC) from OSM LGA to On-OSM RTC controller for real time clock.

For more details on Power and GND Signals pinouts on OSM LGA, refer the below table.

OSM Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y8,Y9,Y10,Y11,Y17 Y25,Y26,Y27,Y28 AE4,AF4,AG4,AH3,AH4, AJ3,AJ4,AK4	VCC_IN_5V	VCC_IN_5V	NA	I, 5V Power	Module power input voltage of 5V
W17	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.
M17	VCC_1_TEST	VDD_3V3	NA	O, 3.3V Power	Module power voltage test point

OSM Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M19	VCC_2_TEST	NVCC_SD2	NA	O, 1.8V or 3V3 Power	Module power voltage test point
Y16	VCC_3_TEST	VDD_ARM_0V85	NA	O, 0.85V Power	Module power voltage test point
Y20	VCC_4_TEST	NVCC_SNVS_1V8	NA	O,1V8 Power	Module power voltage test point
Y3	VCC_5_TEST	VDD_1V8	NA	O,1V8 Power	Module power voltage test point
C5	VCC_6_TEST	NVCC_DRAM_1V1	NA	O ,1.1C Power	Module power voltage test point
AA33	VCC_7_TEST	VDD_SOC_0V85	NA	O, 0.85V Power	Module power voltage test point
B29	VCC_8_TEST	VDDA_1V8	NA	O,1.8V Power	Module power voltage test point
A4,A7,A10,B2,B5,B8,B9,C11,D1,D5,D8,E2,H2,H4,L2,L4,P2,P4,R1,U2,U4,V1,W3,Y2,AA1,AA4,AA7,AA8,AA10,AA11,AB3,AB6,AB9,AC4,AC7,AC10,A26,A29,A32,B27,B28,B30,B33,C25,C32,C35,D28,D34,F33,F35,G34,H32,J33,J35,K34,M35,N34,T34,W34,AA25,AA26,AA27,AA28,AA32,AB28,AB31,AB34,AC27,AC30,AC33,AE2,AE34,AF35,AG3,AH2,AH34,AJ35,AK3,AL2,AL34,AM13,AM16,AM19,AM22,AM35,AN3,AN6,AN9,AN11,AN15,AN18,AN21,AN33,AP2,AP25,AP28,AP31,AP34,AR14,AR17,AR20,AR26,AR29,AR32	GND	GND	NA	Power	Ground.

2.8 Other Features

2.8.1 FORCE_RECOV#

The i.MX 8M Plus OSM LGA Module supports on-OSM push button for FORCE_RECOV#. Pressing this button puts i.MX 8M Plus SoC to serial download mode where the SoC boot media can be programmed. This push button is physically located on the top of the module as shown below.

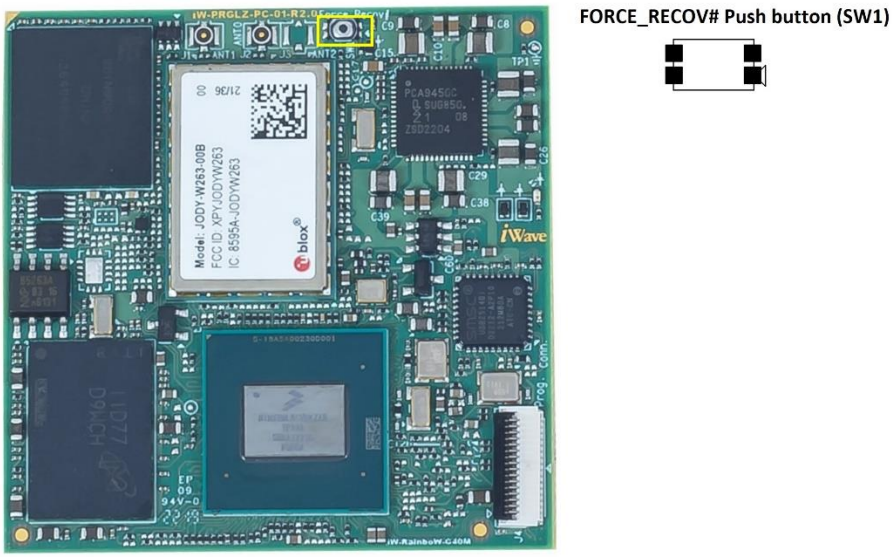

Figure 5: FORCE_RECOV# Push button

SW Identifier	Signal Name	Description		Remarks
		Push	Release	
SW1	FORCE_RECOV#	CPU USB Serial Mode (For programming the OSM boot media)	CPU Normal Boot Mode	*Note: Same signal is connected to 16th pin of on-OSM programming header & P16 of OSM*

2.8.2 Programming Header

The i.MX 8M Plus OSM LGA Module supports 16 pin on-OSM programming header for powering ON and testing the on-OSM features without soldering on the carrier board. This header is physically located on the top of the module as shown below.

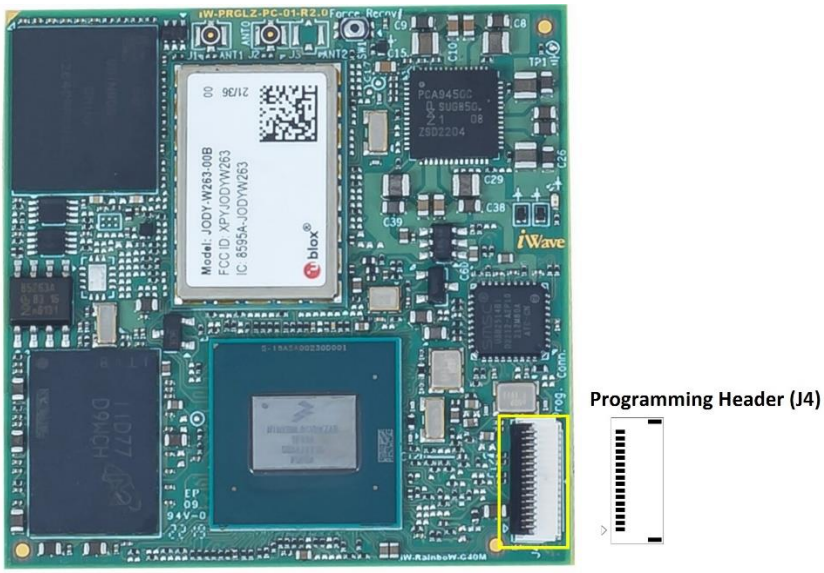

Figure 6: Programming Header

Number of Pins - 16

Connector Part - 503480-1600 from Molex

Table 4: Programming header Pin assignment

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_IN_5V	NA	I, 5V Power	Supply voltage
2	VCC_IN_5V	NA	I, 5V Power	Supply voltage
3	VCC_IN_5V	NA	I, 5V Power	Supply voltage
4	VCC_IN_5V	NA	I, 5V Power	Supply voltage
5	VCC_IN_5V	NA	I, 5V Power	Supply voltage
6	GND	NA	I, 5V Power	Ground
7	USB_OTG1_DM	USB1_D_N/E10	IO, USB	USB 2.0 OTG High Speed Data Negative.
8	USB_OTG1_DP	USB1_D_P/D10	IO, USB	USB 2.0 OTG High Speed Data Positive.
9	GND	NA	Power	Ground
10	VBUS_OTG1	USB1_VBUS/A11	I, Power	USB OTG VBUS power for detection.
11	GND	NA	Power	Ground
12	UART4_RXD	UART4_RXD/AJ5	O, 1.8V CMOS	Debug UART Receiver.
13	UART4_TXD	UART4_TXD/AH5	I, 1.8V CMOS	Debug UART Transmitter.
14	GND	NA	Power	Ground
15	GND	NA	Power	Ground
16	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Active low Force Recovery Input.

2.9 i.MX 8M Plus Pin Multiplexing on OSM LGA

The i.MX 8M Plus SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M Plus SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8M Plus SoC pin connections to the OSM LGA and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M Plus Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the OSM LGA for iWave's BSP reusability and to have compatible OSM modules in future for upgradability.

Table 5: i.MX 8M Plus SoC IOMUX for OSM interfaces

Interface/ Function	OSM Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
MIPI CSI	C2	AH20	ECSPI2_MISO	UART4_CTS_B	I2C4_SCL	SAI7_MCLK	CCM_CLKO1	GPIO5_IO12	
	C4	AJ7	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO18	
	C3	AJ6	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO19	
PWM0	E18	AD8	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO21	
LVDS	AN23	L25	NAND_DATA01	QSPI_A_DATA1	SAI3_TX_SYNC	ISP_PRELIGHT_TRIG_0	UART4_TX	GPIO3_IO7	CORESIGHT_TRACE05
	AN14	L24	NAND_DATA02	QSPI_A_DATA2	USDHC3_CD_B	UART4_CTS_B		GPIO3_IO8	CORESIGHT_TRACE06
	AM11	AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	FLEXCAN1_TX	GPIO5_IO3	
	AM12	AD18	SPDIF1_IN	PWM2_OUT	I2C5_SDA	GPT1_COMPARE2	FLEXCAN1_RX	GPIO5_IO4	
	AN22	AE16	SAI5_RX_DATA0	SAI1_TX_DATA2	PWM2_OUT	I2C5_SCL	PDM_BIT_STREAM0	GPIO3_IO21	
HDMI	C31	AD22	HDMI_CEC			I2C6_SCL	FLEXCAN2_TX	GPIO3_IO28	
	D33	AE22	HDMI_HPD	HDMI_HPD_O		I2C6_SDA	FLEXCAN2_RX	GPIO3_IO29	
	C33	AC22	HDMI_SCL			I2C5_SCL	FLEXCAN1_TX	GPIO3_IO26	
	C34	AF22	HDMI_SDA			I2C5_SDA	FLEXCAN1_RX	GPIO3_IO27	
uSDHC2	F21	AB29	USDHC2_CLK		ECSPI2_SCLK	UART4_RX		GPIO2_IO13	
	E20	AB28	USDHC2_CMD		ECSPI2_MOSI	UART4_TX	PDM_CLK	GPIO2_IO14	
	G20	AC28	USDHC2_DATA0		I2C4_SDA	UART2_RX	PDM_BIT_STREAM0	GPIO2_IO15	
	G21	AC29	USDHC2_DATA1		I2C4_SCL	UART2_TX	PDM_BIT_STREAM1	GPIO2_IO16	

Interface/ Function	OSM Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	H20	AA26	USDHC2_DATA2		ECSPI2_SS0	SPDIF1_OUT	PDM_BIT_STREAM2	GPIO2_IO17	
	H21	AA25	USDHC2_DATA3		ECSPI2_MISO	SPDIF1_IN	PDM_BIT_STREAM3	GPIO2_IO18	SRC_EARLY_RESET
	D21	AD28	USDHC2_RESET_B					GPIO2_IO19	SRC_SYSTEM_RESET
	D20	AC26	USDHC2_WP					GPIO2_IO20	CORESIGHT_EVENTI
	J21	AD29	USDHC2_CD_B					GPIO2_IO12	
uSDHC1	K20	W28	USDHC1_CLK	ENET1_MDC		I2C5_SCL	UART1_TX	GPIO2_IO0	
	K21	W29	USDHC1_CMD	ENET1_MDIO		I2C5_SDA	UART1_RX	GPIO2_IO1	
	L20	Y29	USDHC1_DATA0	ENET1_RGMII_TD1		I2C6_SCL	UART1_RTS_B	GPIO2_IO2	
	L21	Y28	USDHC1_DATA1	ENET1_RGMII_TD0		I2C6_SDA	UART1_CTS_B	GPIO2_IO3	
	M21	V29	USDHC1_DATA2	ENET1_RGMII_RD0		I2C4_SCL	UART2_TX	GPIO2_IO4	
	N20	V28	USDHC1_DATA3	ENET1_RGMII_RD1		I2C4_SDA	UART2_RX	GPIO2_IO5	
	N21	U26	USDHC1_DATA4	ENET1_RGMII_TX_CTL		I2C1_SCL	UART2_RTS_B	GPIO2_IO6	
	P20	AA29	USDHC1_DATA5	ENET1_TX_ER		I2C1_SDA	UART2_CTS_B	GPIO2_IO7	
	P21	AA28	USDHC1_DATA6	ENET1_RGMII_RX_CTL		I2C2_SCL	UART3_TX	GPIO2_IO8	
	R21	U25	USDHC1_DATA7	ENET1_RX_ER		I2C2_SDA	UART3_RX	GPIO2_IO9	
	T21	W25	USDHC1_RESET_B	ENET1_INPUT=ENET1_TX_CLK, OUTPUT=CCM_ENET_REF_CLK_ROOT		I2C3_SCL	UART3_RTS_B	GPIO2_IO10	
	U20	W26	USDHC1_STROBE			I2C3_SDA	UART3_CTS_B	GPIO2_IO11	
ECSPI2	AA23	AJ22	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA		CCM_CLKO2	GPIO5_IO13	
	Y21	AH21	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TX_BCLK		GPIO5_IO10	

Interface/ Function	OSM Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	Y23	AJ21	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI7_TX_DATA0		GPIO5_IO11	
	Y22	AF8	I2C4_SCL	PWM2_OUT	PCIE_CLKREQ_B	ECSPI2_MISO		GPIO5_IO20	
ECSPI1	Y15	AE20	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI7_TX_SYNC		GPIO5_IO9	
	U16	AF20	ECSPI1_SCLK	UART3_RX	I2C1_SCL	SAI7_RX_SYNC		GPIO5_IO6	
	U15	AD20	ECSPI1_MISO	UART3_CTS_B	I2C2_SCL	SAI7_RX_DATA0		GPIO5_IO8	
	V15	AC20	ECSPI1_MOSI	UART3_TX	I2C1_SDA	SAI7_RX_BCLK		GPIO5_IO7	
USB OTG1	C10	A6	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT	
UART2	A14	AF6	UART2_RX	ECSPI3_MISO		GPT1_COMPARE3		GPIO5_IO24	
	B13	AH4	UART2_TX	ECSPI3_SS0		GPT1_COMPARE2		GPIO5_IO25	
	C13	AJ18	SAI3_RX_BCLK	SAI2_RX_DATA2	SAI5_RX_BCLK	GPT1_CLK	UART2_CTS_B	GPIO4_IO29	PDM_CLK
	C14	AF18	SAI3_RX_DATA0	SAI2_RX_DATA3	SAI5_RX_DATA0		UART2_RTS_B	GPIO4_IO30	PDM_BIT_STREAM1
UART1	D13	AJ3	UART1_TX	ECSPI3_MOSI				GPIO5_IO23	
	D14	AD6	UART1_RX	ECSPI3_SCLK				GPIO5_IO22	
	D15	AE6	UART3_RX	UART1_CTS_B	USDHC3_RESET_B	GPT1_CAPTURE2	CAN2_TX	GPIO5_IO26	
	D16	AJ4	UART3_TX	UART1_RTS_B	USDHC3_VSELECT	GPT1_CLK	CAN2_RX	GPIO5_IO27	
UART3	A22	N25	NAND_ALE	QSPI_A_SCLK	SAI3_TX_BCLK	ISP_FL_TRIG_0	UART3_RX	GPIO3_IO0	CORESIGHT_TRACE_CLK
	B23	L26	NAND_CE0_B	QSPI_A_SS0_B	SAI3_TX_DATA0	ISP_SHUTTER_TRIG_0	UART3_TX	GPIO3_IO1	CORESIGHT_TRACE_CTL
UART4	D22	AJ5	UART4_RX	UART2_CTS_B	PCIE_CLKREQ_B	GPT1_COMPARE1	I2C6_SCL	GPIO5_IO28	
	D23	AH5	UART4_TX	UART2_RTS_B		GPT1_CAPTURE1	I2C6_SDA	GPIO5_IO29	
SAI2	V18	AJ15	SAI2_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_IN	FLEXCAN2_RX	ENET_QOS_1588_EVENT3_AUX_IN	GPIO4_IO27	SAI3_MCLK
	W21	AH16	SAI2_TX_DATA0	SAI5_TX_DATA3	ENET_QOS_1588_EVENT2_IN	FLEXCAN2_TX	ENET_QOS_1588_EVENT2_AUX_IN	GPIO4_IO26	

Interface/ Function	OSM Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	V21	AJ14	SAI2_RX_DATA0	SAI5_TX_DATA0	ENET_QOS_1588_EVENT2_OUT	SAI2_TX_DATA1	UART1_RTS_B	GPIO4_IO23	PDM_BIT_STREAM3
	W20	AH15	SAI2_TX_BCLK	SAI5_TX_DATA2		FLEXCAN1_RX		GPIO4_IO25	PDM_BIT_STREAM1
	W18	AJ17	SAI2_TX_SYNC	SAI5_TX_DATA1	ENET_QOS_1588_EVENT3_OUT	SAI2_TX_DATA1	UART1_CTS_B	GPIO4_IO24	PDM_BIT_STREAM2
CAN	AC17	AD16	SAI5_RX_DATA1	SAI1_TX_DATA3	SAI1_TX_SYNC	SAI5_TX_SYNC	PDM_BIT_STREAM1	GPIO3_IO22	FLEXCAN1_TX
	AB17	AF16	SAI5_RX_DATA2	SAI1_TX_DATA4	SAI1_TX_SYNC	SAI5_TX_BCLK	PDM_BIT_STREAM2	GPIO3_IO23	FLEXCAN1_RX
	AC19	AE14	SAI5_RX_DATA3	SAI1_TX_DATA5	SAI1_TX_SYNC	SAI5_TX_DATA0	PDM_BIT_STREAM3	GPIO3_IO24	FLEXCAN2_TX
	AB19	AF14	SAI5_MCLK	SAI1_TX_BCLK	PWM1_OUT	I2C5_SDA		GPIO3_IO25	FLEXCAN2_RX
GPIO	D17	AC12	SAI1_TX_DATA6	SAI6_RX_SYNC	SAI6_TX_SYNC		ENET1_RX_ER	GPIO4_IO18	
	E17	AJ13	SAI1_TX_DATA7	SAI6_MCLK		PDM_CLK	ENET1_TX_ER	GPIO4_IO19	
	F17	AJ9	SAI1_RX_SYNC				ENET1_1588_EVENT0_IN	GPIO4_IO0	
	G17	AH8	SAI1_RX_BCLK			PDM_CLK	ENET1_1588_EVENT0_OUT	GPIO4_IO1	
	H17	AC10	SAI1_RX_DATA0		SAI1_TX_DATA1	PDM_BIT_STREAM0	ENET1_1588_EVENT1_IN	GPIO4_IO2	
	J17	AD14	SAI5_RX_BCLK	SAI1_TX_DATA1	PWM3_OUT	I2C6_SDA	PDM_CLK	GPIO3_IO20	
	K17	AJ16	SAI2_RX_BCLK	SAI5_TX_BCLK		FLEXCAN1_TX	UART1_RX	GPIO4_IO22	PDM_BIT_STREAM1
	L17	AH17	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA1	SAI2_RX_DATA1	UART1_TX	GPIO4_IO21	PDM_BIT_STREAM2
	D19	AJ19	SAI3_RX_SYNC	SAI2_RX_DATA1	SAI5_RX_SYNC	SAI3_RX_DATA1	SPDIF1_IN	GPIO4_IO28	PDM_BIT_STREAM0
	E19	AF10	SAI1_RX_DATA1			PDM_BIT_STREAM1	ENET1_1588_EVENT1_OUT	GPIO4_IO3	
	F19	AC14	SAI5_RX_SYNC	SAI1_TX_DATA0	PWM4_OUT	I2C6_SCL		GPIO3_IO19	
	G19	AC18	SPDIF1_EXT_CLK	PWM1_OUT		GPT1_COMPARE3		GPIO5_IO5	

Interface/ Function	OSM Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	H19	R26	NAND_DQS	QSPI_A_DQS	SAI3_MCLK	ISP_SHUTTER_OPEN_0		GPIO3_IO14	CORESIGHT_TRACE12
	J19	A3	GPIO1_IO6	ENET_QOS_MDC		ISP_SHUTTER_TRIG_1		USDHC1_CD_B	CCM_EXT_CLK3
	K19	A7	GPIO1_IO0	CCM_ENET_PHY_REF_CLK_ROOT		ISP_FL_TRIG_0		CCM_REF_CLK_32K	CCM_EXT_CLK1
	L19	B8	GPIO1_IO9	ENET_QOS_1588_EVENT0_OUTPWM2_OUT	PWM2_OUT	ISP_SHUTTER_OPEN_1	USDHC3_RESET_B	SDMA2_EXT_EVENT[0]	
	D3	F6	GPIO1_IO7	ENET_QOS_MDIO		ISP_FLASH_TRIG_1		USDHC1_WP	CCM_EXT_CLK4
	D4	D8	GPIO1_IO11	USB2_OTG_ID	PWM2_OUT		USDHC3_VSELECT	CCM_PMIC_READY	
	E3	AE12	SAI1_MCLK		SAI1_TX_BCLK		ENET1_TX_CLK/CCM_ENET_REF_CLK_ROOT	GPIO4_IO20	
	G3	B5	GPIO1_IO15	USB2_OTG_OC			USDHC3_WP	PWM4_OUT	CCM_CLKO2
	G4	B7	GPIO1_IO10	USB1_OTG_ID	PWM3_OUT				
I2C2	AA15	AH6	I2C2_SCL	ENET_QOS_1588_EVENT1_IN	USDHC3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_AUX_IN	GPIO5_IO16	
	AA16	AE8	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT	USDHC3_WP	ECSPI1_SS0		GPIO5_IO17	
I2C1	AA20	AC8	I2C1_SCL	ENET_QOS_MDC		ECSPI1_SCLK		GPIO5_IO14	
	AA21	AH7	I2C1_SDA	ENET_QOS_MDIO		ECSPI1_MOSI		GPIO5_IO15	
ENET_QOS	J15	AE24	ENET_QOS_RGMII_TXC	ENET_QOS_TX_ER	SAI7_TX_DATA0			GPIO1_IO23	USDHC3_DATA1
	K16	AF24	ENET_QOS_RGMII_TX_CTL		SAI6_MCLK			GPIO1_IO22	USDHC3_DATA0
	H15	AC25	ENET_QOS_RGMII_TD0		SAI6_RX_BCLK	PDM_CLK		GPIO1_IO21	USDHC3_WP
	G15	AE26	ENET_QOS_RGMII_TD1		SAI6_RX_SYNC	PDM_BIT_STREAM0		GPIO1_IO20	USDHC3_CD_B

Interface/ Function	OSM Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	H16	AF26	ENET_QOS_RGMII_TD2	ENET_QOS_INPUT=ENET_QOS_TX_CLK, OUTPUT=CCM_ENET_QOS_REF_CLK_ROOT	SAI6_RX_DATA0	PDM_BIT_STREAM1		GPIO1_IO19	USDHC3_DATA7
	G16	AD24	ENET_QOS_RGMII_TD3		SAI6_TX_BCLK	PDM_BIT_STREAM2		GPIO1_IO18	USDHC3_DATA6
	R15	AE29	ENET_QOS_RGMII_RXC	ENET_QOS_RX_ER	SAI7_TX_BCLK	PDM_BIT_STREAM2		GPIO1_IO25	USDHC3_DATA3
	M15	AE28	ENET_QOS_RGMII_RX_CTL		SAI7_TX_SYNC	PDM_BIT_STREAM3		GPIO1_IO24	USDHC3_DATA2
	K15	AG29	ENET_QOS_RGMII_RD0		SAI7_RX_DATA0	PDM_BIT_STREAM1		GPIO1_IO26	USDHC3_DATA4
	L15	AG28	ENET_QOS_RGMII_RD1		SAI7_RX_SYNC	PDM_BIT_STREAM0		GPIO1_IO27	USDHC3_RESET_B
	N15	AF29	ENET_QOS_RGMII_RD2		SAI7_RX_BCLK	PDM_CLK		GPIO1_IO28	USDHC3_CLK
	P15	AF28	ENET_QOS_RGMII_RD3		SAI7_MCLK			GPIO1_IO29	USDHC3_CMD
	T15	AH29	ENET_QOS_MDIO		SAI6_TX_SYNC	PDM_BIT_STREAM3		GPIO1_IO17	USDHC3_DATA5
	T16	AH28	ENET_QOS_MDC		SAI6_TX_DATA0			GPIO1_IO16	USDHC3_STROBE
ENET1	H1	AH14	SAI1_TX_DATA5	SAI6_RX_DATA0	SAI6_TX_DATA0		ENET1_RGMII_TXC	GPIO4_IO17	
	J2	AH13	SAI1_TX_DATA4	SAI6_RX_BCLK	SAI6_TX_BCLK		ENET1_RGMII_TX_CTL	GPIO4_IO16	
	G1	AJ11	SAI1_TX_DATA0				ENET1_RGMII_TD0	GPIO4_IO12	
	F1	AJ10	SAI1_TX_DATA1				ENET1_RGMII_TD1	GPIO4_IO13	
	G2	AH11	SAI1_TX_DATA2				ENET1_RGMII_TD2	GPIO4_IO14	

Interface/ Function	OSM Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
	F2	AD12	SAI1_TX_DATA3				ENET1_RGMII_TD3	GPIO4_IO15	
	P1	AJ12	SAI1_TX_BCLK				ENET1_RGMII_RXC	GPIO4_IO11	
	L1	AF12	SAI1_TX_SYNC				ENET1_RGMII_RX_CTL	GPIO4_IO10	
	J1	AD10	SAI1_RX_DATA4	SAI6_TX_BCLK	SAI6_RX_BCLK		ENET1_RGMII_RD0	GPIO4_IO6	
	K1	AE10	SAI1_RX_DATA5	SAI6_TX_DATA0	SAI6_RX_DATA0	SAI1_RX_SYNC	ENET1_RGMII_RD1	GPIO4_IO7	
	M1	AH10	SAI1_RX_DATA6	SAI6_TX_SYNC	SAI6_RX_SYNC		ENET1_RGMII_RD2	GPIO4_IO8	
	N1	AH12	SAI1_RX_DATA7	SAI6_MCLK	SAI1_TX_SYNC	SAI1_TX_DATA4	ENET1_RGMII_RD3	GPIO4_IO9	
	C6	AH9	SAI1_RX_DATA2			PDM_BIT_STREAM2	ENET1_MDC	GPIO4_IO4	
	C7	AJ8	SAI1_RX_DATA3			PDM_BIT_STREAM3	ENET1_MDIO	GPIO4_IO5	
PCIe	T2	A4	GPIO1_IO14	USB2_OTG_PWR			USDHC3_CD_B	PWM3_OUT	CCM_CLKO1
	V2	A5	GPIO1_IO12	USB1_OTG_PWR				SDMA2_EXT_EVENT[1]	
	R2	AJ20	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		SPDIF1_OUT	GPIO5_IO2	SPDIF1_IN

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Plus OSM LGA Module technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the seventeen VCC_IN_5V in Size-L Module and returned through the numerous GND pins on the LGA. A Module will withstand an indefinite exposure to an applied VCC_IN_5V that may vary over the 4.75V to 5.25V range, without damage, and it will operate over the entire VCC_IN_5V range of 4.75V to 5.25V. The OSM Module physical contact consists of a soldered connection able to carry a current of minimum 0.5 A per contact. This works out to 8.5A total for 17 contacts.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX 8M Plus OSM LGA Module.

Table 6: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_IN_5V	4.75V[1]	5V	5.25V	-
2	VDD_RTC [1]	-	3V	-	-

[1] *i.MX 8M Plus OSM LGA Module use this voltage as backup power source to RTC controller when VCC_IN_5V is off.*

3.1.2 Power Input Sequencing

The i.MX 8M Plus OSM LGA Module ’s Power Input sequence requirement is explained below. It is recommended that the main Carrier power supplies do not come up until the Module asserts the CARRIER_PWR_EN signal.

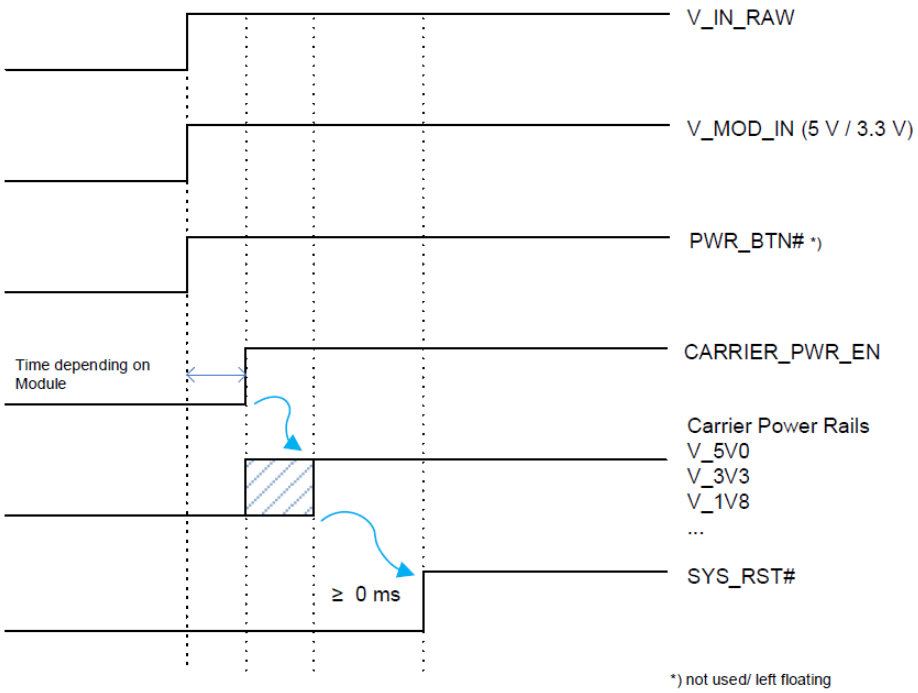

Figure 7: Power Input Sequencing

3.1.3 Power Consumption

Table 7: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Power Consumption during booting		
During Booting	VCC_IN_5V	0.412A/2.06W
Run Mode Power Consumption[1]		
Play Video run in MIPI display (Gstreamer)	VCC_IN_5V	0.428A/2.41W
Play 1080p Video run in 4K HDMI display (Gstreamer)	VCC_IN_5V	0.484A/2.42W
Play Video run in 10'Inch LVDS display (Gstreamer)	VCC_IN_5V	0.526A/2.63W
Camera Streaming in HDMI	VCC_IN_5V	0.496A/2.48W
Camera Streaming in 5.5” MIPI display	VCC_IN_5V	0.473A/2.365W
Camera Streaming in 10.1” LVDS display	VCC_IN_5V	0.513A/2.565W
Camera Streaming by connecting all 3 displays (HDMI, 5.5” MIPI ,10.1” LVDS display)	VCC_IN_5V	0.531A/2.655W
Play Audio	VCC_IN_5V	0.391A/1.955W
Ping Bluetooth	VCC_IN_5V	0.399A/1.995W
Ping Wi-Fi	VCC_IN_5V	0.409A/2.045W
Ping Ethernet (ETH0)	VCC_IN_5V	0.389A/1.945W
Ping Ethernet (ETH1)	VCC_IN_5V	0.369A/1.845W
Ping Ethernet (ETH0 and ETH1)	VCC_IN_5V	0.409A/2.045W
eMMC to Micro SD file transfer	VCC_IN_5V	0.462A/2.31W
eMMC to USB3.0 file transfer	VCC_IN_5V	0.413A/2.065W
eMMC to PCIe file transfer	VCC_IN_5V	0.428A/2.14W
eMMC to USB 3.0 Host (Type C) file transfer	VCC_IN_5V	0.388A/1.94W
Bluetooth file transfer	VCC_IN_5V	0.353A/1.765W
Wi-Fi file transfer	VCC_IN_5V	0.364A/1.82W
Ethernet Streaming (Video Play)	VCC_IN_5V	0.346A/1.73W
GPU Processor -Graphics 3D Test	VCC_IN_5V	0.756A/3.78W
Dhrystone	VCC_IN_5V	0.795A/3.975W
Transfer 1MB file between USB 3.0, USB 3.0TypeC Host, PCIe and Micro SD with 1000 count	VCC_IN_5V	0.665A/3.325W
Maximum Power Test: Run the below during Maximum Power Test, • Run the video on MIPI diplay,10Inch LVDS & HDMI Connected • Camera Streaming • Ethernet - Run the ping (65500 packet size) test on background (ETH0 & ETH1) • Wi-Fi- Run the ping test on back ground • FileTransfer - Transfer the 1GB files in storage devices • Run the dry2 application on back ground	VCC_IN_5V	1.21A/6.05W

Task/Status	Power Rail	Current Drawn/ Power Consumption
• Run the Graphics (GPU) application on HDMI display		
Low Power Mode Power Consumption		
System Idle Mode.	VCC_IN_5V	0.282A/1.41W
Deep Sleep Mode.	VCC_IN_5V	0.038A/0.19W
RTC power when no VCC_IN_5V supply is provided	VRTC_3V0	0.465uA/2.325uW

[1] Power consumption measurements are done in iWave's i.MX 8M Plus SoC based OSM Development platform with iWave's iW-PRGLZ-SC-01-R2.0-REL1.1-Linux5.15.71.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Plus OSM LGA Module.

Table 8: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]For more information on Thermal solution and Heat sink, refer the following section.

3.2.2 Heat Sink

For any highly integrated Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Note: iWave supports Heat Sink Solution for i.MX 8M Plus OSM LGA Module. For more information on Heat Sink, contact iWave support team. Do not Power ON the OSM without a proper thermal solution.

The following drawings illustrate the mechanical dimensions of the OSM-L Heatsink. All measurements are in millimetres (mm).

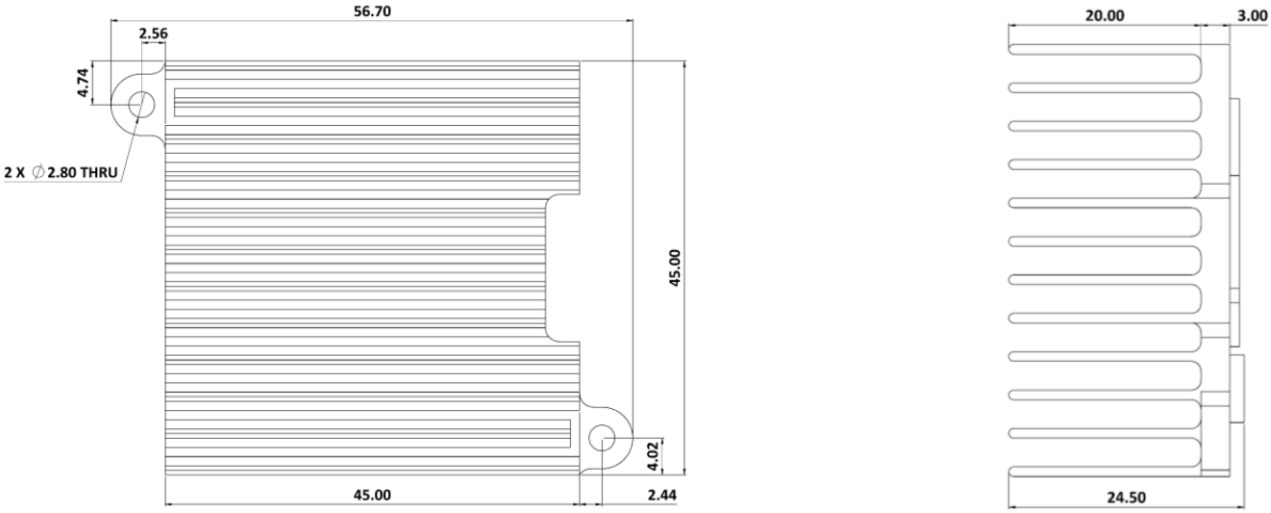

Figure 8: Mechanical dimension of heat Sink

3.2.3 RoHS Compliance

iWave's i.MX 8M Plus OSM LGA Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's i.MX 8M Plus OSM LGA Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the OSM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX 8M Plus OSM LGA Module Mechanical Dimensions

i.MX 8M Plus OSM LGA Module PCB size is 45 mm x 45 mm. Module mechanical dimension is shown below. (All dimensions are shown in mm). The i.MX 8M Plus OSM LGA Module PCB thickness is 1.2mm±0.15mm**,** top side maximum height component is 2.5mm (Wi-Fi module).

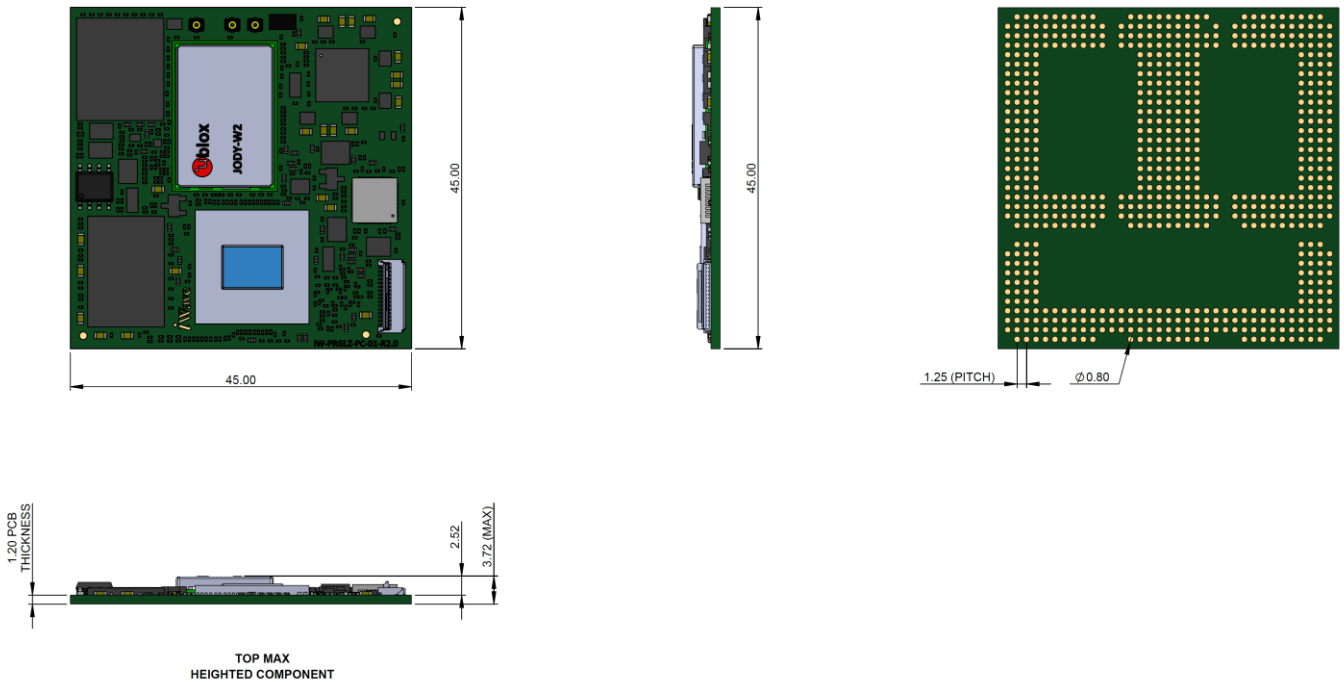

Figure 9: Mechanical dimensions of i.MX 8M Plus OSM LGA Module

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8M Plus OSM LGA Module variants. Please contact iWave for orderable part number of higher RAM memory size, Flash memory size or without Wi-Fi/BT OSM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 9: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G40M - i.MX 8M Plus OSM R2.0 (Industrial grade) with Wi-Fi		
iW-G40M- OLPQ-4L002G-E016G-BIA	i.MX8M Plus Quad, 2GB LPDDR4, 16GB eMMC - With Wi-Fi, BT	-40°C to 85°C
iW-G40M- OLPQ-4L004G-E016G-BIA	i.MX8M Plus Quad, 4GB LPDDR4, 16GB eMMC - With Wi-Fi, BT	-40°C to 85°C

Note:

- *Custom configuration Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.*
- *For OSM identification purpose, Product Part Number and OSM Unique Serial Number are pasted as Label with QR Code on OSM.*

5. APPENDIX-I

5.1 i.MX 8M Plus Pico ITX SBC

iWave Systems supports iW-RainboW-G40S-i.MX 8M Plus Pico ITX SBC which is targeted for quick validation of i.MX 8M Plus SoC based OSM and its features. Being a Pico-ITX form factor with 100mm x 72mm size, the SBC is highly packed with all necessary interfaces and on-board connectors to validate complete OSM supported features.

For more details on i.MX 8M Plus SBC, visit the below web link:

https://www.iwavesystems.com/product/i-mx-8m-plus-pico-itx-single-board-computer/

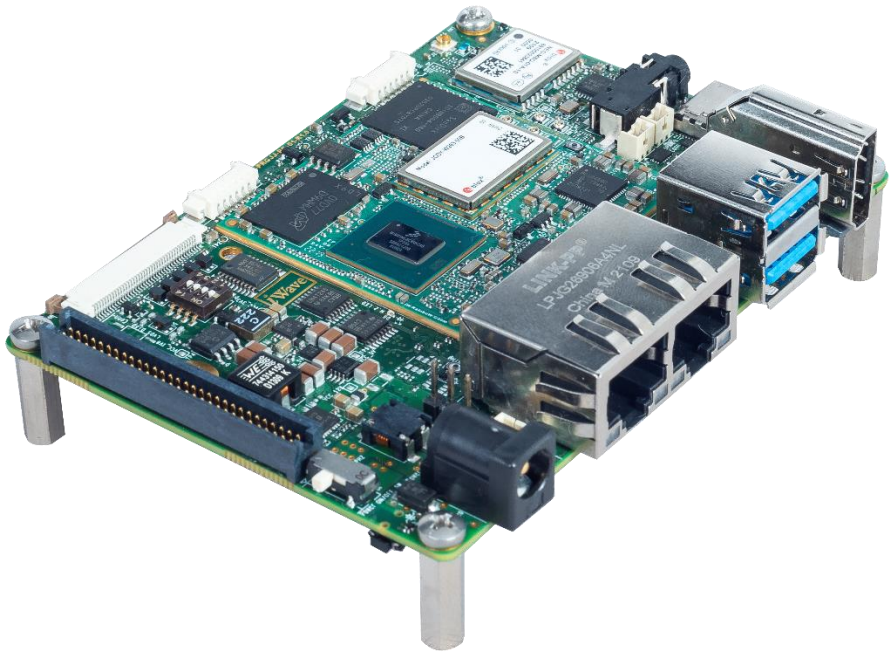

Figure 10: i.MX 8M Plus Pico ITX SBC

6. APPENDIX-II

6.1 Design and Assembly recommendations

- It is recommended to give 50-100mils clearance in the Carrier Board from the OSM Module to other components and more than 200mils to connectors for easier assembly.
- For the vibration environment, it is better to use heat sink with mechanical fixing and it is recommended to have mounting holes in the carrier board.

  If iWave's thermal solution is planned to use, two Mounting holes are recommended in the Carrier Board. For the position and dimensions of the holes, please refer below drawing. (All the dimension are in mm).

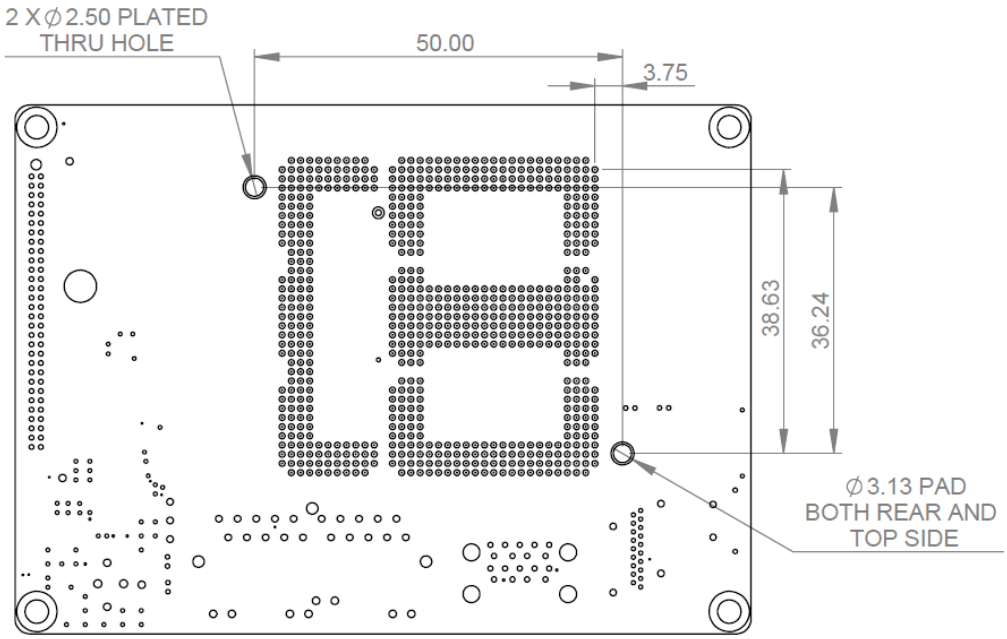

Figure 11: Dimensions of Mounting holes in the Carrier Board

- Contact iWave for more details regarding assembly of OSM on carrier board.


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