6MBP30XSK065-50

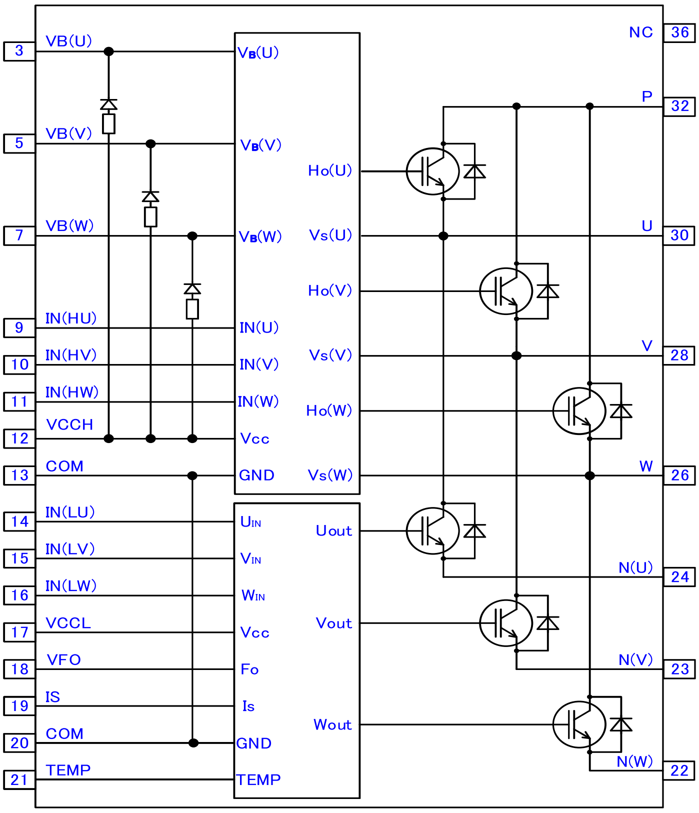
IGBT Modules

IGBT Module (X series)
650V / 30A / IPM

■ Features
Low-side IGBTs are separate emitter type
Short circuit protection
Temperature sensor output function
Overheating protection
Under voltage protection
Fault signal output function
Input interface : TTL(3.3V/5V)Active high logic

■ Applications
AC 100 ~ 240V three phase inverter drive for small power AC motor drives (such as compressor motor drive for air conditioner, compressor motor drive for heat pump applications,fan motor drive,ventilator motor drive)

■ Terminal assign and Internal circuit



Pin No.	Pin Name	Pin Description
3	VB(U)	High-side bias voltage for U-phase IGBT driving
5	VB(V)	High-side bias voltage for V-phase IGBT driving
7	VB(W)	High-side bias voltage for W-phase IGBT driving
9	IN(HU)	Signal input for high side U-phase
10	IN(HV)	Signal input for high side V-phase
11	IN(HW)	Signal input for high side W-phase
12	VCCH	High-side control supply
13	COM	Common supply ground
14	IN(LU)	Signal input for low side U-phase
15	IN(LV)	Signal input for low side V-phase
16	IN(LW)	Signal input for low side W-phase
17	VCCL	Low-side control supply
18	VFO	Fault output
19	IS	Over current sensing voltage input
20	COM	Common supply ground
21	TEMP	Temperature sensor output
22	N(W)	Negative bus voltage input for W-phase
23	N(V)	Negative bus voltage input for V-phase
24	N(U)	Negative bus voltage input for U-phase
26	W	Motor W-phase output
28	V	Motor V-phase output
30	U	Motor U-phase output
32	P	Positive bus voltage input
36	NC	No Connection

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■ Absolute maximum ratings (T_{vj}=25°C, T_c=25°C, V_{cc}=15V unless otherwise specified)

Block	Items	Symbol	Conditions	Units	Remarks
Inverter block	DC bus voltage	$V_{DC(theminal)}$	450	V	Note*1, See Fig.2-2
	Bus voltage (surge)	$V_{DC(surge,terminal)}$	500	V	Note*1, See Fig.2-2
	Collector-Emitter voltage	$V_{CE(chip)}$	650	V	Note*1, See Fig.2-2
	Collector current	I_C	30	A	Note*2
	Peak collector current	I_{CP}	60	A	V_{CC}≧15V, $V_{B(*)}$≧15V Note*2,*3,*4
			40	A	V_{CC}≧13V, $V_{B(*)}$≧13V Note*2,*3,*4
	Forward current	I_F	30	A	Note*2
	Peak forward current	I_{FP}	60	A	Note*2
	Collector power dissipation	P_{D_IGBT}	56.8	W	per single IGBT T_C=25°C
	FWD power dissipation	P_{D_FWD}	43.7	W	per single FWD T_C=25°C
	Self operation "DC bus voltage" of circuit protection between upper-arm and lower-arm	$V_{DC(SC)}$	400	V	$V_{CC}=V_{B(*)}$=13.5~16.5V T_{vj}=125°C, arm short circuit, non-repetitive less than 2us See Fig.2-2
	Virtual junction temperature	T_{vj}	150	°C	Note*8
	Operating virtual junction temperature (under switching conditions)	T_{vjop}	-40～+150	°C	
Control circuit block	High-side supply voltage	V_{CCH}	-0.5～20	V	Applied between VCCH-COM
	Low-side supply voltage	V_{CCL}	-0.5～20	V	Applied between VCCL-COM
	High-side bias absolute voltage	$V_{VB(U)-COM}$ $V_{VB(V)-COM}$ $V_{VB(W)-COM}$	-0.5～670	V	Applied between VB(U)-COM,VB(V)-COM, VB(W)-COM
	High-side bias voltage for IGBT gate driving	$V_{B(U)}$ $V_{B(V)}$ $V_{B(W)}$	-0.5～20	V	Note*4
	High-side bias offset voltage	V_U V_V V_W	-5～650	V	Applied between U-COM,V-COM,W-COM Note*5
	Input signal voltage	V_{IN}	-0.5～ V_{CCH}+0.5 -0.5～ V_{CCL}+0.5	V	Note*6
	Input signal current	I_{IN}	3	mA	sink current
	Fault signal voltage	V_{FO}	-0.5～V_{CCL}+0.5	V	Applied between VFO-COM
	Fault signal current	I_{FO}	1	mA	sink current
	Over current sensing input voltage	V_{IS}	-0.5～V_{CCL}+0.5	V	Applied between IS-COM
	Virtual junction temperature	T_{vj}	150	°C	
Operating case temperature		T_C	-40～+125	°C	See Fig.1-1
Storage temperature		T_{stg}	-40～+125	°C	
Isolation voltage		V_{isol}	AC1500	Vrms	Sine wave,60Hz t = 1min,Note*7
Mounting torque of screws		M_s	0.59～0.98	N･m	Mounting screw : M3

Note
*1 : V_{DC} is applied between P-N(U),P-N(V),P-N(W).
V_{CE} is Collector-Emitter voltage of internal IGBT chip.
*2 : Pulse width and duty are limited by T_{vj}max.
*3 : V_{CC} is applied between VCCH-COM,VCCL-COM.
*4 : $V_{B(*)}$ is applied between VB(U)-U,VB(V)-V, VB(W)-W.
*5 : Over 13.0V applied between VB(U)-U,VB(V)-V, VB(W)-W. This IPM module might make incorrect response if the high-side bias offset voltage is less than -5V.
*6 : Applied between IN(HU)-COM,IN(HV)-COM,IN(HW)-COM,IN(LU)-COM,IN(LV)-COM,IN(LW)-COM.
*7 : Applied between shorted all terminal and IMS (Insulated Metal Substrate).
*8 : The maximum temperature during continuous operation is T_{vj}=150°C.
The operating conditions have to be decided so that the temperature is below T_{vj}=150°C.
Continuous operation at over T_{vj}=150°C may result in degradation of product lifetime such as power cycling capability.

■ Electrical characteristics

●Inverter block (T_{vj}=25°C unless otherwise specified)

Description	Symbol	Conditions		min.	typ.	max	Unit
Zero gate voltage collector current	I_{CE}	V_{CE}=650V V_{IN}=0V	T_{vj}=25°C	-	-	1	mA
			T_{vj}=125°C	-	-	10	mA
Collector-Emitter saturation voltage	$V_{CE(sat)}$	V_{CC} = +15V $V_{B(*)}$=+15V V_{IN}=5V V_{IS}=0V Note *3, *4	I_C=3A T_{vj}=25°C	-	0.90	1.10	V
			I_C=30A T_{vj}=25°C	-	1.60	1.90	
			I_C=30A T_{vj}=125°C	-	1.75	2.10	
Forword voltage	V_F	I_F=30A V_{IN}=0V	T_{vj}=25°C	-	2.00	2.50	V
			T_{vj}=125°C	-	2.15	-	
Turn-on time	t_{on}	V_{DC} = 300V		0.65	1.05	1.45	µs
Turn-on delay time	$t_{d(on)}$	I_C = 30A		-	0.90	-	
Turn-on rise time	t_r	V_{CC}=15V		-	0.15	-	
V_{CE}-I_C cross time of turn-on	$t_{c(on)}$	$V_{B(*)}$=15V		-	0.40	0.70	
Turn-off time	t_{off}	T_{vj} = 125°C		-	1.20	1.70	
Turn-off delay time	$t_{d(off)}$	V_{IN}=0V <-> 5V		-	1.05	-	
Turn-off fall time	t_f	V_{IS}=0V		-	0.10	-	
V_{CE}-I_C cross time of turn-off	$t_{c(off)}$	See Fig.2-1		-	0.20	0.40	
Reverse recovery time	t_{rr}	Note *1, *3, *4		-	0.30	-	

■ Electrical characteristics

● Control circuit block

(T_{vj}=25°C, V_{CC}=15V, $V_{B(*)}$=15V, V_{IN}=0V, V_{IS}=0V unless otherwise specified)

Description	Symbol	Conditions		min.	typ.	max	Unit
Circuit current of low-side	I_{CCL}	V_{CCL}=15V	V_{IN}=5V	-	0.6	0.9	mA
		V_{CCL}=15V	V_{IN}=0V	-	0.6	0.9	
Circuit current of high-side	I_{CCH}	V_{CCH}=15V	V_{IN}=5V	-	0.8	1.9	mA
		V_{CCH}=15V	V_{IN}=0V	-	0.8	1.9	
Circuit current of bootstrap circuit (per one unit)	I_{CCHB}	$V_{B(U)}$=15V $V_{B(V)}$=15V $V_{B(W)}$=15V	V_{IN}=5V	-	-	0.2	mA
			V_{IN}=0V	-	-	0.2	
Input signal threshold voltage	$V_{th(on)}$	Note*9 PW≥0.7μs		-	2.1	2.6	V
	$V_{th(off)}$			0.8	1.3	-	
Input signal threshold hysteresis voltage	$V_{th(hys)}$			0.35	0.8	-	V
Operational input pulse width of turn-on	$t_{IN(ON)}$	V_{IN}=0V to 5V rise up Note*6,*9		0.5	-	-	μs
Operational input pulse width of turn-off	$t_{IN(OFF)}$	V_{IN}=5V to 0V fall down Note*6,*9		0.7	-	-	μs
Input current	I_{IN}	V_{IN}=5V Note*6		0.7	1.0	1.5	mA
Input pull-down resistance	R_{IN}	Note*6		3.3	5.0	7.2	kΩ
Fault output voltage	$V_{FO(H)}$	V_{IS}=0V,V_{FO} terminal pull up to 5V by 10kΩ		4.9	-	-	V
	$V_{FO(L)}$	V_{IS}=1V,I_{FO}=1mA		-	-	0.95	V
Fault output pulse width	t_{FO}	Note*10 See Fig.2-3, 2-4		20	-	-	μs

■ Electrical characteristics

● Control circuit block (continued)

Description	Symbol	Conditions		min.	typ.	max	Unit
Over current protection voltage level	$V_{IS(ref)}$	V_{CC}=15V Note*3,11		0.455	0.480	0.505	V
Over current protection delay time	$t_{d(IS)}$	See Fig.2-3		0.3	0.8	1.3	μs
Output voltage of temperature sensor	$V_{(temp)}$	Note*12	$T_{vj(LVIC)}$=90°C	2.63	2.77	2.91	V
			$T_{vj(LVIC)}$=25°C	0.88	1.13	1.39	
LVIC overheating protection	T_{OH}	Note *12 See Fig.2-7		136	143	150	°C
T_{OH} Hysteresis	$T_{OH(hys)}$			4	10	20	°C
V_{CC} under voltage trip level of low-side	$V_{CCL(OFF)}$	T_{vj}<150°C See Fig.2-4		10.3	-	12.5	V
V_{CC} under voltage reset level of low-side	$V_{CCL(ON)}$			10.8	-	13.0	V
V_{CC} under voltage hysteresis	$V_{CCL(hys)}$			-	0.5	-	V
V_{CC} under voltage trip level of high-side	$V_{CCH(OFF)}$	T_{vj}<150°C See Fig.2-5		8.3	-	10.3	V
V_{CC} under voltage reset level of high-side	$V_{CCH(ON)}$			8.8	-	10.8	V
V_{CC} under voltage hysteresis	$V_{CCH(hys)}$			-	0.5	-	V
V_B under voltage trip level	$V_{B(OFF)}$	T_{vj}<150°C See Fig.2-6		10.0	-	12.0	V
V_B under voltage reset level	$V_{B(ON)}$			10.5	-	12.5	V
V_B under voltage hysteresis	$V_{B(hys)}$			-	0.5	-	V
Forward voltage of bootstrap diode	$V_{F(BSD)}$	T_{vj}=25°C $I_{F(BSD)}$=10mA		1.5	1.7	1.9	Ω
Built-in limiting Series Resistance (BSD)	$R_{S(BSD)}$	T_{vj}=25°C		80	100	120	

Note

*9 : This IPM module might make incorrect response if the input signal pulse width is less than $t_{IN(on)}$ and $t_{IN(off)}$.

*10 : Fault signal is asserted corresponding to “Over-current protection”, “Under-voltage protection” at low-side, and “Overheat protection”.
Under the condition of “Over-current protection”, “Under-voltage protection” or “Overheat protection”, the fault signal is asserted continuously while these conditions are continuing. However, the minimum fault output pulse width is minimum 20μsec even if very short failure condition (which is less than 20μs) is triggered.

*11 : Over current protection is functioning only for the low-side arms.

*12 : Fig.1-1 shows the measurement position of temperature sensor.

■ Thermal characteristic(T_C=25°C)

Description	Symbol	min.	typ.	max	Unit
Junction to case thermal resistance (per single IGBT) Note*13	$R_{th(j-c)\_IGBT}$	-	-	2.20	°C/W
Junction to case thermal resistance (per single FWD) Note*13	$R_{th(j-c)\_FWD}$	-	-	2.86	°C/W

Note
*13 : Thermal compound with good thermal conductivity should be applied evenly with +100µm~+200µm on the contacting surface of this device and heat-sink.

■ Mechanical characteristics(T_C=25°C)

Description	Symbol	Conditions	min.	typ.	max	Unit
Mounting torque of screws	M_S	Mounting screw : M3	0.59	0.69	0.98	N･m
Heat-sink side flatness	-	The AL-IMS part: See (A1),(A2) of Fig.1-2 and Fig.1-3	-50	-	100	µm
		The resin case part: See (B1),(B2) of Fig.1-2 and Fig.1-3	-200	-	0	
Weight	-	-	-	9.3	-	g
Resistance to soldering heat	–	Solder temp : 260 ±5°C Immersion time : 10±1s Solder alloy : Sn-Ag-Cu type	-	-	1	time

■ Recommend operation conditions(Note*17)

Description	Symbol	min.	typ.	max	Unit
DC bus voltage	V_{DC}	0	300	400	V
High-side bias voltage for IGBT gate driving	$V_{B(*)}$	13.0	15.0	18.5	V
High-side supply voltage	V_{CCH}	13.5	15.0	16.5	V
Low-side supply voltage	V_{CCL}	13.5	15.0	16.5	V
Control supply variation (under swiching conditions)	ΔV_B	-1	-	1	V/μs
	ΔV_{CC}	-1	-	1	
Input signal voltage	V_{IN}	0	-	5	V
Voltage for current sensing	V_{IS}	0	-	5	V
Potential difference of between COM to N (including surge)	V_{COM_N}	-5	-	5	V
Dead time for preventing arm-short (T_C≤125°C)	t_{DEAD}	1.0	-	-	μs
Output current (Note*14)	I_O	-	-	24.0	A rms
Minimum input pulse widht (Note*15,Note*16)	$PW_{IN(on)}$	0.5	-	-	μs
	$PW_{IN(off)}$	0.7	-	-	μs
PWM input frequency	f_{PWM}	-	-	20	kHz
Operating virtual junction temperature	T_{vjop}	-30	-	150	°C

Note

*14 : V_{DC}=300V, V_{CCH}=V_{CCL}=$V_{B(*)}$=15V, PF=0.8, Sinusoidal PWM, 3phase modulation, T_{vj}≤150°C ,T_c≤100°C , f_{PWM}=5kHz, f_O=200Hz, Ks=0.9

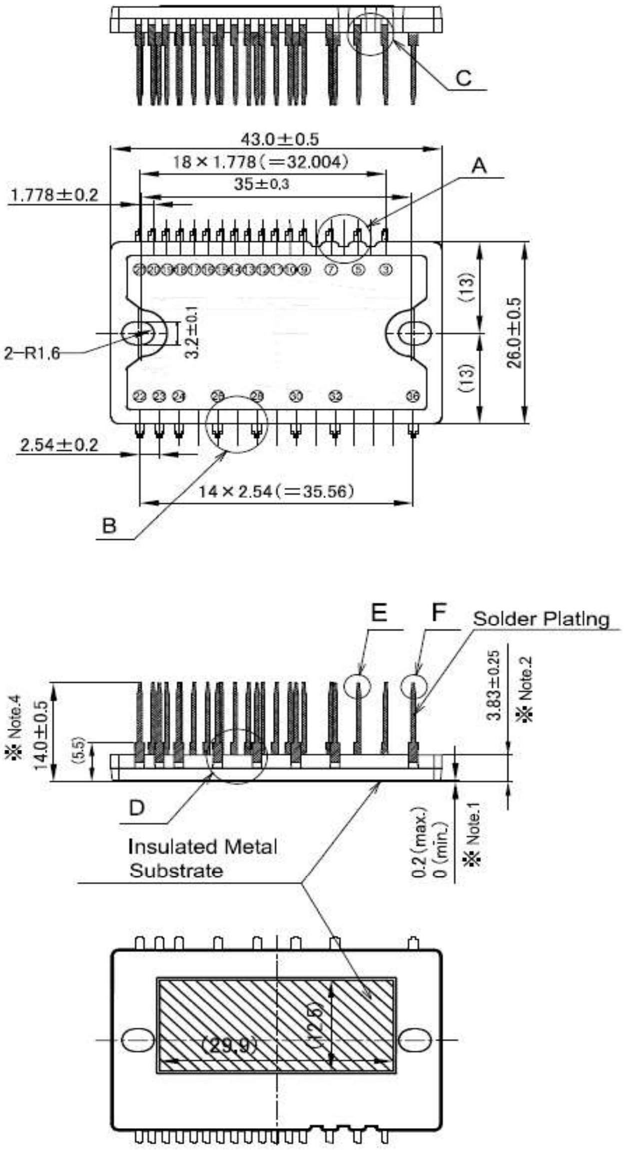
*15 : In the pulse width of 0.5us, the loss of IGBT increases for the saturation operation. To reduce the loss of IGBT, please enlarge the pulse width more than the switching time of IGBT.

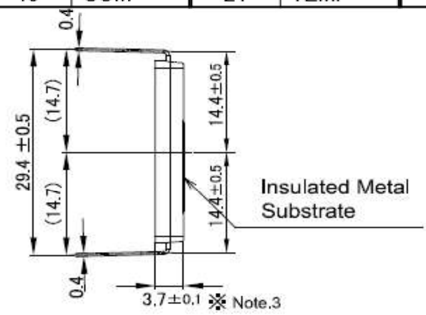
*16 : This IPM module might response according to input signal pulse even when the input signal pulse width is less than $PW_{IN(on)}$ and $PW_{IN(off)}$.

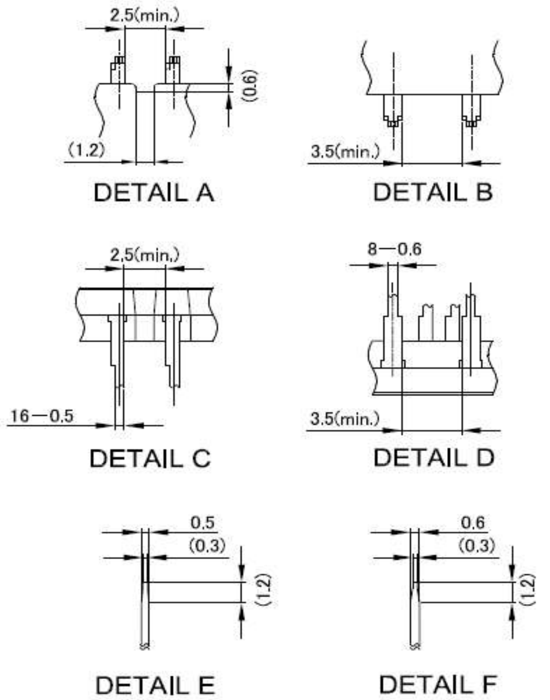
*17 : Recommended operating conditions are conditions for guaranteeing that the product operates normally. If it is used beyond this condition, operation and reliability may be adversely affected.

■ Packing outline dimensions (T_C=25℃)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
3	VB(U)	14	IN(LU)	22	N(W)
5	VB(V)	15	IN(LV)	23	N(V)
7	VB(W)	16	IN(LW)	24	N(U)
9	IN(HU)	17	VCCL	26	W
10	IN(HV)	18	VFO	28	V
11	IN(HW)	19	IS	30	U
12	VCCH	20	COM	32	P
13	COM	21	TEMP	36	NC



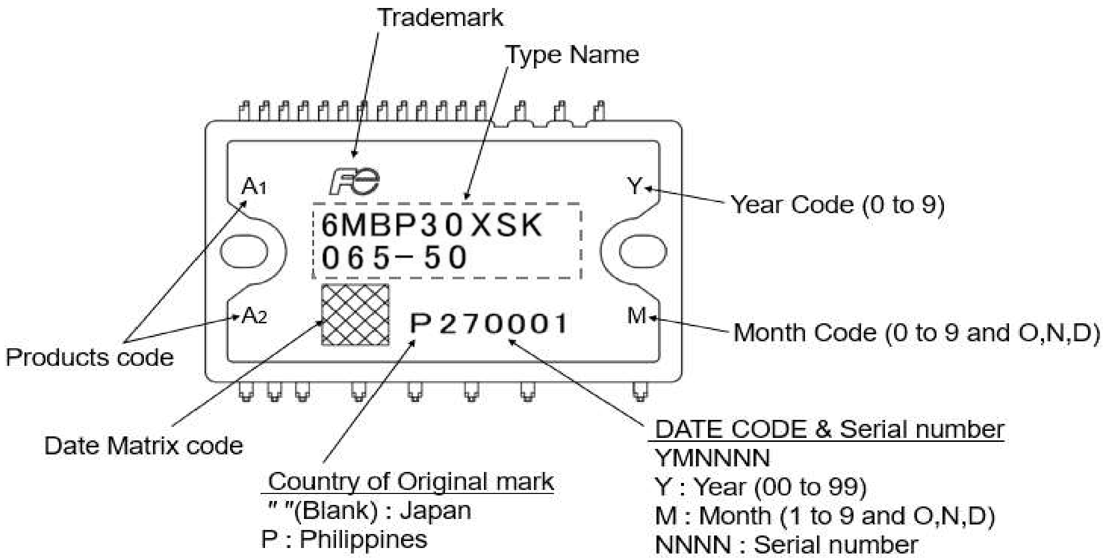




Unit: mm

Note.1
IMS(Insulated Metal Substrate) is deliberately protruded to improve the thermal conductivity between IMS and heat-sink.
Note.2
The thickness from the package surface to the back side includes the IMS.
Note.3
Thickness of the case part of the package outer wall. (excluding the IMS and marking surface)
Note.4
Height of the terminal and height of the stopper part including IMS.

■ Marking



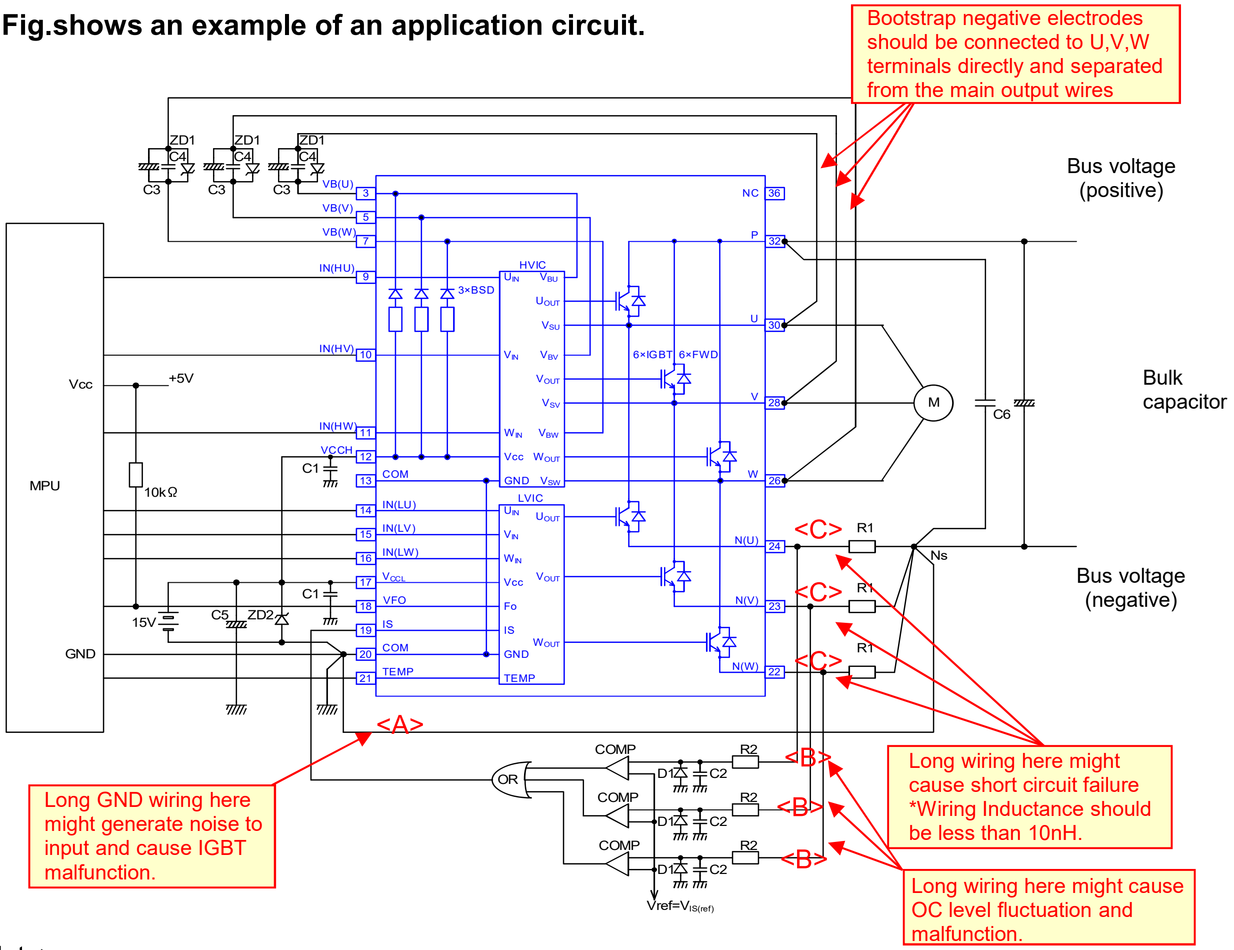
Note

Product code A_1 means current ratings , and “O” is marked.

Product code A_2 means variations , and “K” is marked.

■ An example of application circuit.

● Fig.shows an example of an application circuit.



<Note>

1. Input signal for drive is High-Active. There is a pull-down resistor built in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using R-C coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
2. By the function of the HVIC, it is possible of the direct coupling to microprocessor (MPU) without any photo-coupler or pulse-transformer isolation.
3. VFO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.
4. To prevent erroneous protection, the wiring of (A), (B), (C) should be as short as possible.
5. The time constant R2-C2 of the protection circuit should be selected approximately 0.7μs.
   Over current (OC) shutdown time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.
6. Please set the threshold voltage of the comparator reference input to be same as the IPM OC trip reference voltage $V_{IS(ref)}$.
7. Please use high speed type comparator and logic IC to detect OC condition quickly.
8. If negative voltage of R1 at the switching timing is applied, the schottky barrier diode D1 is recommended to be inserted parallel to R1.
9. All capacitors should be mounted as close to the terminals of the IPM as possible. (C1, C4 : narrow temperature drift, higher frequency and DC bias characteristic ceramic type are recommended, and C3, C5: narrow temperature drift, higher frequency and electrolytic type.)
10. To prevent surge destruction, the wiring between the snubber capacitor and the P terminal, Ns node should be as short as possible. Generally a 0.1μ to 0.22μF snubber capacitor (C6) between the P terminal and Ns node is recommended.
11. Two COM terminals (13 & 20 pin) are connected inside the IPM, it must be connected either one to the signal GND outside and leave another one open.
12. It is recommended to insert a zener-diode (22V) between each pair of control supply terminals to prevent surge destruction.
13. If signal GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect signal GND and power GND at only a point.

Fig.1-1 :
The measurement position of temperature sensor.

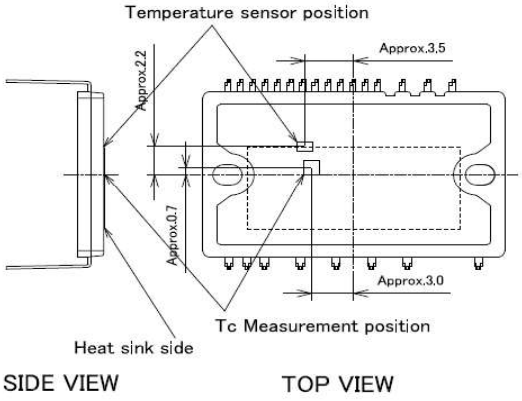


Fig.1-2 :
The measurement position of heat sink flatness.

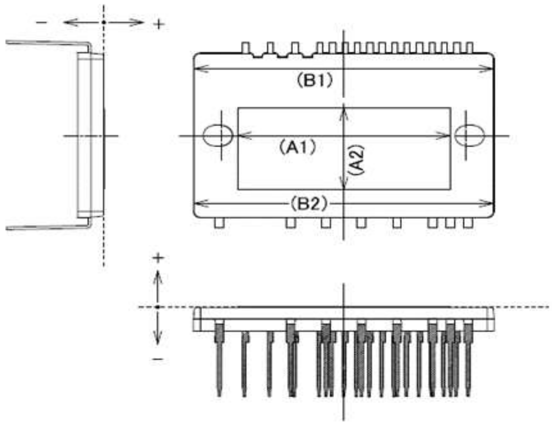
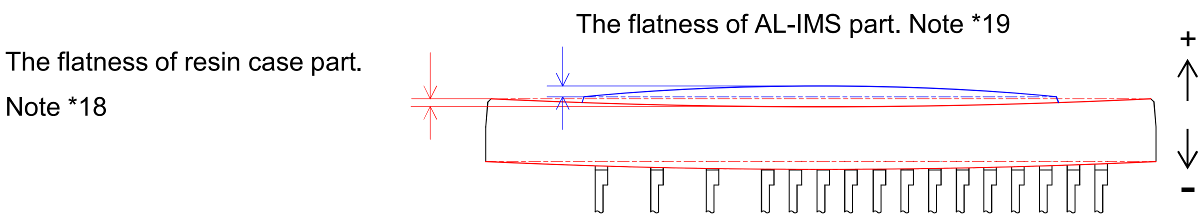


Fig.1-3 :
The magnified cross section image of warp direction.
* This image is a stretched drawing.(Not true scale)
* A positive value means the AL-IMS direction. A negative value means the marking surface direction.



Note

*18: The virtual datum level assumes a straight line to link both ends of the resin case.
*19 : The virtual datum level assumes a straight line to link both ends of the AL-IMS.

Fig.2-1 Switching waveforms

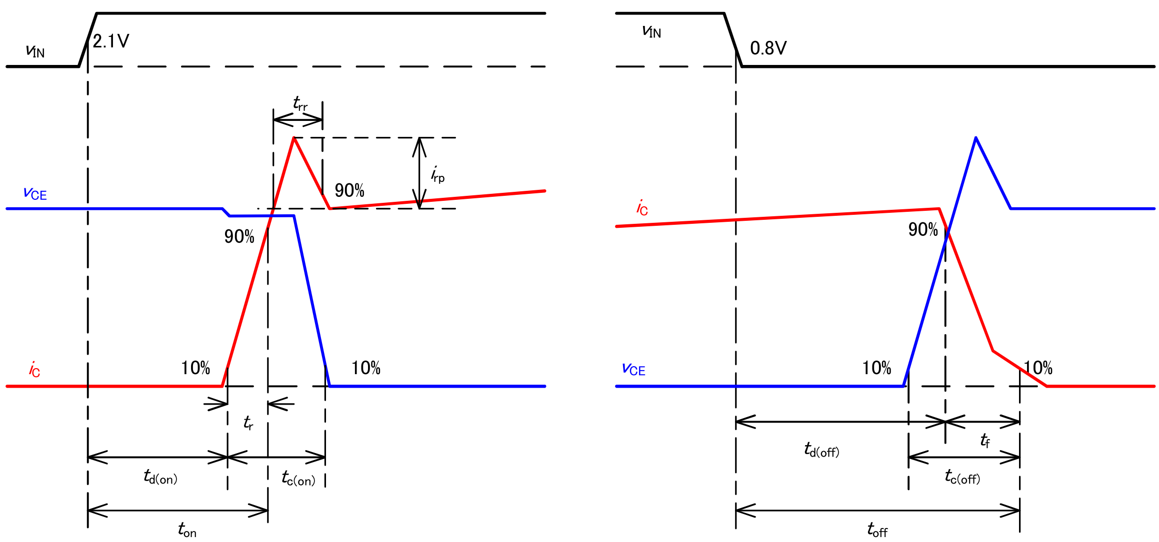


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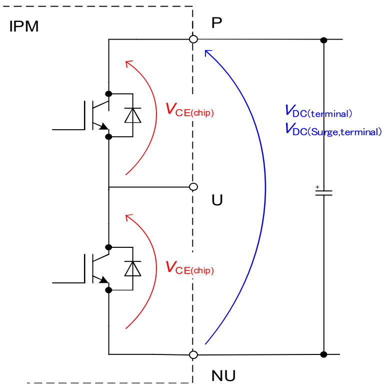
Fig.2-2 Rated voltage



・$V_{DC(terminal)}$, $V_{DC(Surge,terminal)}$ are applied between P-N(U),P-N(V),P-N(W) at the lead stopper.

・$V_{CE(chip)}$ is Collector-Emitter voltage of internal IGBT chip.

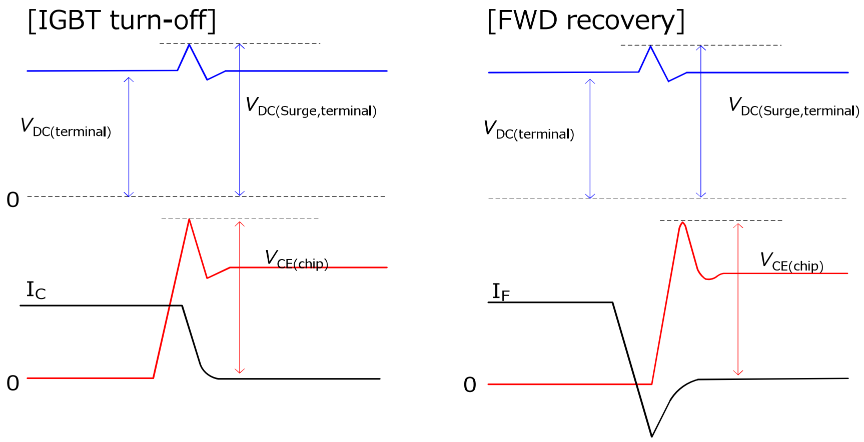
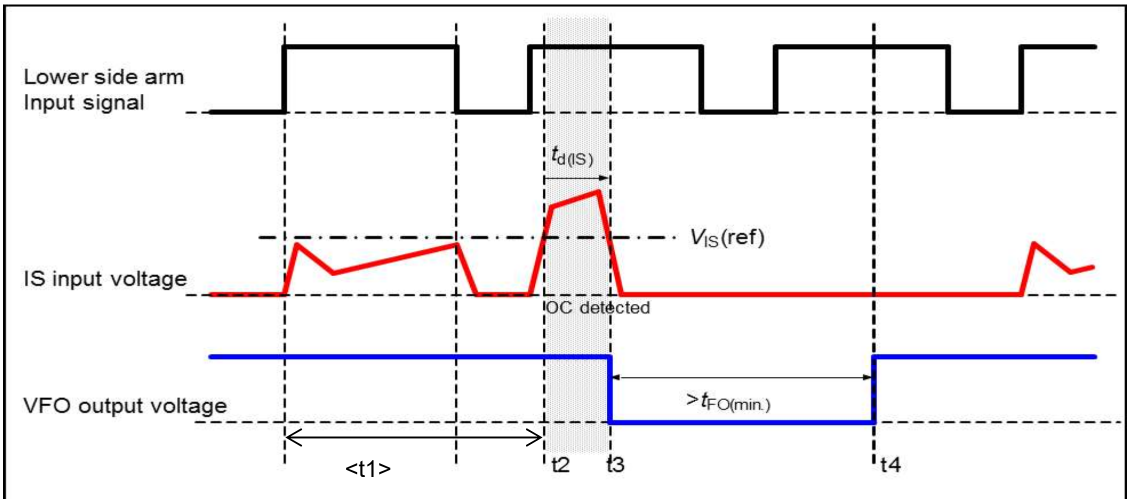


Fig.2-3 Operation sequence of over current protection



Operation sequence of over current protection

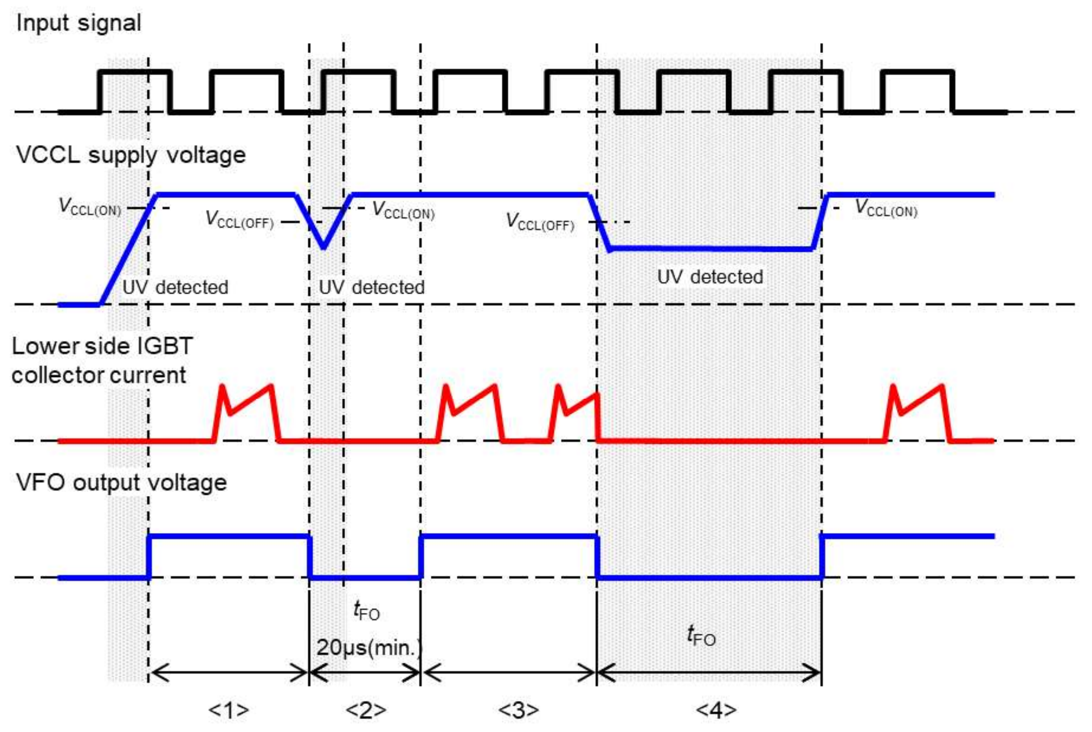
<t1> : IS input voltage does not exceed $V_{IS(ref)}$, while the collector current of the lower side IGBT is under the normal operation.

t2 : When is input voltage exceeds $V_{IS(ref)}$, the OC is detected.

t3 : The fault output VFO is activated and all lower side IGBT shut down simultaneously after the over current protection delay time $t_{d(IS)}$. Inherently there is dead time of LVIC in $t_{d(IS)}$.

t4 : After the fault output pulse width t_{FO}, the OC is reset. Then next input signal is activated.

Fig.2-4 Operation sequence of V_{CCL} under voltage protection (lower side arm)



Operation sequence of V_{CCL} under voltage protection (lower side arm)

When V_{CCL} is under 4V, UV and fault output are not activated.

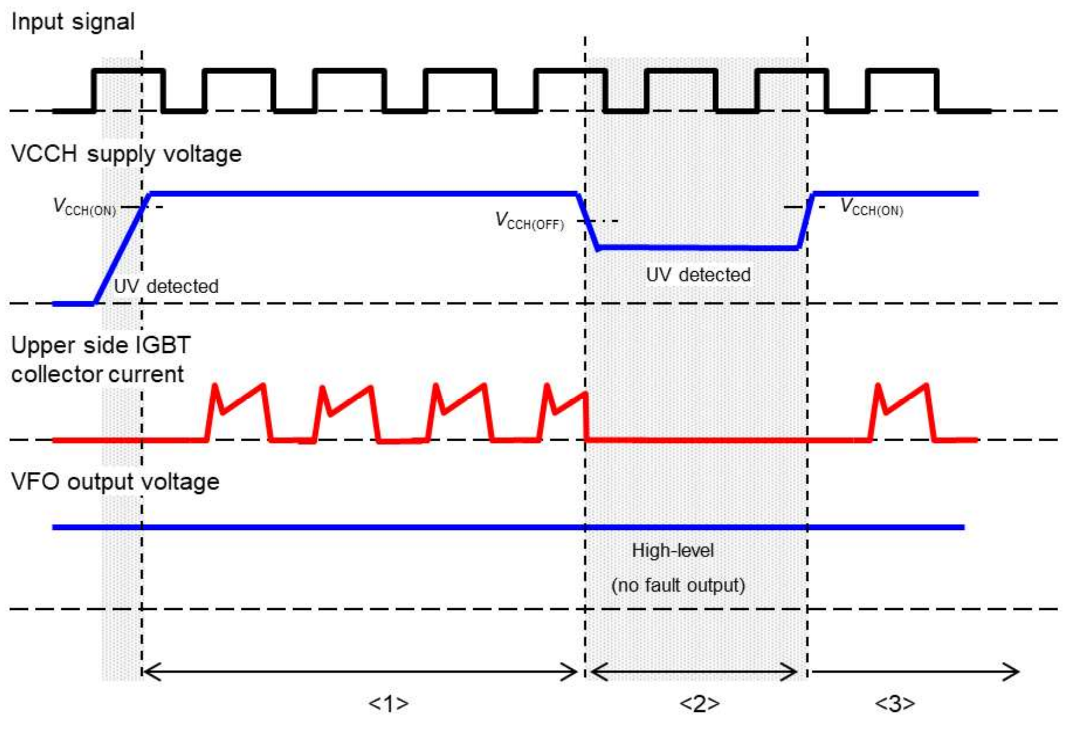
<1> When V_{CCL} is under $V_{CCL(ON)}$, all lower side IGBTs are OFF state.
After V_{CCL} rises to $V_{CCL(ON)}$, the fault output VFO is released (high level).
And the LVIC starts to operate, then next input is activated.

<2> The fault output VFO is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state.
When the voltage drop time is less than 20μs, the fault output pulse width is generated minimum 20μs and all lower side IGBTs are OFF state in spite of input signal condition during that time.

<3> UV is reset after t_{FO} when V_{CCL} exceeds $V_{CCL(ON)}$ and the fault output VFO is reset simultaneously.
And the LVIC starts to operate, then next input is activated.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state in spite of input signal condition during the same time.

Fig.2-5 Operation sequence of V_{CCH} under voltage protection (upper side arm)



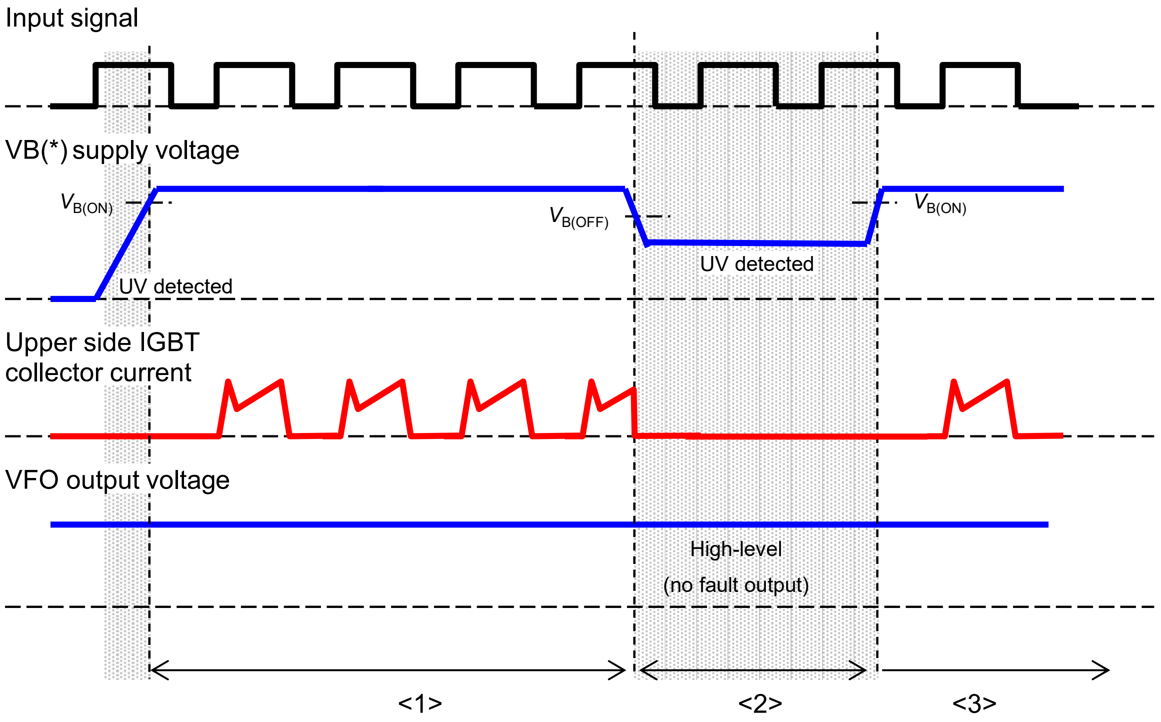
Operation sequence of V_{CCH} under voltage protection (upper side arm)

<1> When V_{CCH} is under $V_{CCH(ON)}$, the upper side IGBT is OFF state.
After V_{CCH} exceeds $V_{CCH(ON)}$, the HVIC starts to operate. Then next input is activated.
The fault output VFO is constant (high level) not depending on V_{CCH}.

<2> After V_{CCH} falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO remains at high level.

<3> The HVIC starts to operate after UV is reset, then next input is activated.

Fig.2-6 Operation sequence of $V_{B(*)}$ under voltage protection (upper side arm)



Operation sequence of $V_{B(*)}$(Note.*4) under voltage protection (upper side arm)

<1> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ are under $V_{B(ON)}$, the corresponding upper side IGBTs are OFF state.
After $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ exceed $V_{B(ON)}$, the corresponding upper side IGBTs start to operate.
Then next input is activated.
The fault output VFO is constant (high level) not depending on $V_{B(*)}$. (Note*20)

<2> After $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ fall below $V_{B(OFF)}$, the corresponding upper side IGBTs remain OFF state. But the fault output VFO keeps high level.

<3> The HVIC starts to operate after UV is reset, then next input is activated.

Note *20 : The fault output is not given HVIC bias conditions.

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