



40V P-Channel Enhancement Mode MOSFET

Voltage

-40 V

Current

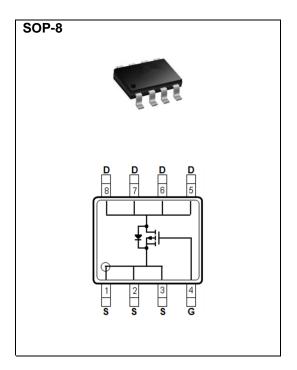
-8.8 A

Features

- R_{DS(ON)}, V_{GS}@-10V, I_D@-8A<17mΩ
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-4A<25m\Omega$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOP-8 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams



Maximum Ratings and Thermal Characteristics (T_A =25 $^{\circ}$ C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS		
Drain-Source Voltage		V _{DS}	-40	V	
Gate-Source Voltage		V_{GS}	<u>+</u> 20		
Continuous Drain Current (Note 3)	T _A =25°C	l _D	-8.8		
	T _A =70°C		-7	Α	
Pulsed Drain Current (Note 1)		I _{DM}	-35.2		
Power Dissipation	T _A =25°C	P _D	2.1	W	
	T _A =70°C		1.3		
Operating Junction and Storage Temperature Range		T_{J} , T_{STG}	-55~150	°C	
Typical Thermal Resistance - Junction to Ambient (Note 5)		$R_{ heta JA}$	59.5	°C/W	





Electrical Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS		
Static								
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-40	-	-	V		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=-250uA$	-1	-1.6	-2.5			
Drain-Source On-State Resistance	R _{DS(on)}	V_{GS} =-10V, I_D =-8A	-	14	17	mΩ		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-4A	-	20	25			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	-1	uA		
Gate-Source Leakage Current	I _{GSS}	V _{GS} = <u>+</u> 20V, V _{DS} =0V	-	-	<u>+</u> 100	nA		
Dynamic (Note 6)								
Total Gate Charge	Q_g	V _{DS} =-32V, I _D =-8A, V _{GS} =-4.5V ^(Note 1,2)	-	19	-	nC		
Gate-Source Charge	Q_gs		-	5.3	-			
Gate-Drain Charge	Q_gd		-	6.6	-			
Input Capacitance	Ciss	V _{DS} =-25V, V _{GS} =0V, f=1MHZ	-	2030	-	pF		
Output Capacitance	Coss		-	190	-			
Reverse Transfer Capacitance	Crss		-	139	-			
Turn-On Delay Time	td _(on)	V_{DS} =-20V, I_{D} =-1A, V_{GS} =-10V, R_{G} =6 Ω (Note 1,2)	-	8.6	-	ns		
Turn-On Rise Time	tr		-	9.6	-			
Turn-Off Delay Time	td _(off)		-	77	-			
Turn-Off Fall Time	tf		-	39	-			
Drain-Source Diode								
Maximum Continuous Drain-Source	l _s		_	-	-8.8	А		
Diode Forward Current	'S		_					
Diode Forward Voltage	V_{SD}	I _S =-1A, V _{GS} =0V	-	-0.7	-1	V		

NOTES:

- 1. Pulse width<300us, Duty cycle<2%.
- 2. Essentially independent of operating temperature typical characteristics.
- 3. The maximum current rating is package limited.
- 4. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
- 5. R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 6. Guaranteed by design, not subject to production testing.





TYPICAL CHARACTERISTIC CURVES

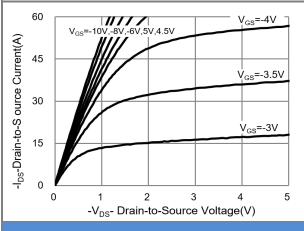


Fig.1 On-Region Characteristics

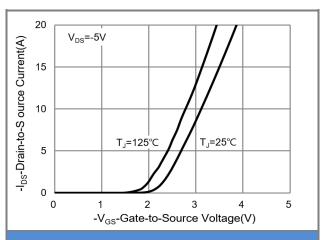


Fig.2 Transfer Characteristics

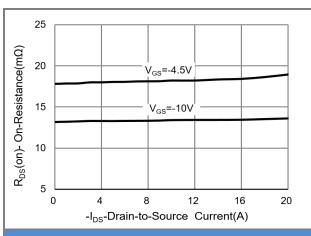


Fig.3 On-Resistance vs. Drain Current

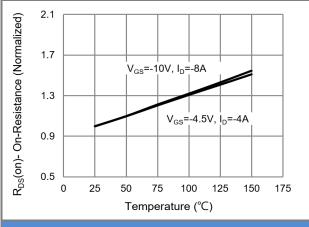


Fig.4 On-Resistance vs. Junction temperature

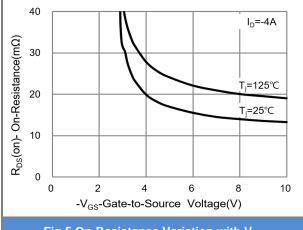


Fig.5 On-Resistance Variation with V_{GS}

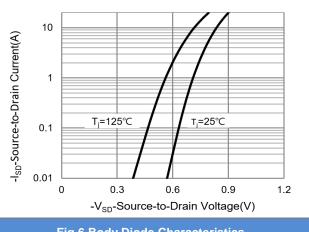


Fig.6 Body Diode Characteristics





TYPICAL CHARACTERISTIC CURVES

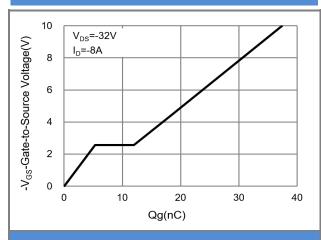


Fig.7 Gate-Charge Characteristics

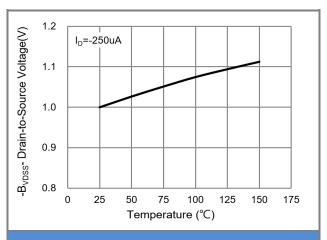


Fig.8 Breakdown Voltage Variation vs. Temperature

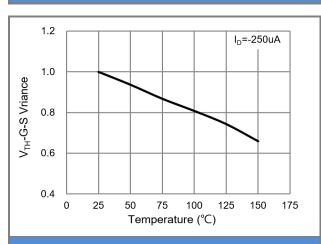


Fig.9 Threshold Voltage Variation with Temperature

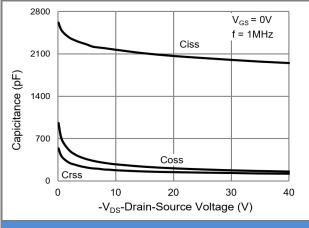


Fig.10 Capacitance vs. Drain-Source Voltage

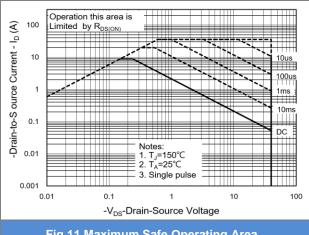


Fig.11 Maximum Safe Operating Area

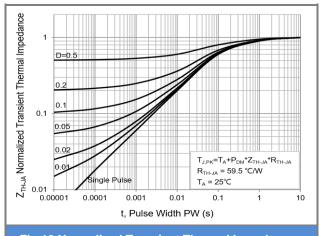


Fig.12 Normalized Transient Thermal Impedance

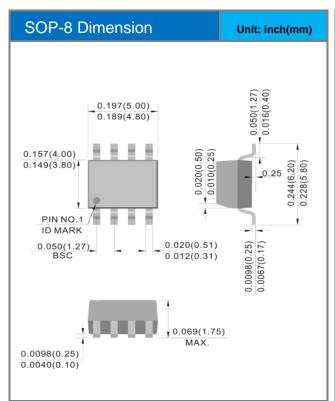


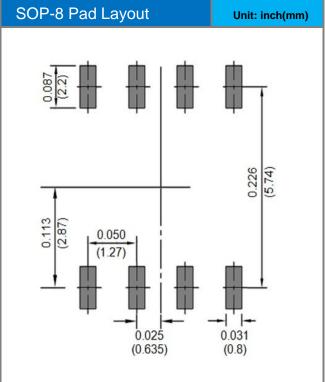


Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJL9421_R2_00001	SOP-8	2.5K pcs / 13" reel	L9421	Halogen free

Packaging Information & Mounting Pad Layout









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