

# PJQ5524

## 30V N-Channel Enhancement Mode MOSFET

**Voltage**

**30 V**

**Current**

**85 A**

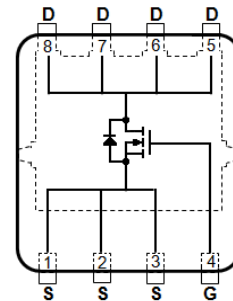
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@20A < 3.6m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@20A < 6.1m\Omega$
- Excellent FOM
- Logic Level Drive
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case : DFN5060X-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.087 grams

DFN5060X-8L



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

| PARAMETER   |                         | SYMBOL          | LIMIT    | UNITS              |
|---|-------------------------|-----------------|----------|--------------------|
| Drain-Source Voltage                              |                         | $V_{DS}$        | 30       | V                  |
| Gate-Source Voltage                               |                         | $V_{GS}$        | $\pm 20$ |                    |
| Continuous Drain Current <sup>(Note 3)</sup>      | $T_C=25^\circ\text{C}$  | $I_D$           | 85       | A                  |
|   | $T_C=100^\circ\text{C}$ |                 | 54       |                    |
| Pulsed Drain Current <sup>(Note 1)</sup>          | $T_C=25^\circ\text{C}$  | $I_{DM}$        | 340      |                    |
| Power Dissipation                                 | $T_C=25^\circ\text{C}$  | $P_D$           | 41.7     | W                  |
|   | $T_C=100^\circ\text{C}$ |                 | 16.7     |                    |
| Continuous Drain Current <sup>(Note 4)</sup>      | $T_A=25^\circ\text{C}$  | $I_D$           | 22       | A                  |
|   | $T_A=70^\circ\text{C}$  |                 | 18       |                    |
| Power Dissipation                                 | $T_A=25^\circ\text{C}$  | $P_D$           | 2.8      | W                  |
|   | $T_A=70^\circ\text{C}$  |                 | 1.8      |                    |
| Single Pulse Avalanche Energy <sup>(Note 5)</sup> |                         | $E_{AS}$        | 46       | mJ                 |
| Operating Junction and Storage Temperature Range  |                         | $T_J, T_{STG}$  | -55~150  | $^\circ\text{C}$   |
| Thermal Resistance <sup>(Note 4)</sup>            | Junction to Case        | $R_{\theta JC}$ | 3        | $^\circ\text{C/W}$ |
|   | Junction to Ambient     | $R_{\theta JA}$ | 45       |                    |

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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

| PARAMETER                        | SYMBOL              | TEST CONDITION   | MIN. | TYP. | MAX. | UNITS |
|----------------------------------|---------------------|--|------|------|------|-------|
| <b>Static</b>                    |                     |  |      |      |      |       |
| Drain-Source Breakdown Voltage   | BV <sub>DSS</sub>   | V <sub>GS</sub> =0V, I <sub>D</sub> =250uA   | 30   | -    | -    | V     |
| Gate Threshold Voltage           | V <sub>GS(th)</sub> | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA   | 1.3  | 1.7  | 2.5  |       |
| Drain-Source On-State Resistance | R <sub>DS(on)</sub> | V <sub>GS</sub> =10V, I <sub>D</sub> =20A  | -    | 3    | 3.6  | mΩ    |
|                                  |                     | V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A   | -    | 4.7  | 6.1  |       |
| Zero Gate Voltage Drain Current  | I <sub>DSS</sub>    | V <sub>DS</sub> =30V, V <sub>GS</sub> =0V  | -    | -    | ±1   | uA    |
| Gate-Source Leakage Current      | I <sub>GSS</sub>    | V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V   | -    | -    | ±100 | nA    |
| <b>Dynamic</b> (Note 6)          |                     |  |      |      |      |       |
| Total Gate Charge                | Q <sub>g</sub>      | V <sub>DS</sub> =24V, I <sub>D</sub> =20A,<br>V <sub>GS</sub> =10V                                 | -    | 21   | -    | nC    |
| Gate-Source Charge               | Q <sub>gs</sub>     |  | -    | 3.6  | -    |       |
| Gate-Drain Charge                | Q <sub>gd</sub>     |  | -    | 3.2  | -    |       |
| Input Capacitance                | C <sub>iss</sub>    | V <sub>DS</sub> =25V, V <sub>GS</sub> =0V,<br>f=1MHz   | -    | 1260 | -    | pF    |
| Output Capacitance               | C <sub>oss</sub>    |  | -    | 560  | -    |       |
| Reverse Transfer Capacitance     | C <sub>rss</sub>    |  | -    | 44   | -    |       |
| Gate resistance                  | R <sub>g</sub>      | f=1MHz   | -    | 0.85 | -    | Ω     |
| Turn-On Delay Time               | t <sub>d(on)</sub>  | V <sub>DS</sub> =24V, I <sub>D</sub> =20A,<br>V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω<br>(Note 2) | -    | 15   | -    | ns    |
| Turn-On Rise Time                | t <sub>r</sub>      |  | -    | 26   | -    |       |
| Turn-Off Delay Time              | t <sub>d(off)</sub> |  | -    | 24   | -    |       |
| Turn-Off Fall Time               | t <sub>f</sub>      |  | -    | 5    | -    |       |
| <b>Drain-Source Diode</b>        |                     |  |      |      |      |       |
| Diode Forward Current            | I <sub>S</sub>      | T <sub>C</sub> =25°C   | -    | -    | 85   | A     |
| Pulsed Diode Forward Current     | I <sub>SM</sub>     |  | -    | -    | 340  |       |
| Diode Forward Voltage            | V <sub>SD</sub>     | I <sub>S</sub> =20A, V <sub>GS</sub> =0V   | -    | 0.85 | 1.1  | V     |
| Reverse Recovery Time            | T <sub>rr</sub>     | V <sub>GS</sub> =0V, I <sub>S</sub> =20A   | -    | 31   | -    | ns    |
| Reverse Recovery Charge          | Q <sub>rr</sub>     | dI <sub>S</sub> /dt=100A/us  | -    | 19   | -    | nC    |

**NOTES :**

1. Pulse width ≤ 100us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R<sub>θJC</sub>=3°C/W.
4. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
5. The test condition is L=0.5mH, I<sub>AS</sub>=14A, V<sub>DD</sub>=30V, V<sub>GS</sub>=10V, Starting T<sub>J</sub>=25°C. the chip is about to carry I<sub>AS</sub>≈27A.
6. Guaranteed by design, not subject to production testing.

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## TYPICAL CHARACTERISTIC CURVES

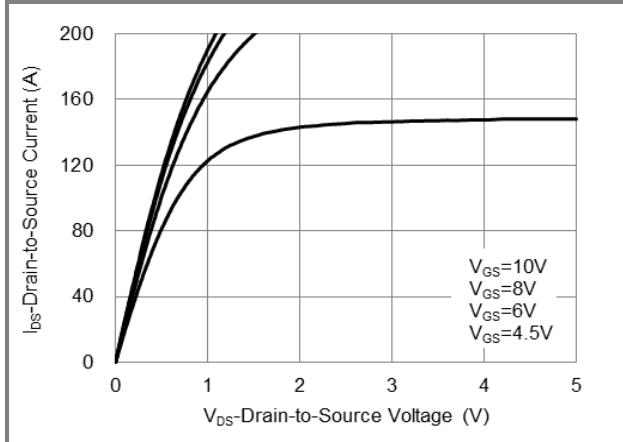


Fig.1 On-Region Characteristics

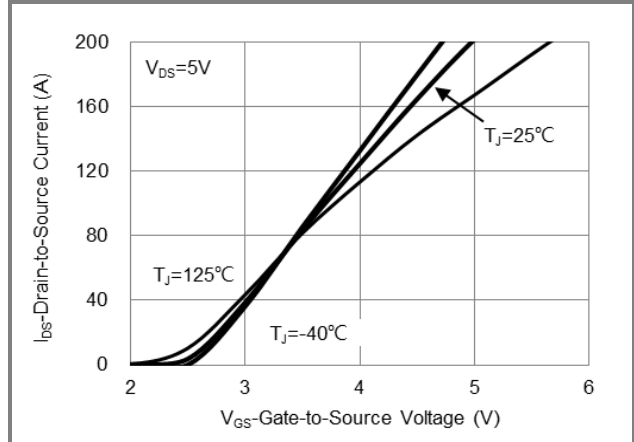


Fig.2 Transfer Characteristics

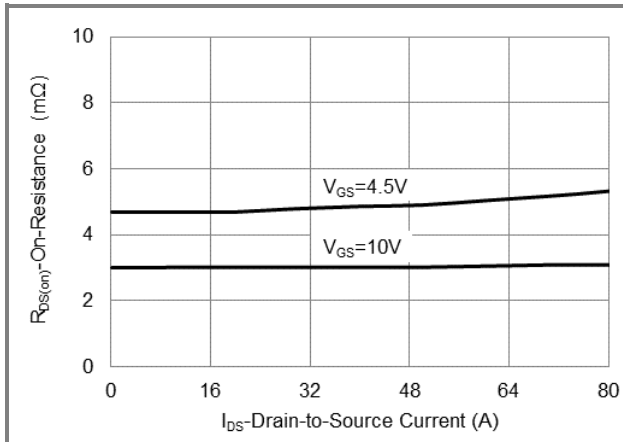


Fig.3 On-Resistance vs. Drain Current

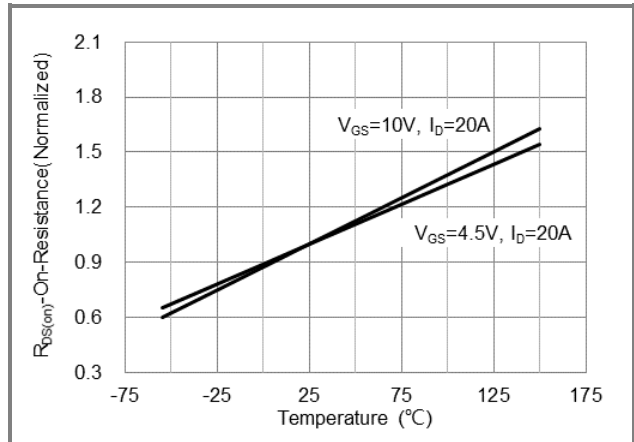


Fig.4 On-Resistance vs. Junction temperature

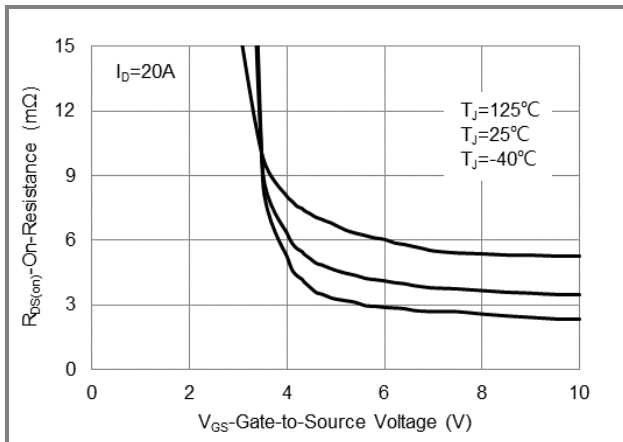


Fig.5 On-Resistance Variation with Vgs

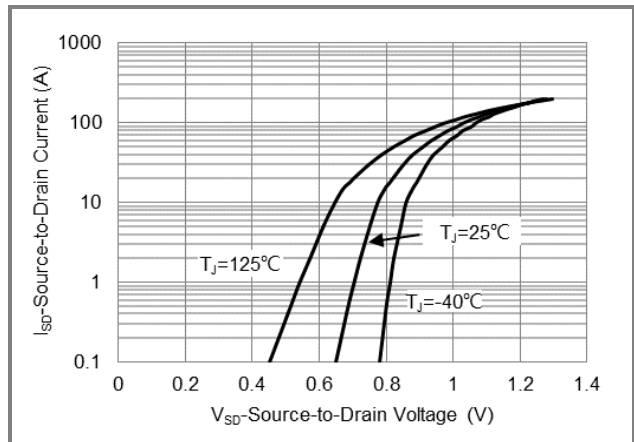


Fig.6 Source-Drain Diode Forward Voltage

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## TYPICAL CHARACTERISTIC CURVES

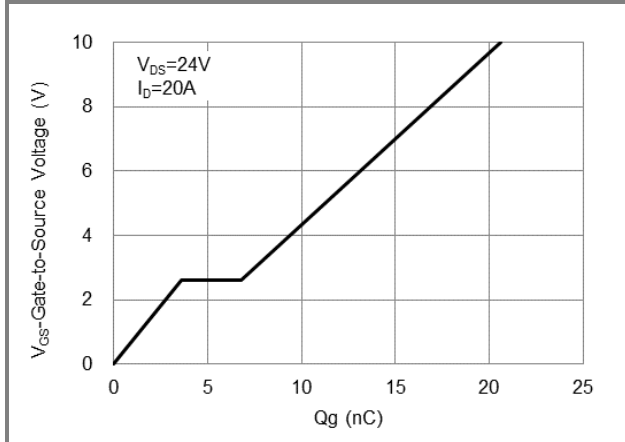


Fig.7 Gate-Charge Characteristics

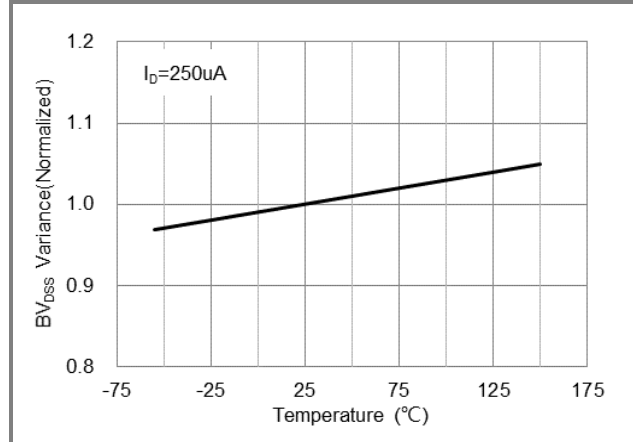


Fig.8 Breakdown Voltage Variation vs. Temperature

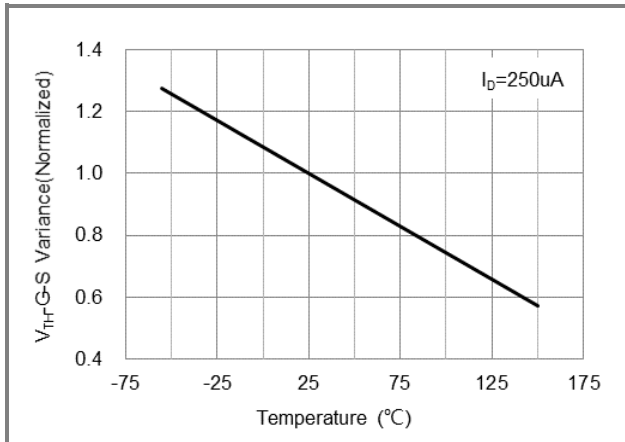


Fig.9 Threshold Voltage Variation with Temperature

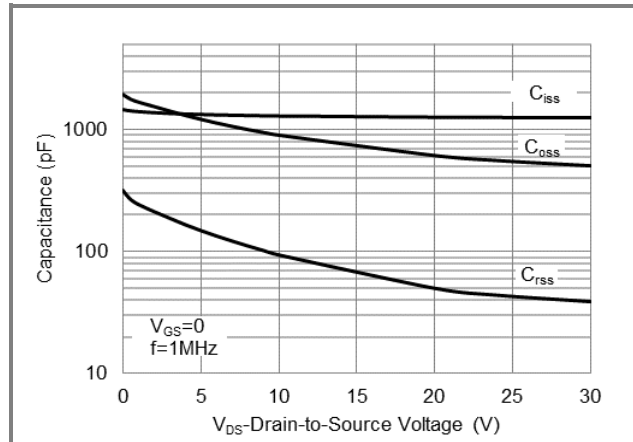


Fig.10 Capacitance vs. Drain-Source Voltage

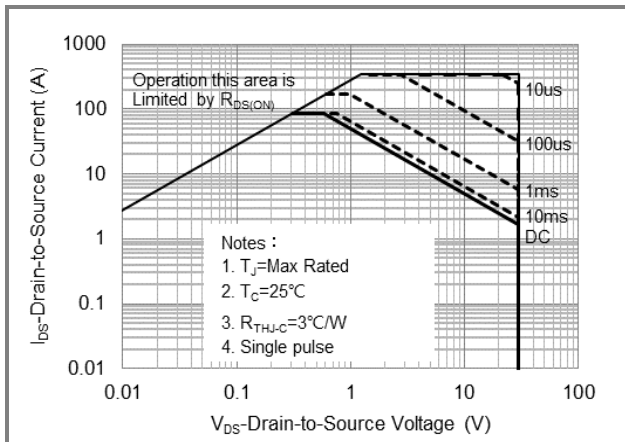


Fig.11 Maximum Safe Operating Area

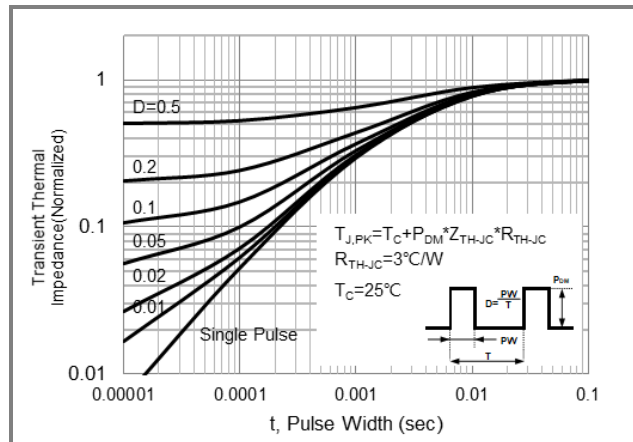


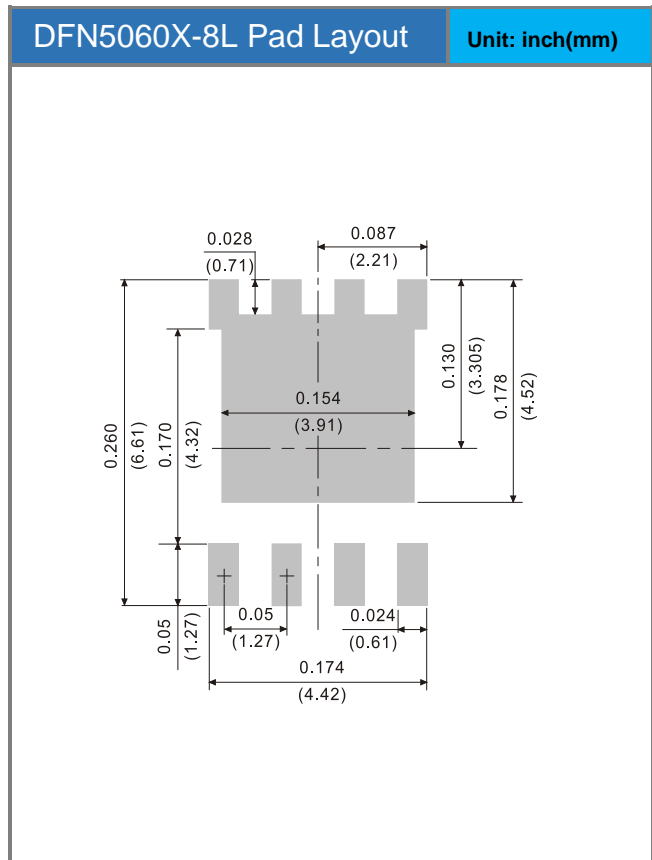
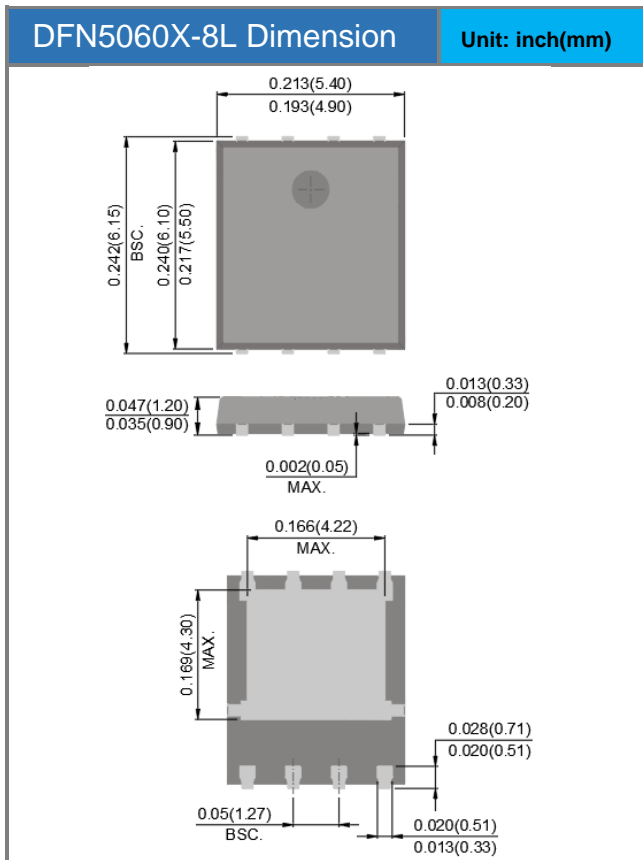
Fig.12 Normalized Transient Thermal Impedance

# PJQ5524

## Product and Packing Information

| Part No. | Package Type | Packing Type      | Marking |
|----------|--------------|-------------------|---------|
| PJQ5524  | DFN5060X-8L  | 3K pcs / 13" reel | Q5524   |

## Packaging Information & Mounting Pad Layout



## PJQ5524

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