



PJQ5441

40V P-Channel Enhancement Mode MOSFET

Voltage

-40V

Current

-80A

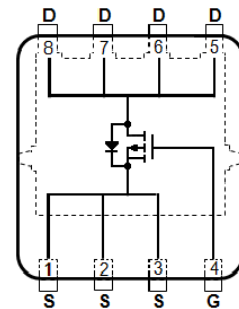
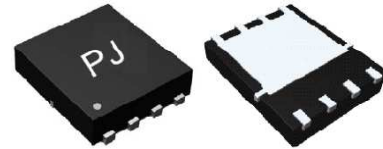
Features

- $R_{DS(ON)}$, $V_{GS}@-10V, I_D@-20A < 6.5m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V, I_D@-10A < 9m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0028 ounces, 0.08 grams

DFN5060-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 4)	$T_C=25^\circ\text{C}$	I_D	-80	A
	$T_C=100^\circ\text{C}$		-50	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	-300	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	69	W
	$T_C=100^\circ\text{C}$		28	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	-17	A
	$T_A=70^\circ\text{C}$		-14	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	3.1	W
	$T_A=70^\circ\text{C}$		2.0	
Single Pulse Avalanche Energy ^(Note 6)		E_{AS}	245	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Typical Thermal Resistance ^(Note 5)	Junction to Case	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	40	



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1	-1.4	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-20A	-	4.5	6.5	mΩ
		V _{GS} =4.5V, I _D =-10A	-	6	9	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	-1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 7)						
Total Gate Charge	Q _g	V _{DS} =-32V, I _D =-10A, V _{GS} =-10V (Note 2,3)	-	128	-	nC
Gate-Source Charge	Q _{gs}		-	15	-	
Gate-Drain Charge	Q _{gd}		-	29	-	
Input Capacitance	C _{iss}	V _{DS} =-25V, V _{GS} =0V, f=1MHZ	-	6324	-	pF
Output Capacitance	C _{oss}		-	548	-	
Reverse Transfer Capacitance	C _{rss}		-	292	-	
Gate resistance	R _g	f=1MHZ	-	3.7	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} =-32V, I _D =-1A, V _{GS} =-10V, R _G =6Ω (Note 2,3)	-	12	-	ns
Turn-On Rise Time	t _r		-	19	-	
Turn-Off Delay Time	t _{d(off)}		-	241	-	
Turn-Off Fall Time	t _f		-	91	-	
Drain-Source Diode						
Diode Forward Current	I _S	---	-	-	-85	A
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V	-	-0.67	-1	V

NOTES :

1. Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
4. The maximum current rating is package limited.
5. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. The test condition is L=0.1mH, I_{AS}=-70A, V_{DD}=-25V, V_{GS}=-10V, Starting T_J=25°C.
7. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

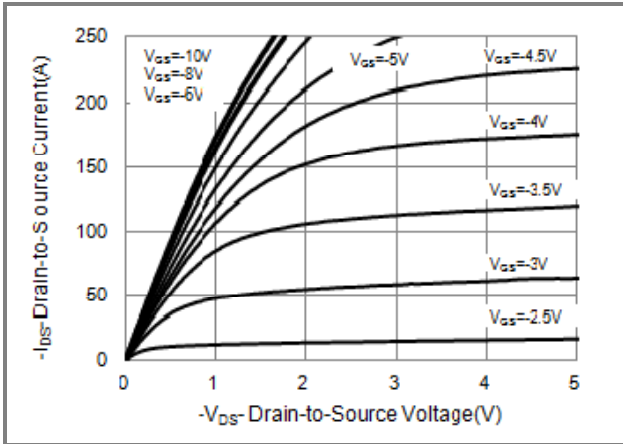


Fig.1 Output Characteristics

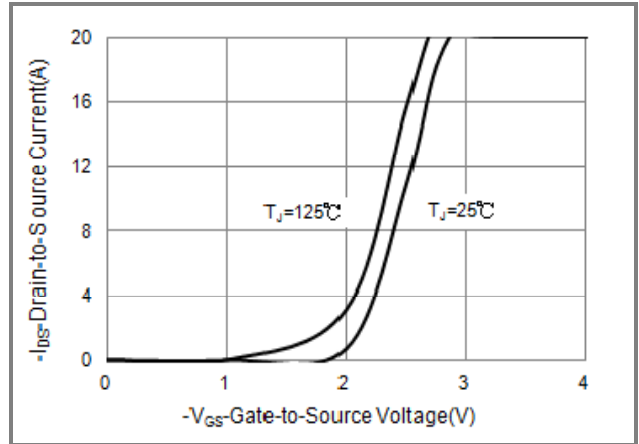


Fig.2 Transfer Characteristics

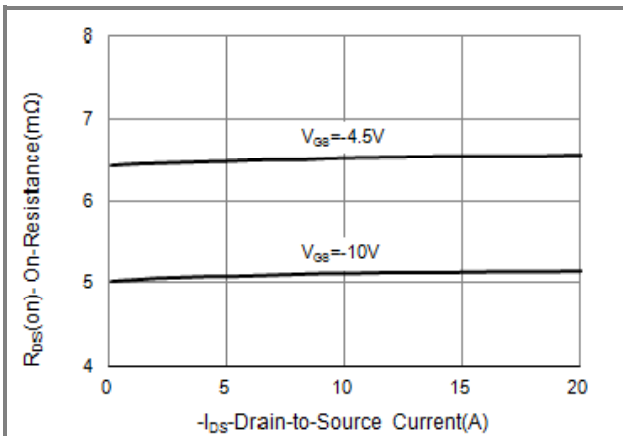


Fig.3 On-Resistance vs. Drain Current

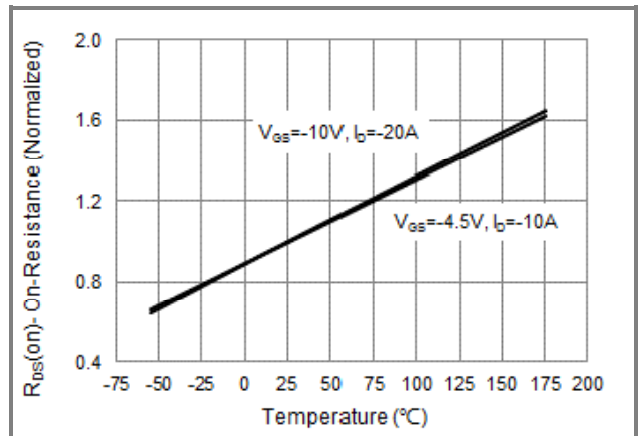


Fig.4 On-Resistance vs. Junction temperature

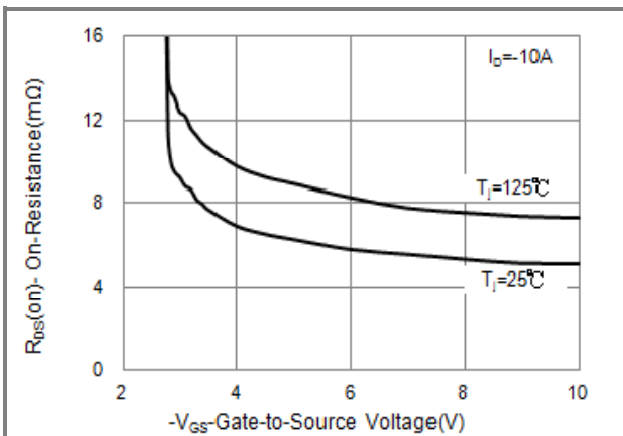


Fig.5 On-Resistance Variation with V_{GS}

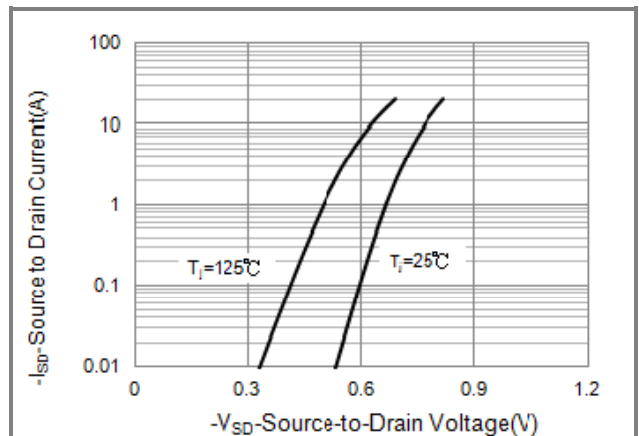


Fig.6 Source-Drain Diode Forward Voltage



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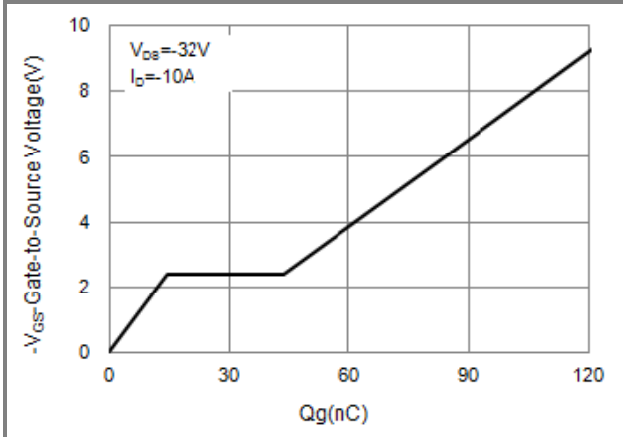


Fig.7 Gate-Charge Characteristics

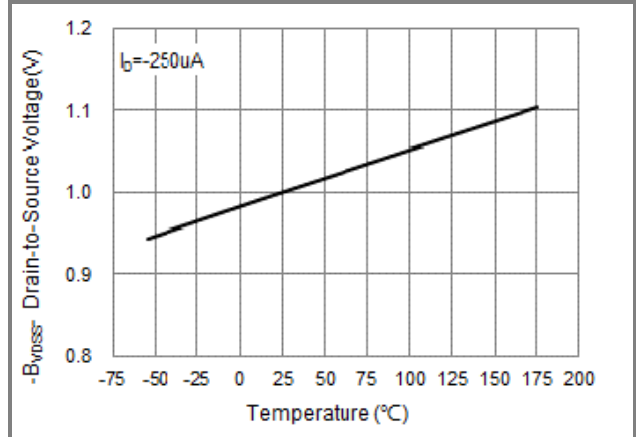


Fig.8 Breakdown Voltage Variation vs. Temperature

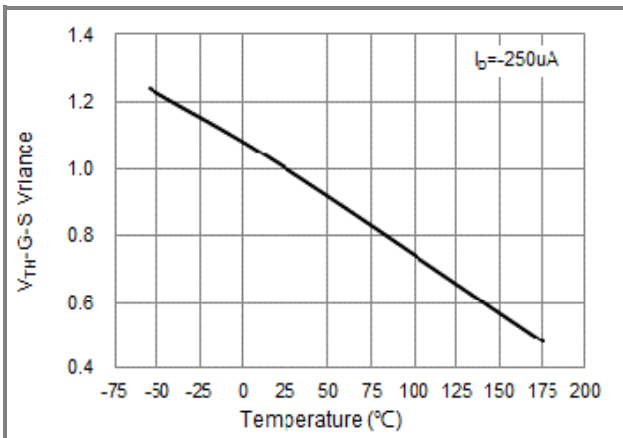


Fig.9 Threshold Voltage Variation with Temperature

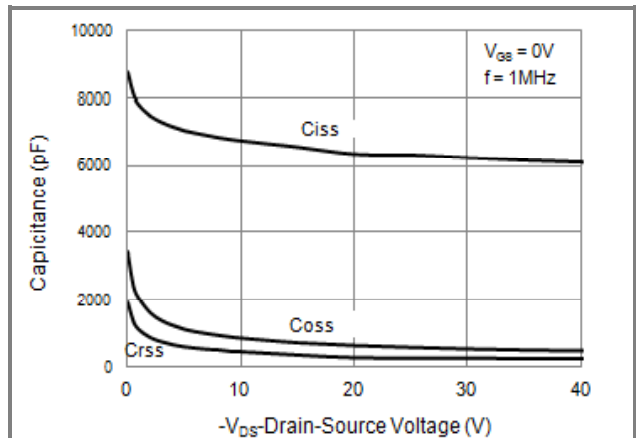


Fig.10 Capacitance vs. Drain-Source Voltage

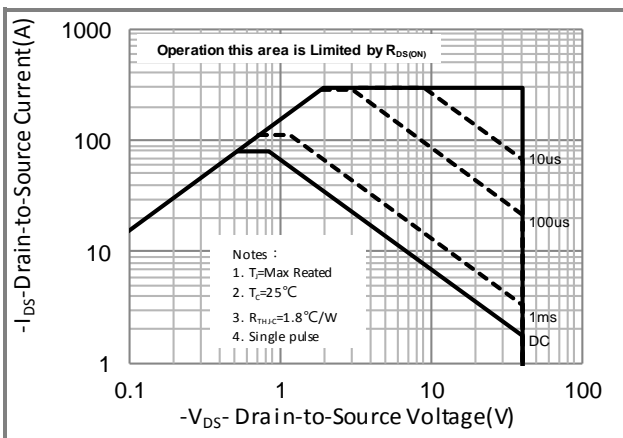


Fig.11 Maximum Safe Operating Area

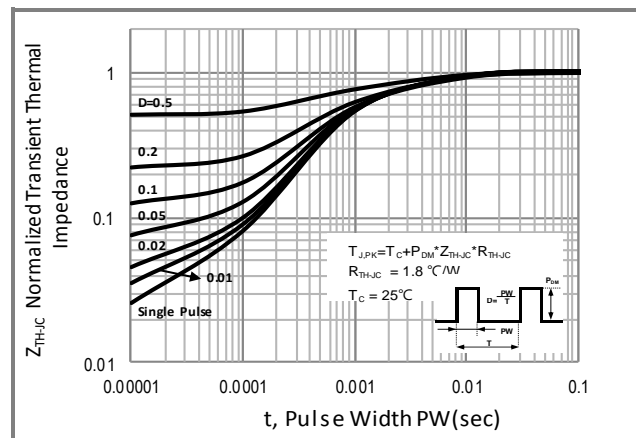


Fig.12 Normalized Transient Thermal Impedance



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