

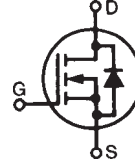
PolarHV™
Power MOSFET
ISOPLUS220™

IXTC 26N50P

V_{DSS} = 500 V
I_{D25} = 15 A
R_{DS(on)} ≤ 260 mΩ

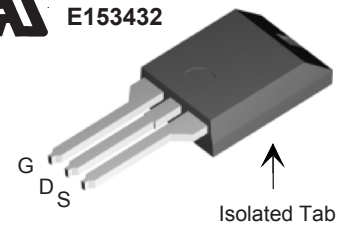
(Electrically Isolated Tab)

N-Channel Enhancement Mode
 Avalanche Rated



Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25° C to 150° C	500	V
V _{DGR}	T _J = 25° C to 150° C; R _{GS} = 1 MΩ	500	V
V _{GS}	Continuous	±30	V
V _{GSM}	Transient	±40	V
I _{D25}	T _C = 25° C	15	A
I _{DM}	T _C = 25° C, pulse width limited by T _{JM}	78	A
I _{AR}	T _C = 25° C	26	A
E _{AR}	T _C = 25° C	40	mJ
E _{AS}	T _C = 25° C	1.0	J
dv/dt	I _S ≤ I _{DM} , di/dt ≤ 100 A/μs, V _{DD} ≤ V _{DSS} , T _J ≤ 150° C, R _G = 4 Ω	10	V/ns
P _D	T _C = 25° C	130	W
T _J		-55 ... +150	°C
T _{JM}		150	°C
T _{stg}		-55 ... +150	°C
T _L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V _{ISOL}	50/60 Hz, RMS, t = 1, leads-to-tab	2500	V~
F _C	Mounting Force	11..65/2.5..15	N/lb
Weight		2	g

ISOPLUS220™ (IXTC)
E153432



G = Gate D = Drain
 S = Source

Features

- † Silicon chip on Direct-Copper-Bond substrate
- High power dissipation
- Isolated mounting surface
- 2500V electrical isolation
- † Low drain to tab capacitance(<30pF)

Applications

- † DC-DC converters
- † Battery chargers
- † Switched-mode and resonant-mode power supplies
- † DC choppers
- † AC motor control

Advantages

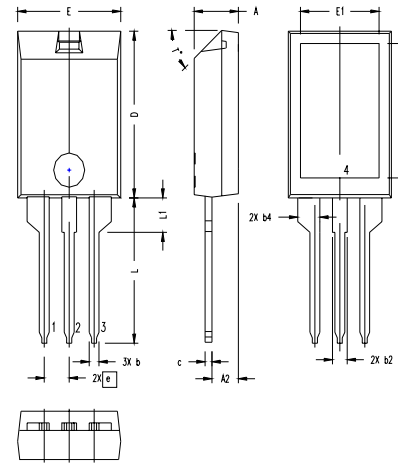
- † Easy assembly
- † Space savings
- † High power density

Symbol	Test Conditions (T _J = 25° C, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV _{DSS}	V _{GS} = 0 V, I _D = 250 μA	500		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	3.0		5.5 V
I _{GSS}	V _{GS} = ±30 V _{DC} , V _{DS} = 0			±100 nA
I _{DSS}	V _{DS} = V _{DSS} V _{GS} = 0 V T _J = 125° C			25 μA 250 μA
R _{DS(on)}	V _{GS} = 10 V, I _D = 13A Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			260 mΩ

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		Min.	Typ.	Max.
g_{fs}	V _{DS} = 10 V; I _D = 13A, pulse test	20	28	S
C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		3600	pF
C_{oss}			380	pF
C_{rss}			48	pF
t_{d(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 13A R _G = 4 Ω (External)		20	ns
t_r			25	ns
t_{d(off)}			58	ns
t_f			20	ns
Q_{g(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 13A		65	nC
Q_{gs}			20	nC
Q_{gd}			20	nC
R_{thJC}				0.95°C/W
R_{thCS}		0.21		°C/W

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		Min.	Typ.	Max.
I_S	V _{GS} = 0 V			15 A
I_{SM}	Repetitive			78 A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5 V
t_{rr}	I _F = 25 A -di/dt = 100 A/μs		400	ns
Q_{RM}		V _R = 100 V, V _{GS} = 0 V		5.0

ISOPLUS220 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T*			42.5*	47.5*

NOTE:
 1. Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
 2. This drawing will meet dimensional requirement of JEDEC SS Product Outline 10-273 except D and D1 dimension.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405B2	6,759,692
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2

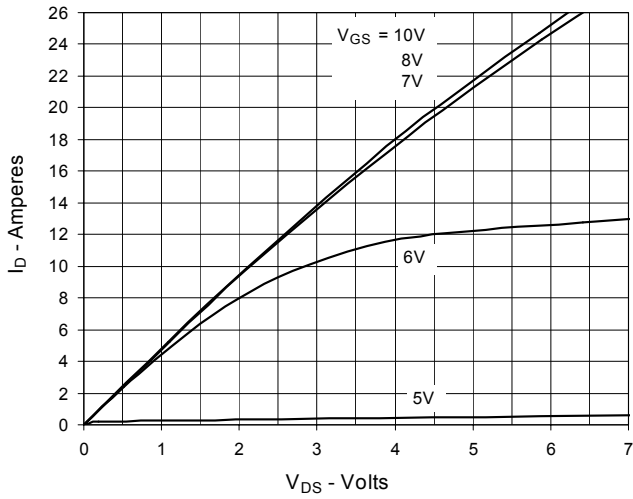
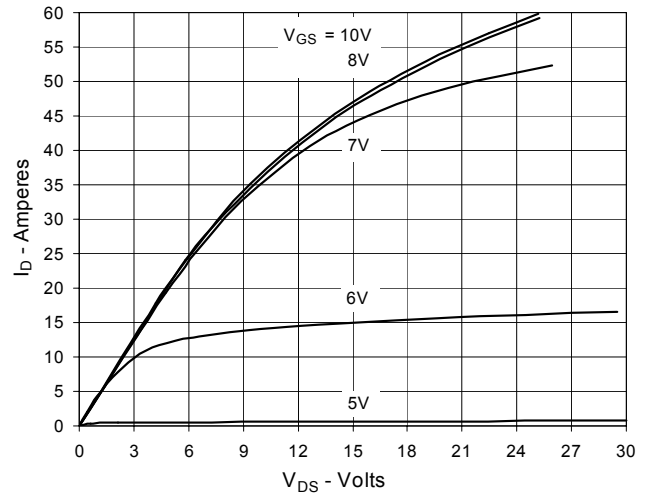
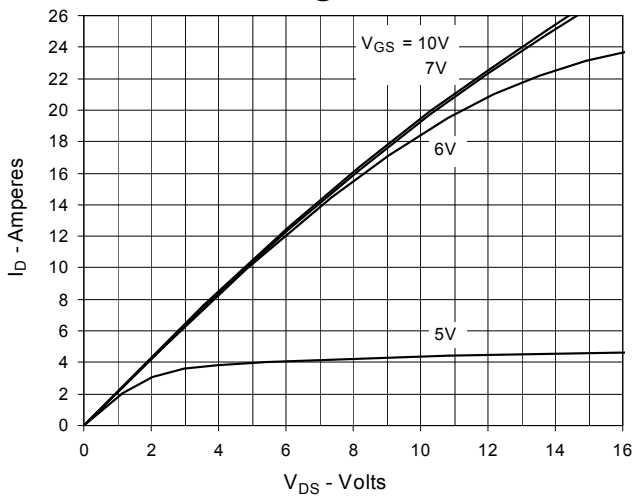
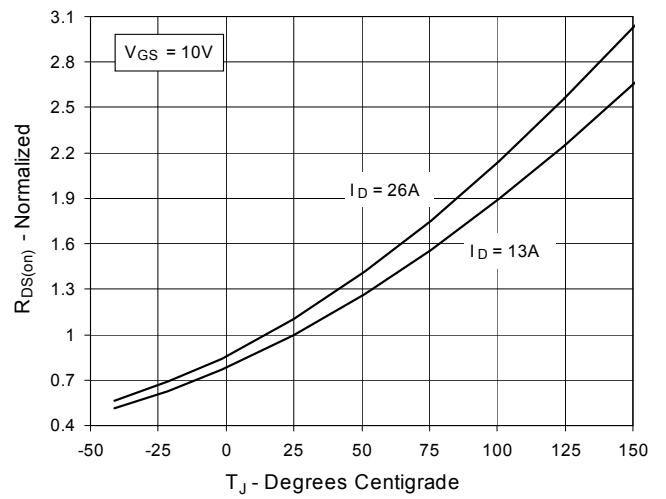
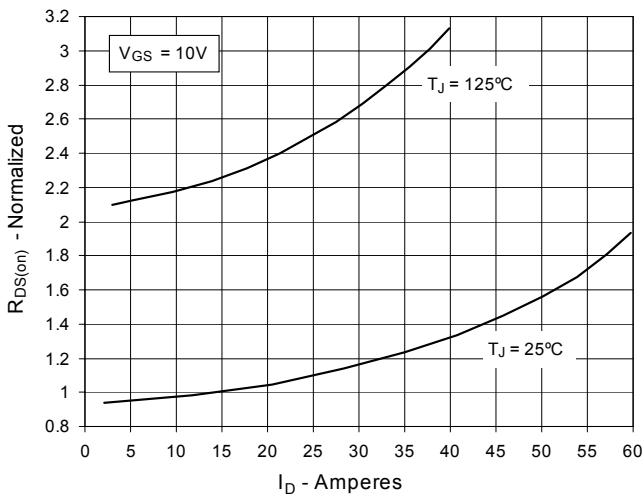
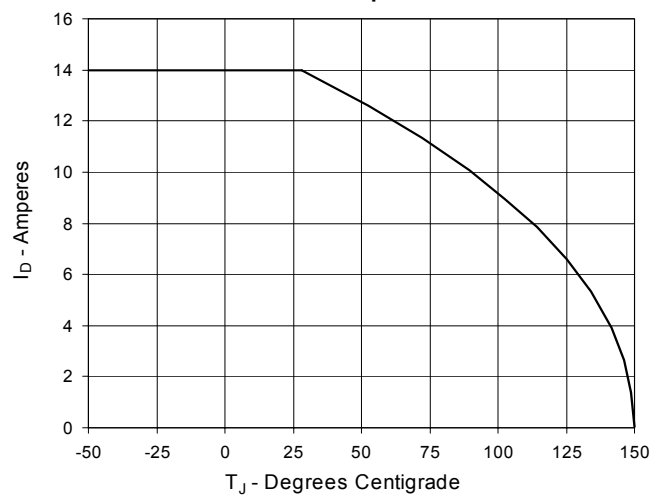
**Fig. 1. Output Characteristics
@ 25°C**

**Fig. 2. Extended Output Characteristics
@ 25°C**

**Fig. 3. Output Characteristics
@ 125°C**

**Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 13A$ Value
vs. Junction Temperature**

**Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 13A$ Value
vs. Drain Current**

**Fig. 6. Maximum Drain Current vs.
Case Temperature**


Fig. 7. Input Admittance

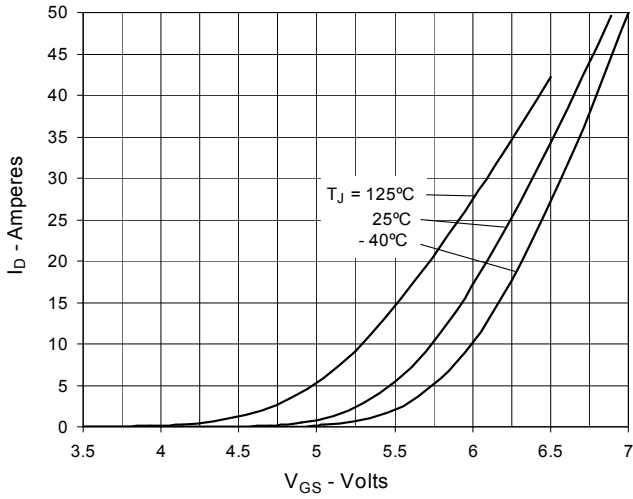


Fig. 8. Transconductance

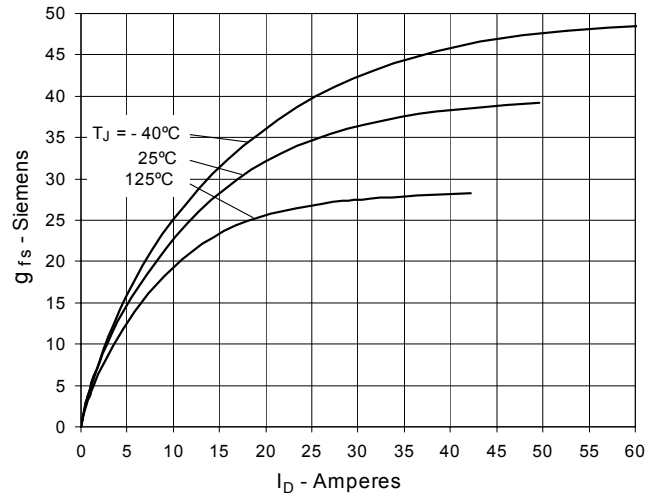


Fig. 9. Forward Voltage Drop of Intrinsic Diode

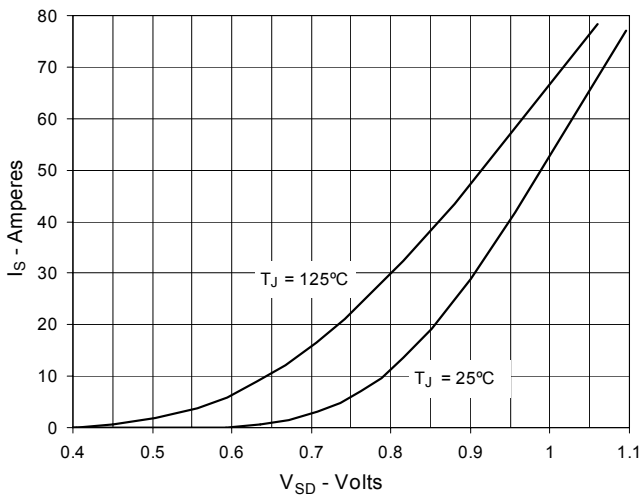


Fig. 10. Gate Charge

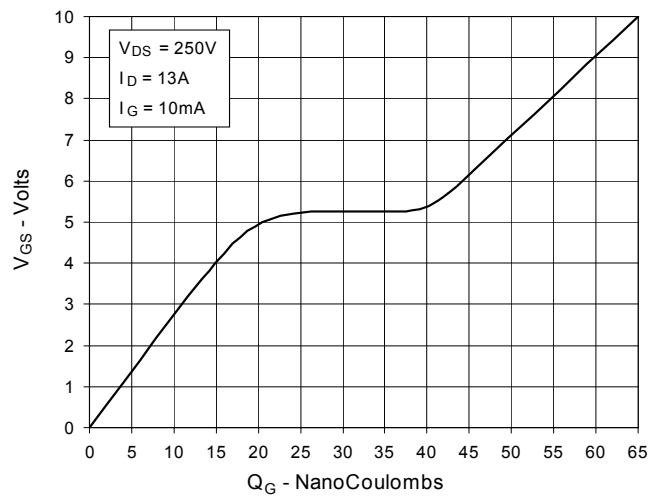


Fig. 11. Capacitance

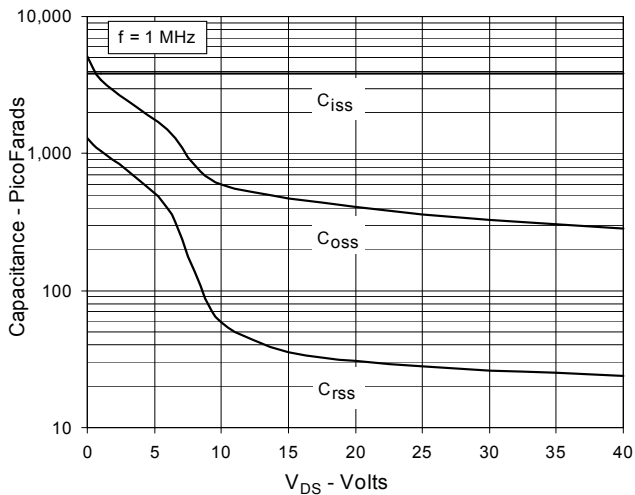


Fig. 12. Forward-Bias Safe Operating Area

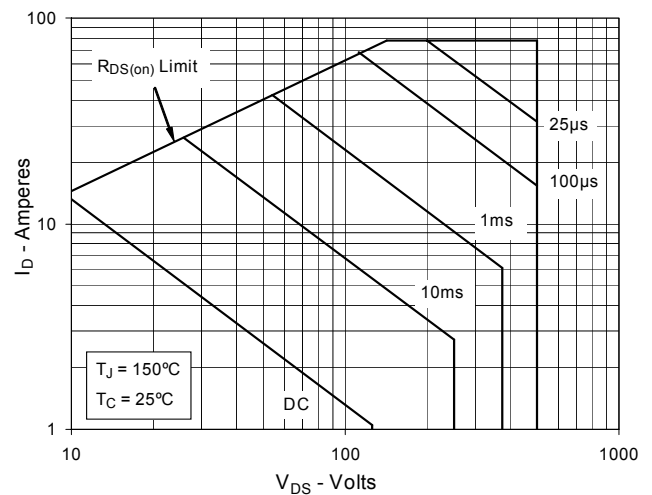


Fig. 13. Maximum Transient Thermal Resistance

