

MC74HCT541A

Octal 3-State Non-Inverting Buffer/Line Driver/ Line Receiver With LSTTL-Compatible Inputs

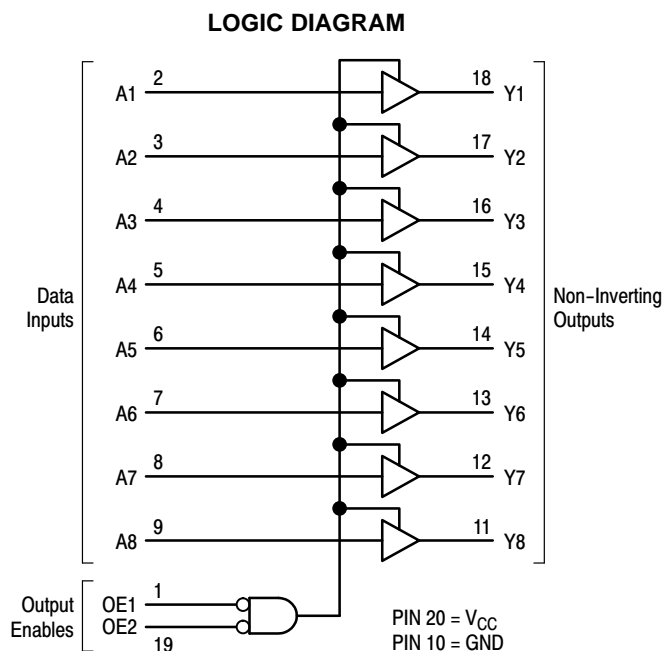
High-Performance Silicon-Gate CMOS

The MC74HCT541A is identical in pinout to the LS541. This device may be used as a level converter for interfacing TTL or NMOS outputs to high speed CMOS inputs.

The HCT541A is an octal non-inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

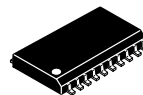
Features

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant



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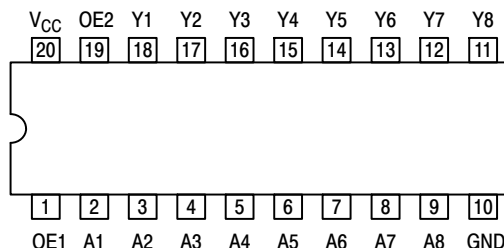


SOIC-20
DW SUFFIX
CASE 751D

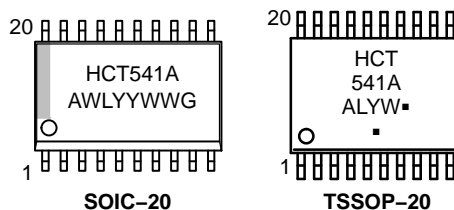


TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance

X = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

MC74HCT541A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air SOIC Package†	500	mW
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	-55	+125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V or V _{CC} − 0.1V I _{out} ≤ 20μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1V or V _{CC} − 0.1V I _{out} ≤ 20μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0mA	4.5	3.98	3.84	3.70	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0mA	4.5	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum 3-State Leakage Current	Output in High Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	5.5	4	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0μA	5.5	≥ −55°C	25 to 125°C		mA
				2.9	2.4		

1. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC74HCT541A

AC CHARACTERISTICS ($V_{CC} = 5.0V$, $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	23	28	32	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum 3–State Output Capacitance (Output in High Impedance State)	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		55	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

SWITCHING WAVEFORMS

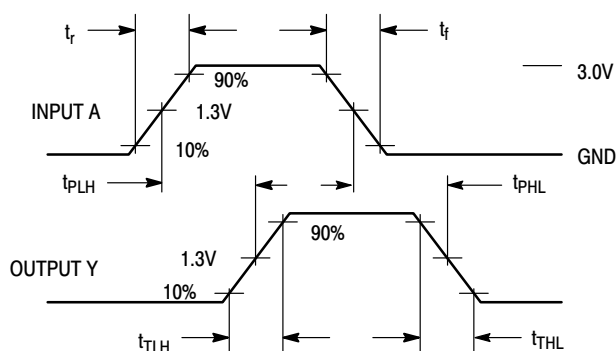


Figure 1.

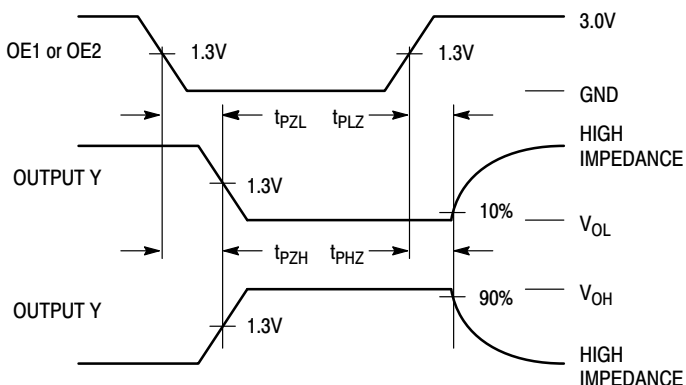
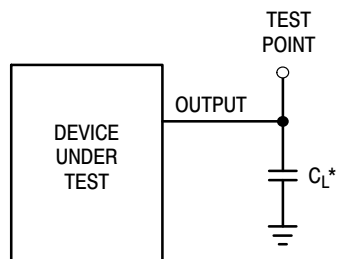


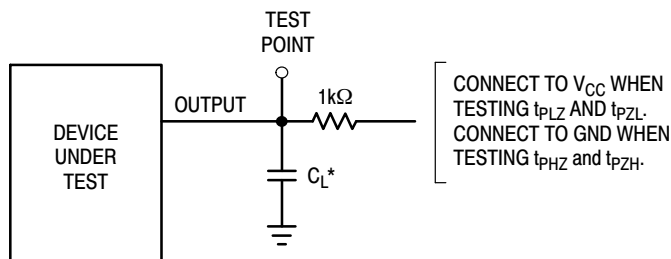
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3.



*Includes all probe and jig capacitance

Figure 4.

MC74HCT541A

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

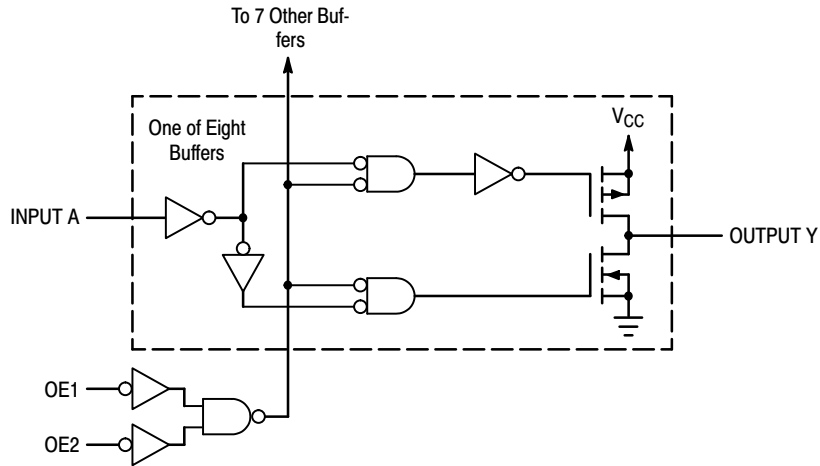
OE1, OE2 (PINS 1, 19) — Output enables (active-low). When a low voltage is applied to both of these pins, the

outputs are enabled and the device functions as a non-inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either non-inverting outputs or high-impedance outputs.

LOGIC DETAIL



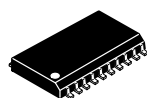
ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HCT541ADWG	SOIC-20 (Pb-Free)	38 Units / Rail
MC74HCT541ADWR2G		1000 / Tape & Reel
NLV74HCT541ADWR2G*		1000 / Tape & Reel
MC74HCT541ADTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
NLV74HCT541ADTR2G*		2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

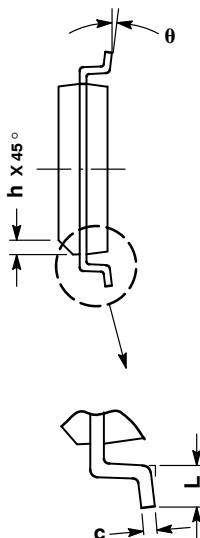
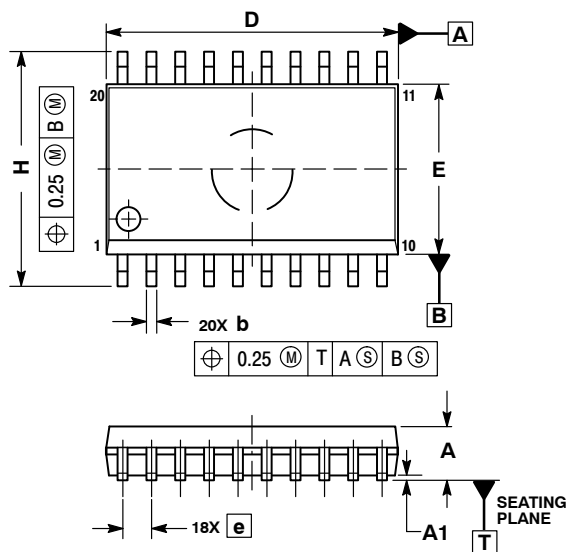
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

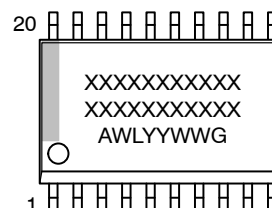


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

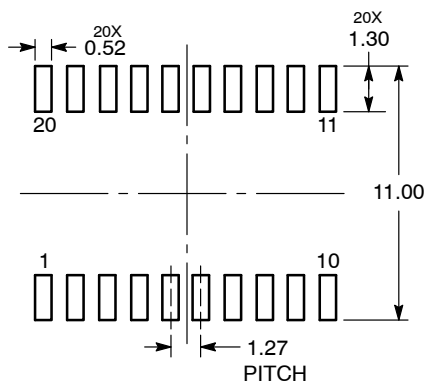
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

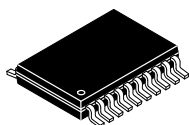
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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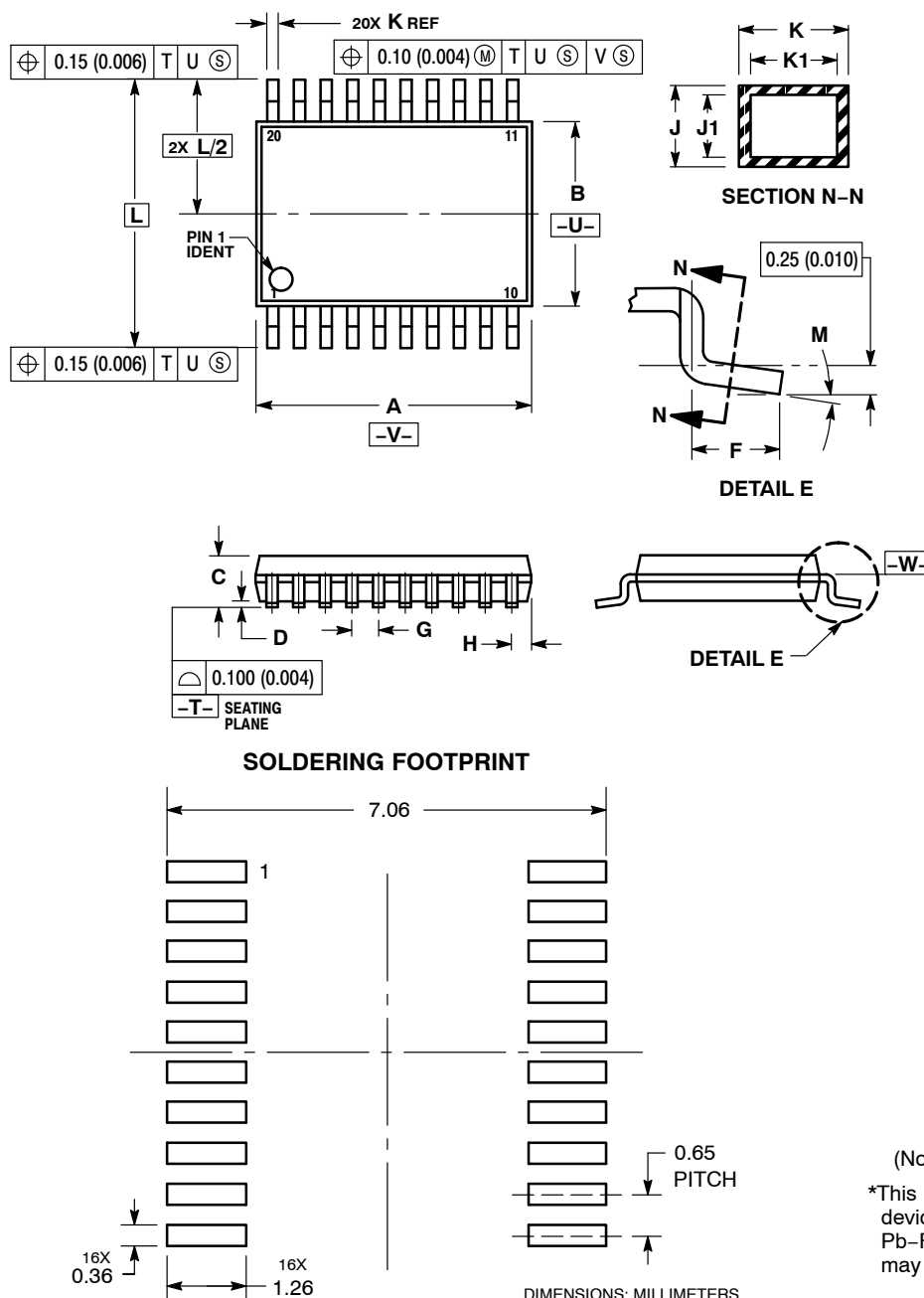
ON



SCALE 2:1

TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

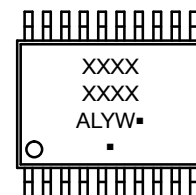


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION: TSSOP-20 WB

PAGE 1 OF 1

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