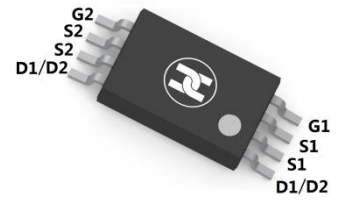
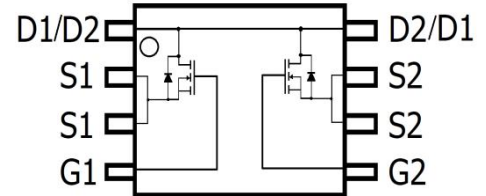


## DUAL N-CANNEL ENHANCEMENT MODE FET

### FEATURES

- Ultra low on-resistance:  $V_{DS}=20V, I_D=5A, R_{DS(ON)} \leq 25m\Omega @ V_{GS}=4.5V$
- Low gate charge
- ESD protected
- Surface Mount device


**TSSOP-8**


### MECHANICAL DATA

- Case: TSSOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: not available

### MAXIMUM RATINGS ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-source voltage	$V_{DS}$	20	V	
Gate-source voltage	$V_{GS}$	$\pm 12$	V	
Continuous drain current $T_A = 25^\circ C$	$I_D$	5	A	
Pulsed drain current(Note 1)	$I_{DM}$	20	A	
Power dissipation	$T_A = 25^\circ C$	$P_D$	2.0	W
	$T_A = 70^\circ C$	$P_D$	1.6	W
Thermal resistance from Junction to ambient (Note 2)	$R_{\theta JA}$	78	$^\circ C/W$	
Thermal resistance from Junction to case(Note 2)	$R_{\theta JC}$	40	$^\circ C/W$	
Junction and Storage temperature	$T_J, T_{STG}$	-55 ~ +150	$^\circ C$	

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ C$ unless otherwise specified)

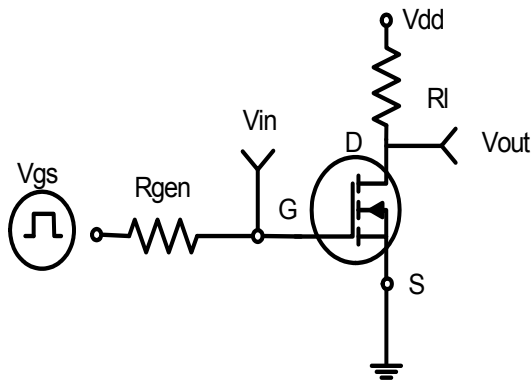
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>Off Characteristics</b>						
Drain-Source breakdown voltage	$V_{(BR)DSS}^*$	20			V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	$I_{DSS}^*$			1	$\mu A$	$V_{DS}=20V, V_{GS}=0V$
				5	$\mu A$	$V_{DS}=20V, V_{GS}=0V, T_J = 55^\circ C$
Gate-body leakage current	$I_{GSS}^*$			$\pm 50$	nA	$V_{DS}=0V, V_{GS}=\pm 8V$
<b>On Characteristics (Note 3)</b>						
Gate-threshold voltage	$V_{GS(th)}^*$	0.5		1.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Drain-source on-resistance	$R_{DS(ON)}^*$		20	25	m $\Omega$	$V_{GS}=4.5V, I_D=5A$
			35	40	m $\Omega$	$V_{GS}=2.5V, I_D=4A$
Forward transconductance	$g_{FS}$		11		S	$V_{DS}=5V, I_D=4.5A$
On-state Drain Current	$I_{D(ON)}$	15			A	$V_{DS}=5V, V_{GS}=4.5V$
<b>Drain-Source Diode Characteristics</b>						
Diode forward voltage	$V_{SD}$		0.75	1.2	V	$I_S=4.5A, V_{GS}=0V$
Diode forward current	$I_S$	5			A	
<b>Dynamic Characteristics (Note4)</b>						
Input capacitance	$C_{iss}$		700		pF	$V_{DS}=10V, V_{GS}=4.5V, f=1MHz$
Output capacitance	$C_{oss}$		175		pF	
Reverse transfer capacitance	$C_{rss}$		85		pF	
<b>Switching Characteristics (Note 4)</b>						
Total gate charge	$Q_g$		7	10	nC	$V_{GS}=4.5V, V_{DS}=10V, I_D=3A$
Gate-source charge	$Q_{gs}$		1.2		nC	
Gate-drain charge	$Q_{gd}$		1.9		nC	
Turn-on delay time	$t_{d(on)}$		8	16	nS	$V_{GS}=4.5V, V_{DS}=10V, I_D=1A, R_{GEN}=6\Omega$
Turn-on rise time	$t_r$		10	18	nS	
Turn-off delay time	$t_{d(off)}$		18	29	nS	
Turn-off fall time	$t_f$		5	10	nS	

### Notes:

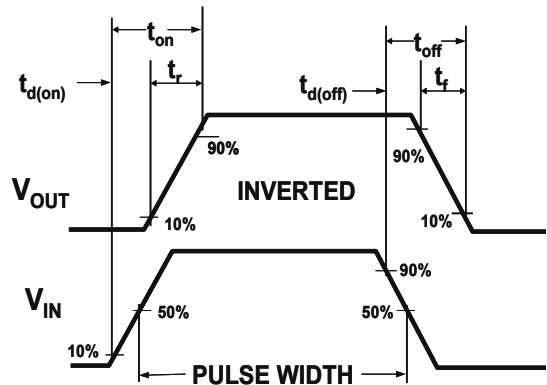
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300 \mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

**DUAL N-CHANNEL ENHANCEMENT MODE FET**

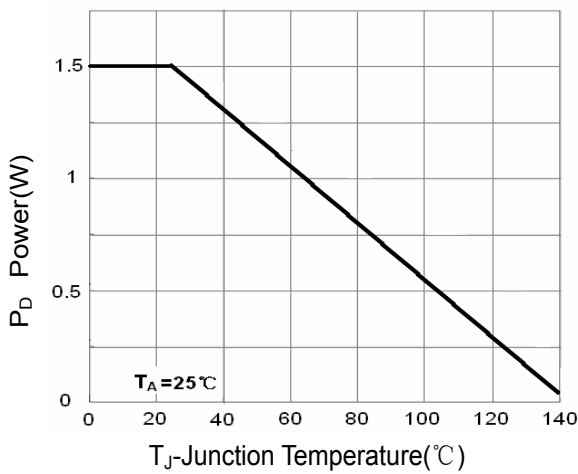
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



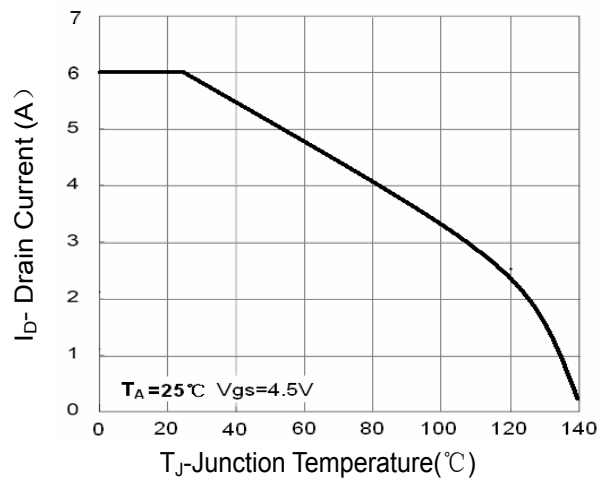
**Figure 1: Switching Test Circuit**



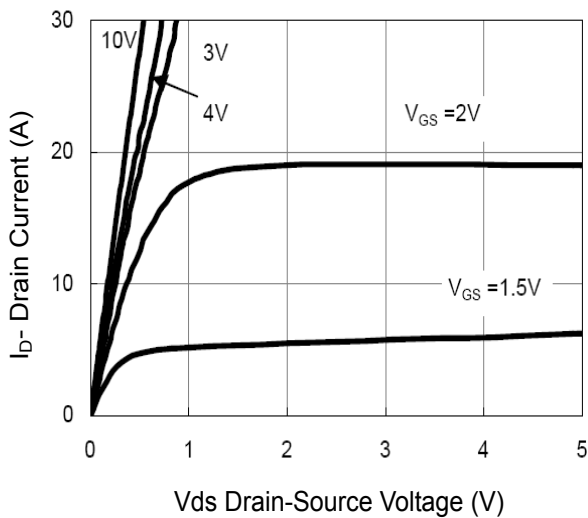
**Figure 2: Switching Waveforms**



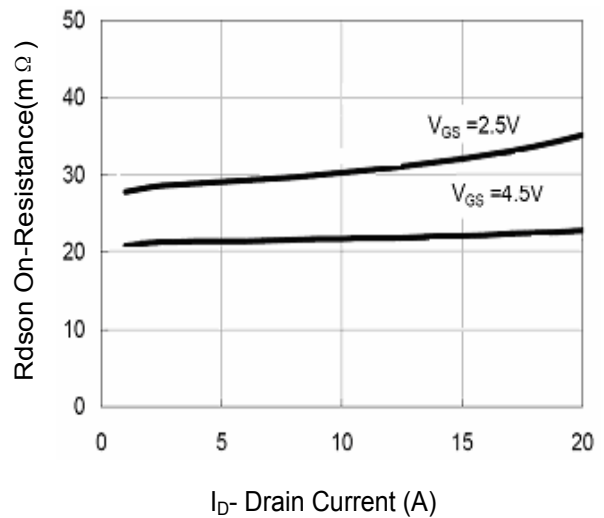
**Figure 3 Power Dissipation**



**Figure 4 Drain Current**

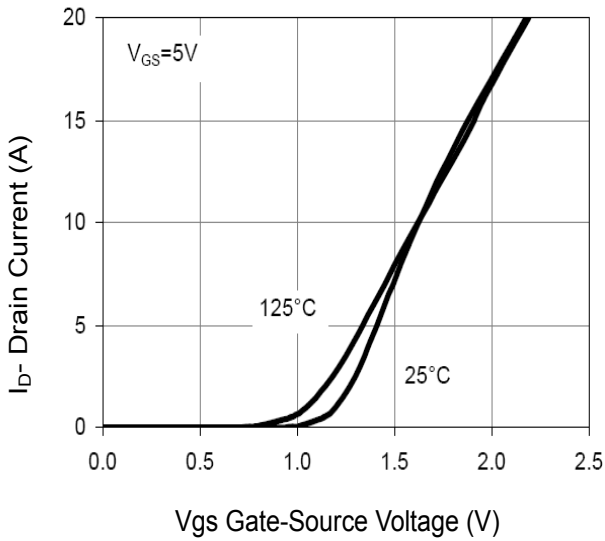


**Figure 5 Output CHARACTERISTICS**

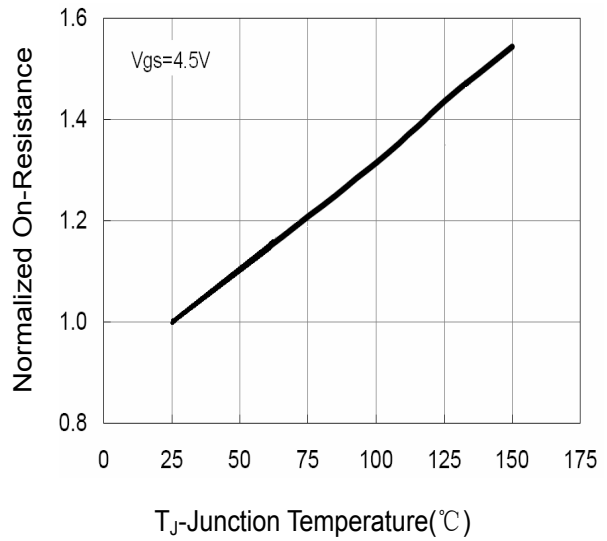


**Figure 6 Drain-Source On-Resistance**

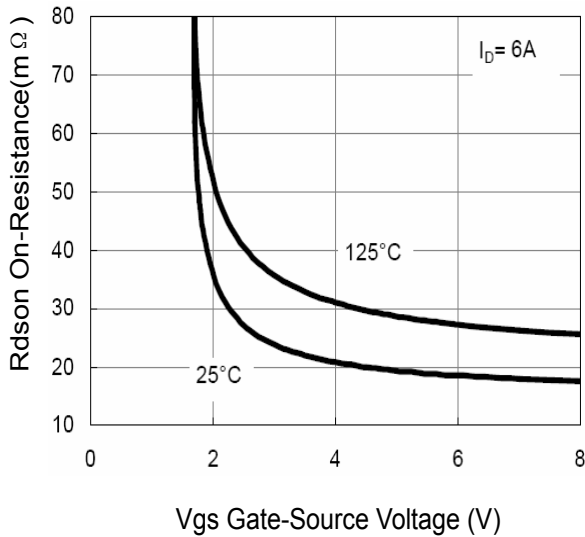
**DUAL N-CHANNEL ENHANCEMENT MODE FET**



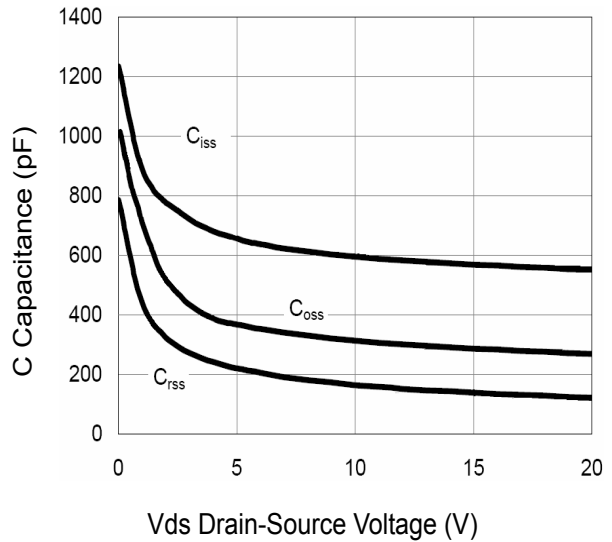
**Figure 7 Transfer Characteristics**



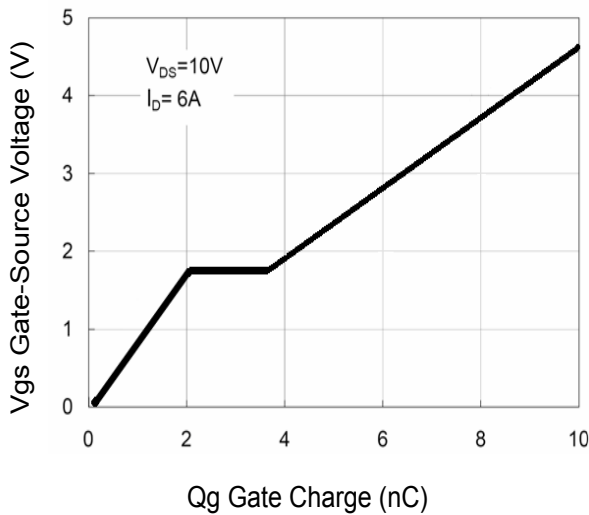
**Figure 8 Drain-Source On-Resistance**



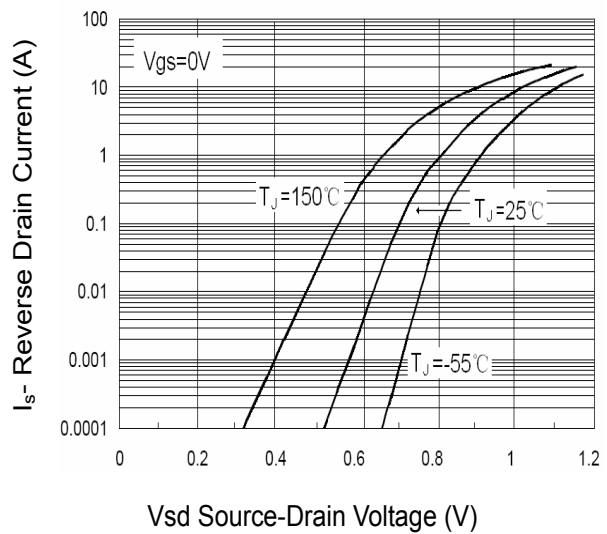
**Figure 9 Rdson vs Vgs**



**Figure 10 Capacitance vs Vds**

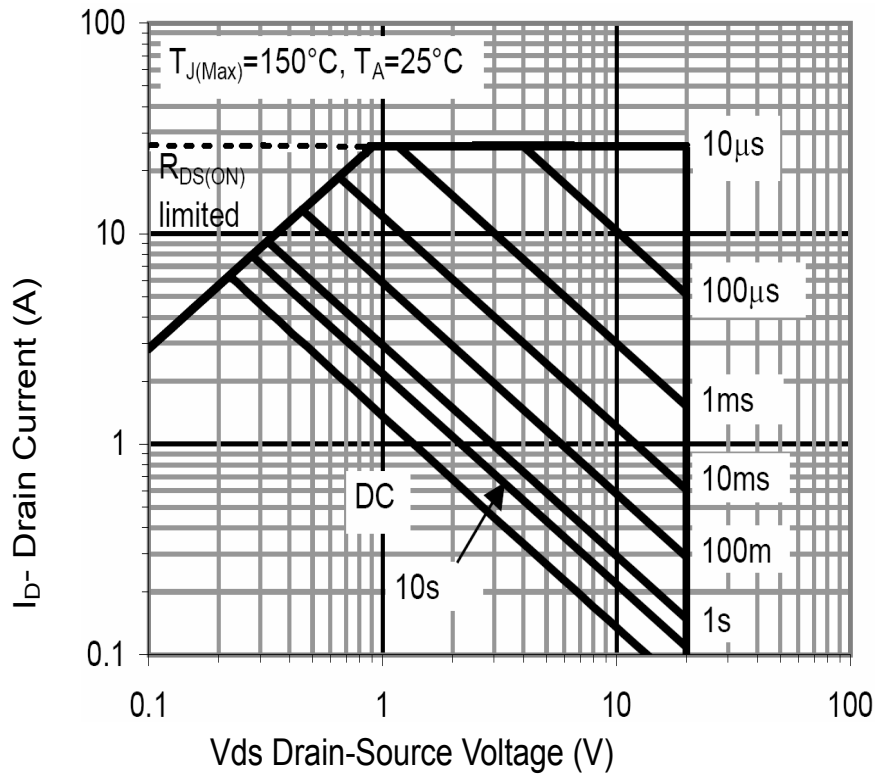


**Figure 11 Gate Charge**

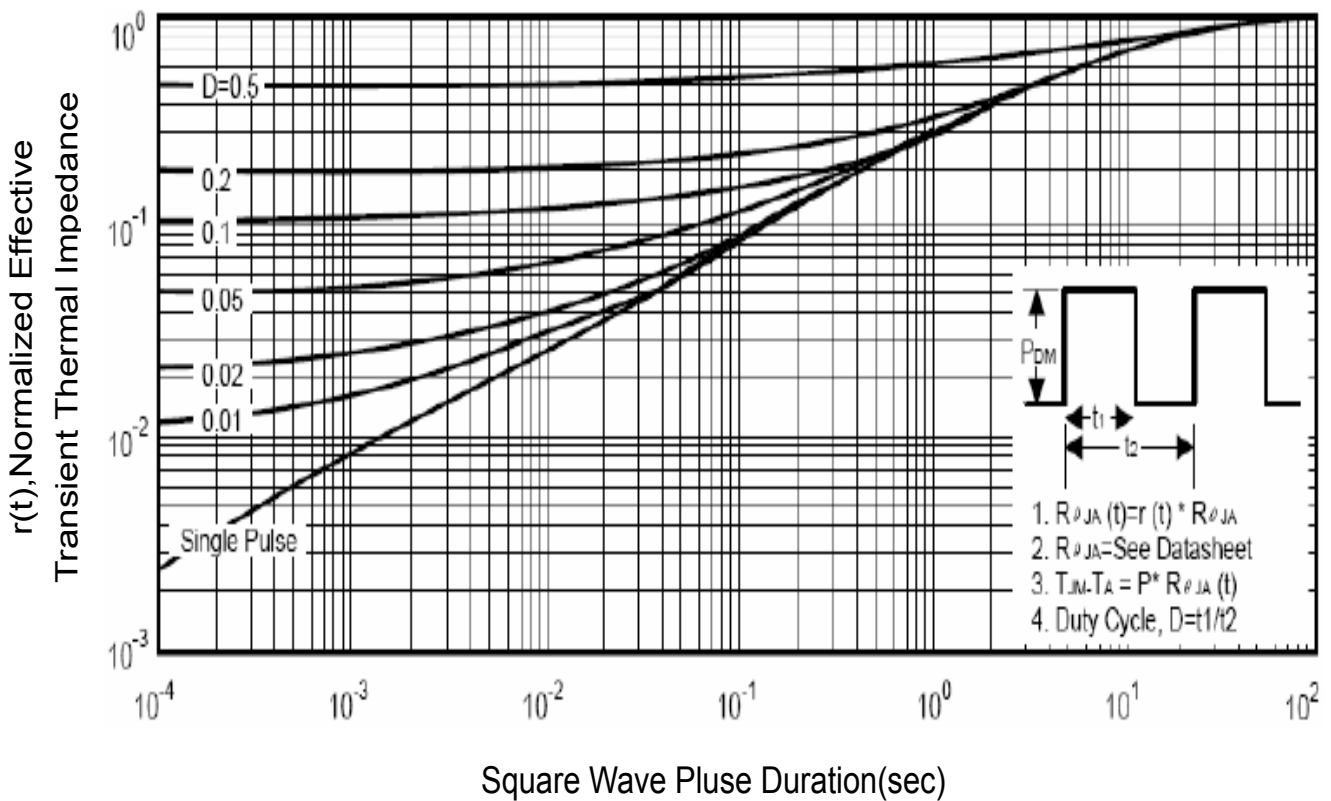


**Figure 12 Source- Drain Diode Forward**

**DUAL N-CHANNEL ENHANCEMENT MODE FET**



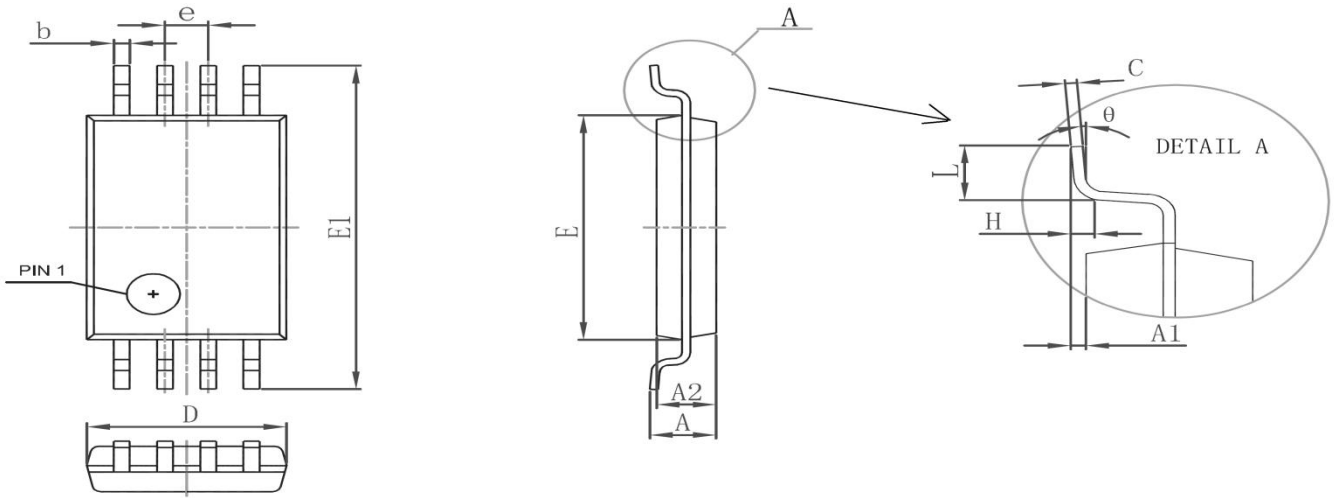
**Figure 13 Safe Operation Area**



**Figure 14 Normalized Maximum Transient Thermal Impedance**

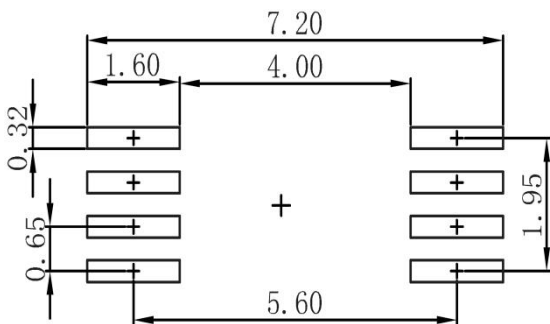
## DUAL N-CHANNEL ENHANCEMENT MODE FET

### TSSOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
$\theta$	1°	7°	1°	7°

### TSSOP-8 Suggested Pad Layout



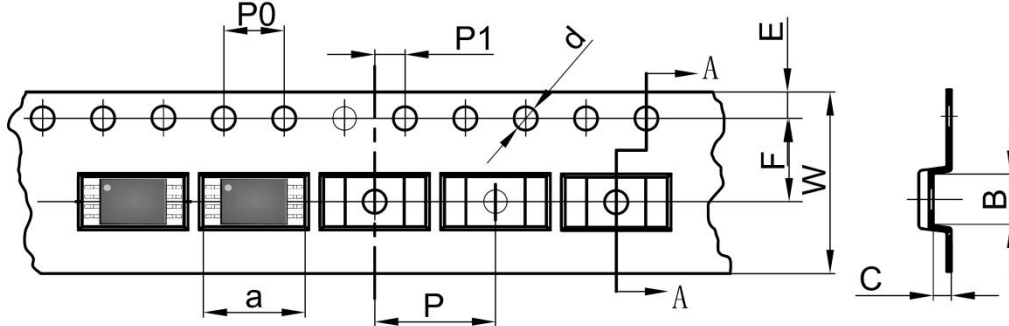
**Note:**

1. Controlling dimension: in millimeters
2. General tolerance:  $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

## DUAL N-CHANNEL ENHANCEMENT MODE FET

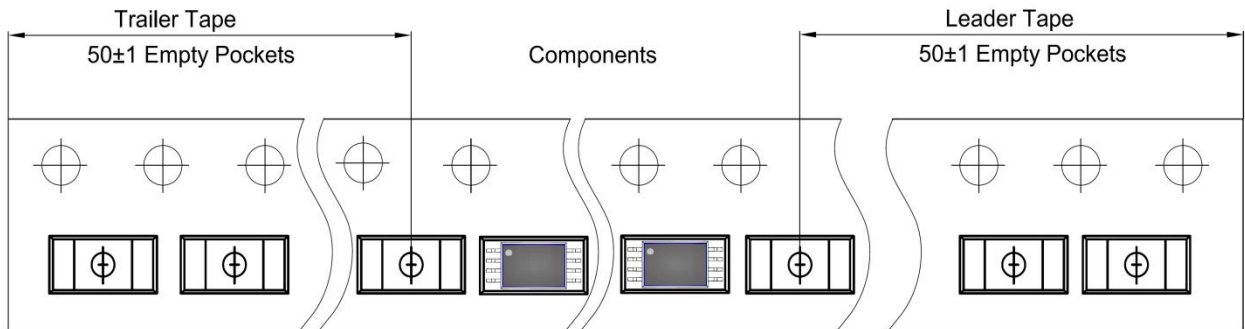
### TSSOP-8 Tape and Reel

#### TSSOP-8 Embossed Carrier Tape

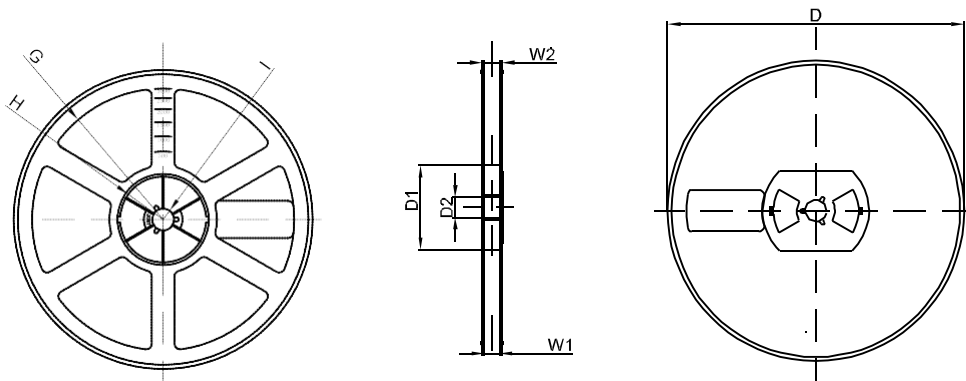


DIMENSIONS ARE IN MILLIMETER										
TYPE	a	B	C	d	E	F	P0	P	P1	W
SOP-8	6.76	3.30	1.20	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

#### TSSOP-8 Tape Leader and Trailer



#### SOP-8 Reel



DIMENSIONS ARE IN MILLIMETER								
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1