UCC5880-Q1 Isolated 20-A Adjustable Gate Drive IGBT/SiC MOSFET Gate Driver With Advanced Protection Features For Automotive Applications

1 Features

- Dual output split driver with on-the-fly programmable drive strength
  – ±15-A and ±5-A drive current outputs
  – Digital input pins (GD*) for drive strength adjustment without SPI
  – 3 resistor settings R1, R2, or R1||R2
  – Integrated 4-A active Miller clamp or optional external drive for Miller clamp transistor
- Primary and secondary side active short circuit (ASC) support
- Internal and external supply under-voltage and over-voltage protection
- Driver die temperature sensing and over temperature protection
- Short-circuit protection:
  – 75-ns response time to over-current event
  – DESAT protection – selections up to 14 V
  – Shunt resistor based over-current protection
  – Configurable protection threshold values and blanking times
  – Programmable soft turnoff (STO) and two-level soft turnoff (2STO) current
- Integrated 10-bit ADC
  – Power switch temperature, driver die temperature, DESAT pin voltage, VCC2 voltage, phase current, DC Link voltage
  – Programmable digital comparators
- Advanced VCE/VDS clamping circuit
- Functional Safety-Compliant
  – Developed for functional safety applications
  – Documentation available to aid ISO 26262 system design up to ASIL D
- Integrated diagnostics:
  – Built in self-test (BIST) for protection comparators
  – Gate threshold voltage measurement for power device health monitoring
  – INP to transistor gate path integrity
  – Internal clock monitoring
  – Fault alarm and warning outputs (nFLT*)
  – ISO communication data integrity check
- SPI based device reconfiguration, verification, supervision, and diagnosis
- 100 kV/µs CMTI
- Safety-related certifications:
  – 5-kV_{RMS} isolation for 1 minute per UL1577 (planned)
  – Reinforced isolation 7070-V_{PK} per DIN VDE 0884-11: 2017-01 (planned)
- AEC-Q100 qualified with the following results:
- – Device temperature grade 1: -40°C to +125°C ambient operating temperature
  – Device HBM ESD classification level 2
  – Device CDM ESD classification level C4B

2 Applications

- EV and HEV traction inverter
- EV and HEV power modules

3 Description

The UCC5880-Q1 device is an isolated, highly configurable adjustable slew-rate gate driver targeted to drive high power SiC MOSFETs and IGBTs in EV/HEV applications. Power transistor protections such as shunt resistor based over-current, over-temperature (PTC, NTC, or diode), and DESAT detection, including selectable soft turn-off or two-level soft turn-off during these faults. To further reduce the application size, the UCC5880-Q1 integrates an active Miller clamp, and an active gate pull-down while the driver is unpowered. An integrated 10-bit ADC enables monitoring of up to 2 analog inputs, VCC2, DESAT, and the gate driver temperature for enhanced system management. Diagnostics and detection functions are integrated to simplify the design of ASIL compliant systems. The parameters and thresholds for these features are configurable using the SPI, which allows the device to be used with nearly any SiC MOSFET or IGBT.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
UCC5880DFC-Q1	SSOP (32)	10.5mm x 7.5mm

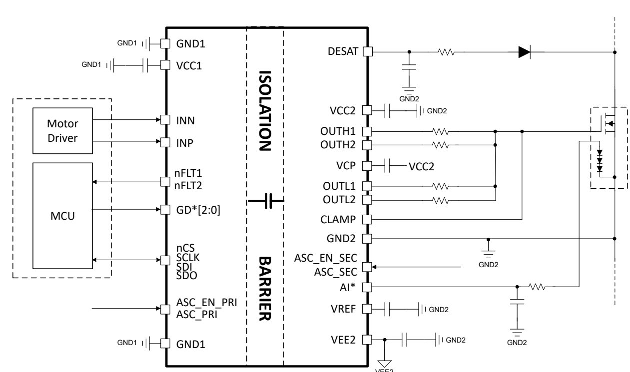

Figure 3-1. Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Advance Information Release

5 Pin Configuration and Functions

32-pin SSOP Top View

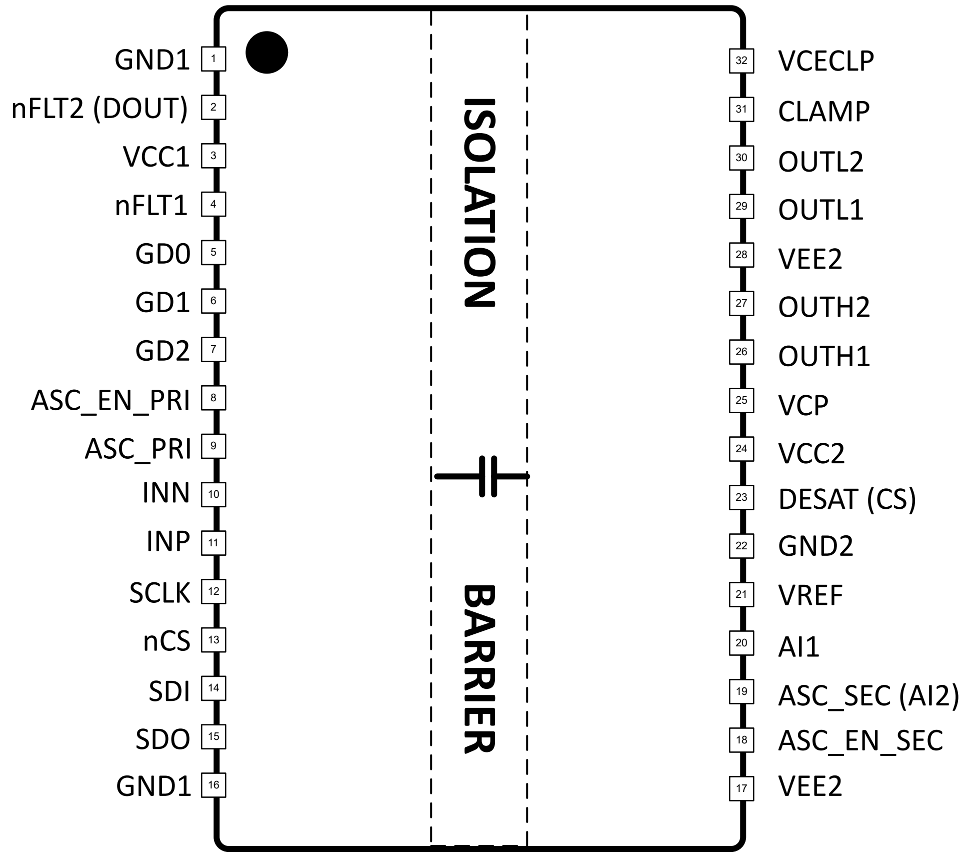

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Table 5-1. Pin Functions

PIN NAME	PIN NO.	I/O(1)	DESCRIPTION
GND1	1, 16	P	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side. Prioritize pin 1 for supply and input filter decoupling.
nFLT2 (DOUT)	2	O	Fault Indicator Output 2. nFLT2 is used to interrupt the host when a fault occurs. Additionally, nFLT2 may be configured as DOUT to provide the host controller a PWM signal with a duty cycle relative to the ADC input of interest. Faults that are unmasked pull nFLT2 low when the fault occurs. nFLT2 is high when all faults are either non-existent or masked.
VCC1	3	P	Primary Side Power Supply. Connect a 3V to 5.5V power supply to VCC1. Bypass VCC1 to GND1 with ceramic bulk capacitance as close to the VCC1 pin as possible.
nFLT1	4	O	Fault Indicator Output 1. nFLT1 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT1 low when the fault occurs. nFLT1 is high when all faults are either non-existent or masked.
GD0	5	I	OUTL1/2 and OUTH1/2 Selector Inputs. GD* select combinations of OUT*1 and OUT*2 with user-selectable resistors. Drive all GD* high to force the gate of the power transistor low and reset all faults. See Adjustable Gate Drive Outputs (OUTL* OUTH*) for more details. Tie to GND1 if not used.
GD1	6	I	
GD2	7	I	
ASC_EN_PRI	8	I	Primary-side Active Short Circuit Enable Input. ASC_EN_PRI enables the ASC function and forces the output to follow the ASC_PRI pin input state. If ASC_EN_PRI is high, the OUTx pins follow the ASC_PRI pin state. When ASC_EN_PRI is low, the OUT* pins follow the INP and INN pin logical truth table. Tie to GND1 if not used.
ASC_PRI	9	I	Primary-side Active Short Circuit Polarity Input. The OUT* pins follow the logic level at ASC_PRI when the ASC_EN_PRI input is driven high. See the ASC section for more details. Tie to GND1 if not used.
INN	10	I	Negative PWM Input. INN is connected to the INP from the opposite arm of the half-bridge. If INP and INN overlap, the Shoot Through Protection (STP) engages and forces output low. Tie to GND1 if not used.
INP	11	I	Positive PWM Input. INP drives the state of the driver output. With the driver enabled, when INP is high, OUTH* is pulled high. When INP is low, OUTL* is pulled low. Drive INP up to a 50kHz PWM signal, with a logic level determined by the VCC1 voltage. INP is connected to the INN of the opposite arm of the half-bridge. If INP and INN overlap, STP engages and forces output low.
SCLK	12	I	SPI Clock. SCLK is the clock signal for the main SPI interface. The SPI interface operates with clock rates up to 4MHz.
nCS	13	I	SPI Chip Selection Input. nCS is an active low input used to activate the SPI peripheral device. Drive nCS low during SPI communication. When nCS is high, the CLK and SDI inputs are ignored. Tie to VCC1 if not used.
SDI	14	I	SPI Data Input. SDI is the data input for the main SPI interface. Data is sampled on the falling edge of CLK, SDI must be in a stable condition to ensure proper communication.
SDO	15	O	SPI Data Output. SDO is the data output for the main SPI interface. Data is clocked out on the falling edge of CLK, SDO is changed with a rising edge of CLK.
VEE2	17, 28	P	Secondary Negative Power Supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of ceramic capacitance as close to pin 28 as possible.
ASC_EN_SEC	18	I	Secondary-side Active Short Circuit Enable Input. ASC_EN_SEC enables the ASC function and forces the output of the driver to the low safe state. If ASC_EN_SEC is high, OUTL* is pulled low. When ASC_EN_SEC is low, the output is controlled by primary side pins. Tie to GND2 if not used.
ASC_SEC	19	I	Analog Input 2/ Secondary-side Active Short Circuit Polarity Input. ASC_SEC (AI2) defaults to Active Short Circuit Polarity Input. When programmed as ASC_SEC, the OUTx pins follow the logic level at ASC_SEC when the ASC_EN_SEC input is driven high. See the ASC section for more details. Tie to GND2 if not used.
AI2		I	Analog Input 2/ Secondary-side Active Short Circuit Polarity Input. ASC_SEC (AI2) can be programmed as an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable "digital comparator" is available to signal faults when the voltage is above/below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.

Table 5-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
AI1	20	I	Analog Input 1. AI1 is an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable “digital comparator” is available to signal faults when the voltage is above/ below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.
VREF	21	P	Internal ADC Voltage Regulator Output. VREF provides an internal 5V, reference for the ADC. Bypass VREF to GND2 with at least 1uF of ceramic capacitance. Loads up to 5mA on VREF are allowed.
GND2	22	P	Gate Drive Supply Reference. Connect GND2 to the power FET source/ IGBT emitter. ASC_EN_SEC, ASC_SEC (AI2), AI1, VREF, and DESAT are referenced to GND2.
DESAT	23	I	Current Sense Input/ Desaturation based Short Circuit Detection Input. DESAT (CS) is configurable to sense over-current conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For DESAT applications, bypass DESAT to GND2 with a ceramic capacitor and, in parallel, connect a Schottky diode with the cathode connected to the DESAT, anode connected to GND2. See the applications section for details on calculating the component values. Additionally, connect DESAT to a resistor to the anode of a diode to the collector of the power FET. DESAT detects a fault when the VDS/VCE voltage of the power FET exceeds the SPI programmable threshold while the power FET is on. Tie to GND2 if not used.
CS		I	Current Sense Positive Input/ Desaturation based Short Circuit Detection Input. CS (DESAT) is configurable to sense over-current and short-circuit conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For sense resistor based applications, connect DESAT (CS) pin to the positive side of the sense element through an RC. The current limit threshold is programmable via SPI. Tie to GND2 if not used.
VCC2	24	P	Secondary Positive Power Supply. Connect a 15V to 30V power supply to VCC2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VCC2 to GND2 and VCC2 to VEE2 with bulk ceramic capacitance as close to the VCC2 pin as possible. Additional capacitance may be needed depending on the required drive current.
VCP	25	P	High-side Drive Supply. VCP supplies power for the OUTH* drive. Bypass VCP to VCC2 with a ceramic capacitor between 10nF and 100nF, as close to the VCP pin as possible.
OUTH1	26	O	Gate driver source pins (OUTH1 = $15A_{PK}$, OUTH2 = $5A_{PK}$). When the driver is active and commanded high, OUTH* pins are used to source current to the gate of the power FET to drive the output high. Connect OUTH* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTH1 and OUTH2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTH1 only, OUTH2 only, and OUTH1 + OUTH2).
OUTH2	27	O	
OUTL1	29	O	Gate driver sink pins (OUTL1 = $15A_{PK}$, OUTL2 = $5A_{PK}$). When the driver is active and commanded low, OUTL* pins are used to sink current from the gate of the power FET to drive the gate low. Connect OUTL* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTL1 and OUTL2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTL1 only, OUTL2 only, and OUTL1 + OUTL2).
OUTL2	30	O	
CLAMP	31	O	Miller Clamp pin. The CLAMP pin is used to hold the gate of the power FET strongly to VEE2 while the power FET is "off". CLAMP is configurable as an internal Miller clamp, or to drive an external clamping circuit. When using the internal clamping function, connect CLAMP directly the power FET gate. When configured as an external clamp, connect CLAMP to the gate of an external pulldown MOSFET. Disable and tie to VEE2 if not used.
VCECLP	32	I	VCE Clamp Input. VCECLP clamps to a diode above the VCC2 rail and indicates a fault when the voltage at VCECLP is above the VCECLPth voltage. Bypass VCECLP to VEE2 with ceramic capacitor and, in parallel, connect a resistor. See the applications section for details on calculating the component values. Additionally, connect VCECLP to the anode of a zener diode to the collector/drain of the power FET. Tie to VEE2 if not used.

ADVANCE INFORMATION

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Documentation Support

6.1.1 Related Documentation

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

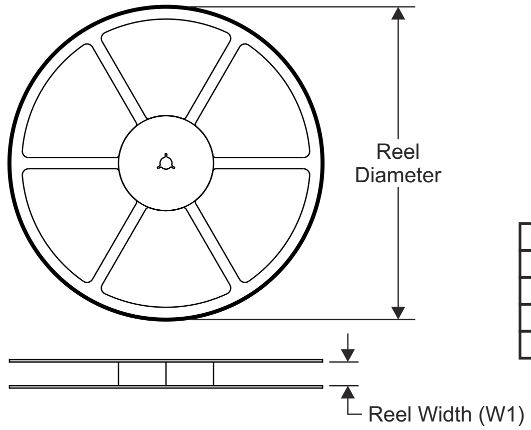
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

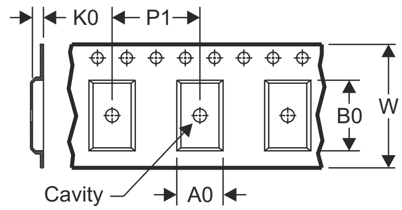
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information

REEL DIMENSIONS

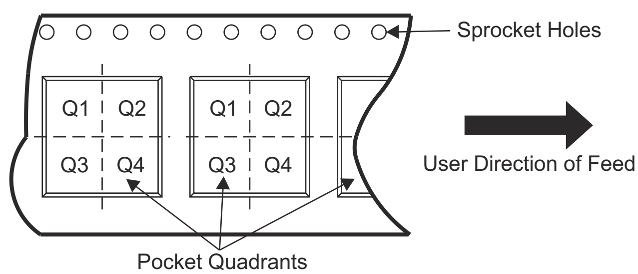


TAPE DIMENSIONS



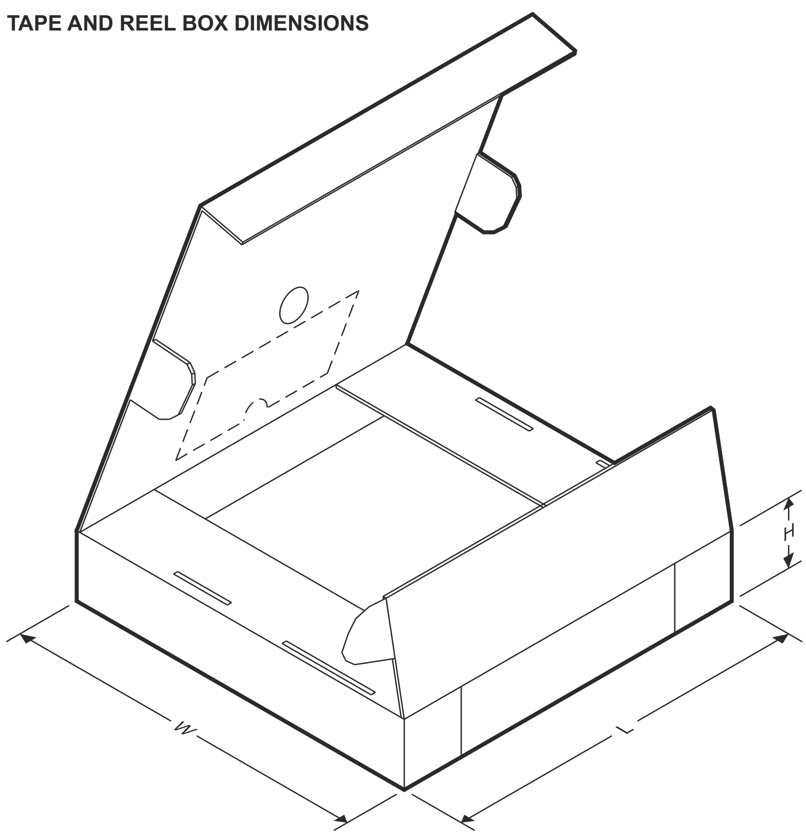
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)

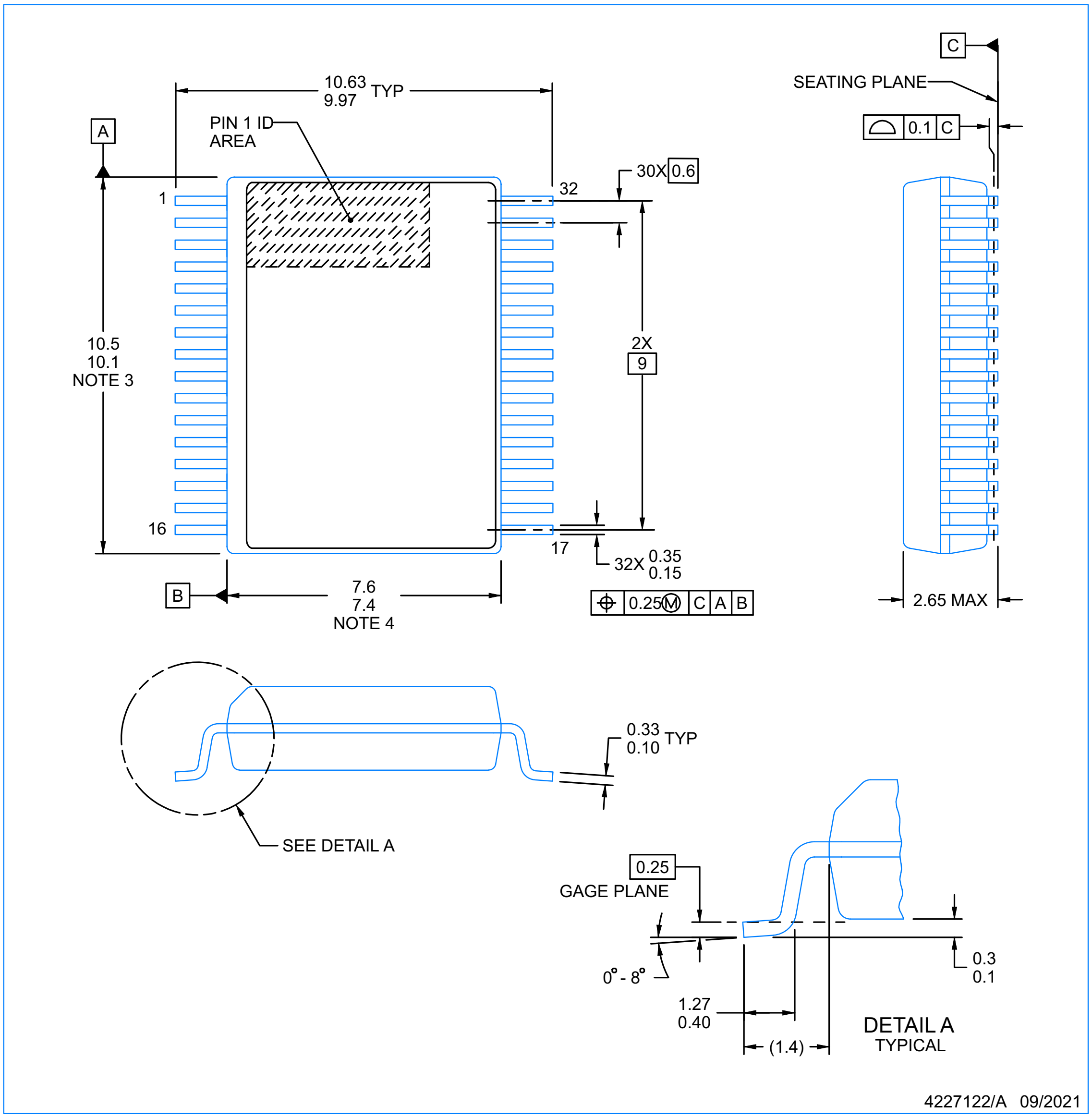
ADVANCE INFORMATION

PACKAGE OUTLINE

DFC0032A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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EXAMPLE BOARD LAYOUT

DFC0032A

SSOP - 2.65 mm max height

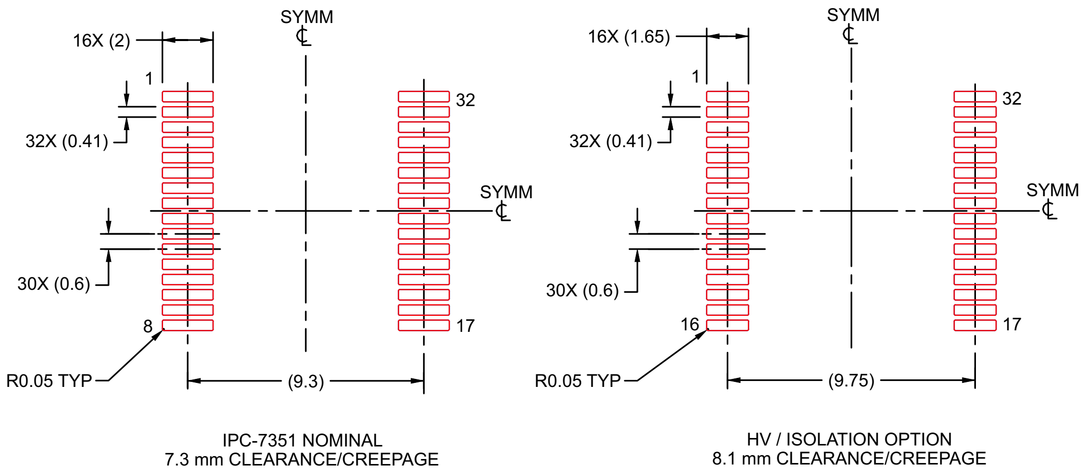
SMALL OUTLINE PACKAGE

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DFC0032A SSOP - 2.65 mm max height

SAMLL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4227122/A 09/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC5880QDFCQ1	ACTIVE	SSOP	DFC	32	40	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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