

### Innovating Energy Technology

# FML60N104S2FDHF

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**FUJI POWER MOSFET** 

# Super J MOS® S2 series

#### N-Channel enhancement mode power MOSFET

#### Features

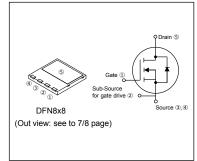
Pb-free lead terminal RoHS compliant Halogen-free molding compound MSL:1, Reflow available

#### Applications

For switching



#### Package and Internal circuit chart



#### ■ Absolute Maximum Ratings at T<sub>c</sub>=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Ducin Source Voltage	V <sub>DS</sub>	600	V	
Drain-Source Voltage	V <sub>DSX</sub>	600	V	V <sub>GS</sub> =-30V
Continuous Drain Current	,	41.3	Α	T <sub>c</sub> =25°C Note*1,2
Continuous Drain Current	<b>/</b> D	26.1	Α	T <sub>c</sub> =100°C Note*1,2
Pulsed Drain Current	<b>I</b> <sub>DP</sub>	120.4	Α	Note *2
Gate-Source Voltage	<b>V</b> <sub>GS</sub>	±30	V	
Non-Repetitive Maximum Avalanche Current	<b>I</b> AS	4.9	А	Note *3
Non-Repetitive Maximum Avalanche Energy	<b>E</b> AS	809.3	mJ	Note *4
Maximum MOSFET dv/dt	d <i>v</i> ⊳s/d <i>t</i>	50	V/ns	V <sub>DS</sub> ≤ 600V
Continuous	,	41.3	Α	T <sub>c</sub> =25°C Note*1,2
Diode Forward Current	<b>I</b> DR	26.1	Α	T <sub>c</sub> =100°C Note*1,2
Pulsed Diode Forward Current	I <sub>DRP</sub>	120.4	Α	Note *2
Peak Diode Recovery dv/dt	dv/dt	30	V/ns	Note *5
Peak Diode Recovery -didr/dt	-d <i>i</i> <sub>DR</sub> /d <i>t</i>	100	A/µs	Note *6
Maximum Dawar Dissination	P <sub>tot</sub>	232	W	<i>T</i> c=25°C
Maximum Power Dissipation	Ptot	2.78	W	<i>T</i> <sub>a</sub> =25°C
Operating Channel Temperature	T <sub>ch</sub>	150	°C	
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C	

Note \*1 : Maximum duty cycle D=0.53

Note 1. Maximum duty cycle D=0.30Note \*2: Limited by maximum channel temperature. Note \*3:  $T_{ch} \le 150$  °C, See Figure 1 and 2. Note \*4: Starting  $T_{ch} = 25$  °C,  $I_{AS} = 3$  A, L = 165 mH,  $V_{DD} = 60$  V,  $R_{G} = 50$   $\Omega$ , See Figure 1 and 2. Eas limited by maximum channel temperature and avalanche current.

EAS Illillied by Histarillian Grainfel Ching-Cartains and Sciences 2. Note \*5: Jor ≤32.8 A , -dios/dt ≤ 100 A/ys, Vbs peak ≤ 600 V, 7ch ≤ 150 °C. Note \*6: Jor ≤32.8 A , dv/dt ≤ 30 V/ns, Vbs peak ≤ 600 V, 7ch ≤ 150 °C.

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# ■ Electrical Characteristics at *T*<sub>c</sub>=25°C (unless otherwise specified) • Static characteristics

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V I <sub>D</sub> = 250 μA		600	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ $I_D = 4.9 \text{ mA}$		3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	Ibss	V <sub>DS</sub> = 600 V V <sub>GS</sub> = 0 V	T <sub>ch</sub> = 25 °C	-	-	25	μΑ
		V <sub>DS</sub> = 480 V V <sub>GS</sub> = 0 V	T <sub>ch</sub> = 125 °C	-	-	250	
Gate-Source Leakage Current	<b>I</b> GSS	V <sub>DS</sub> = 0 V V <sub>GS</sub> = ± 30 V		-	10	100	nA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V I <sub>D</sub> = 8.2 A		-	0.093	0.104	Ω
Gate resistance	r <sub>g</sub>	f = 1 MHz, open drain		-	7.5	-	Ω

#### • Dynamic characteristics

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Forward Transconductance	<b>g</b> fs	V <sub>DS</sub> = 25 V I <sub>D</sub> = 16.4 A	6	24	-	S
Input Capacitance	Ciss	V <sub>DS</sub> = 400 V	-	1720	-	
Output Capacitance	Coss	V <sub>GS</sub> = 0 V	-	60	-	
Reverse Transfer Capacitance	Crss	f = 250 kHz	-	7.9	-	
Effective output capacitance, energy related (Note *7)	C <sub>o(er)</sub>	V <sub>DS</sub> = 0400 V V <sub>GS</sub> = 0 V	-	139	-	pF
Effective output capacitance, time related (Note *8)	C <sub>o(tr)</sub>	V <sub>DS</sub> = 0400 V V <sub>GS</sub> = 0 V I <sub>D</sub> = constant	-	569	-	
Turn-On Time	t <sub>d(on)</sub>	$V_{\rm DD}$ = 400 V, $V_{\rm GS}$ = 10 V $I_{\rm D}$ = 16.4 A, $R_{\rm G}$ = 20 $\Omega$ See Figure 3 and 4	-	36	-	ns
	<b>t</b> r		-	33	-	
Turn-Off Time	t <sub>d(off)</sub>		-	207	-	
	<b>t</b> f		-	21	-	
Total Gate Charge	<b>Q</b> <sub>G</sub>	$V_{DD} = 400 \text{ V}, V_{GS} = 10 \text{ V}$	-	83	-	
Gate-Source Charge	Q <sub>GS</sub>	I <sub>D</sub> = 32.8 A	-	27	-	nC
Gate-Drain Charge	<b>Q</b> <sub>GD</sub>	See Figure 5	-	47	-	

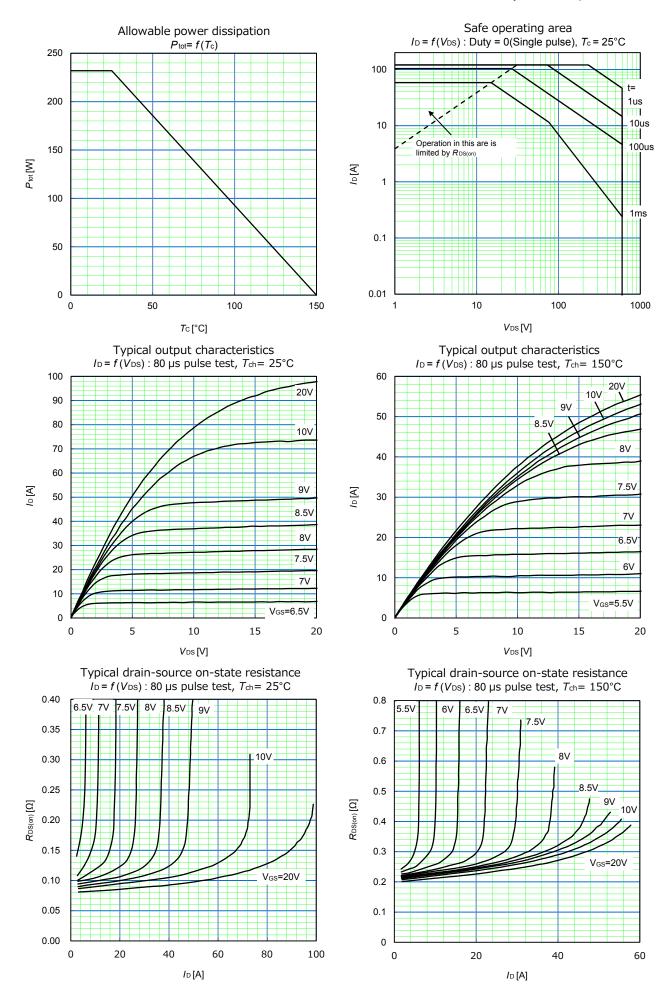
Note  $^*7$ :  $C_{0(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while Vos is rising from 0 to 400V. Note  $^*8$ :  $C_{o(er)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while Vos is rising from 0 to 400V.

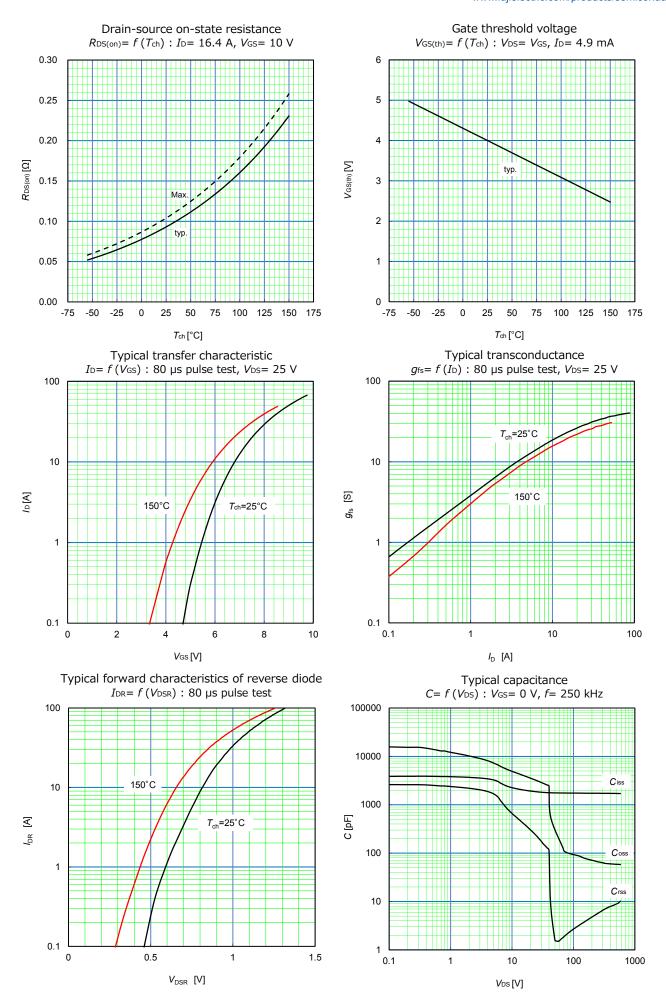
#### • Reverse diode characteristics

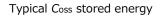
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Diode Forward On-Voltage	<b>V</b> <sub>DSR</sub>	I <sub>DR</sub> = 32.8 A, V <sub>GS</sub> = 0 V T <sub>ch</sub> = 25 °C	-	1.00	1.35	V
Reverse Recovery Time	<b>t</b> rr	V <sub>DD</sub> = 400 V I <sub>DR</sub> = 32.8 A	-	185	-	ns
Reverse Recovery Charge	Qrr	$V_{GS} = 0 \text{ V} \\ -di_{DR}/dt = 100 \text{ A/}\mu\text{s}$	-	1.6	-	μC
Peak Reverse Recovery Current	<b>I</b> rrm	T <sub>ch</sub> = 25 °C See Figure 6 and 7	-	15.8	-	Α

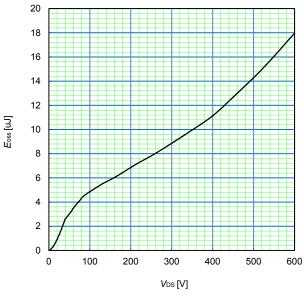
#### ■ Thermal Resistance

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Thermal Resistance, Channel – Ambient	Rth(ch-a)	Device mounted on PCB (FR4) Size: 40mm*40mm*1.5mm with 6cm² copper area (one layer, 70µm thickness) for drain connection and cooling.	-	-	45	°C/W
Thermal Resistance, Channel – Case	R <sub>th(ch-c)</sub>		-	-	0.539	°C/W

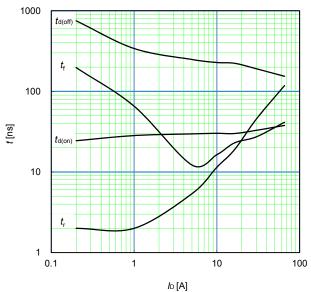




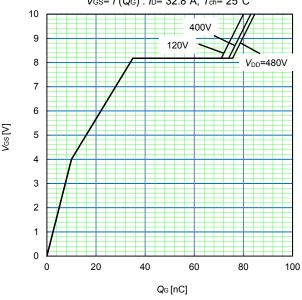




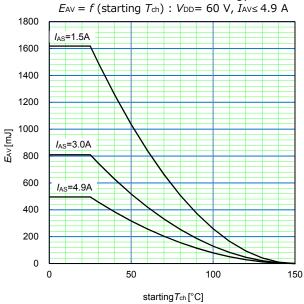
# Typical switching times vs. $I_D$ t= $f(I_D)$ : $V_{DD}$ = 400 V, $V_{GS}$ = 10 V/0 V, $R_G$ = 20 $\Omega$ , $T_{Ch}$ = 25°C



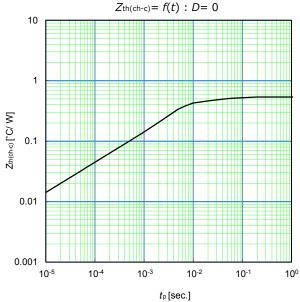
# Typical gate charge $V_{GS} = f(Q_G)$ : $I_{D} = 32.8$ A, $T_{Ch} = 25$ °C



#### Maximum Avalanche Energy



### Transient Thermal Impedance



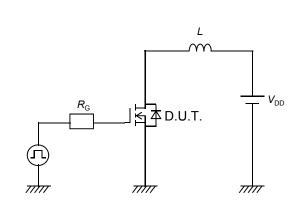


Figure 1. Unclamped inductive load test circuit

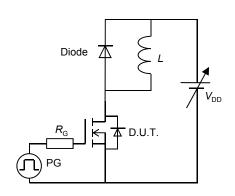


Figure 3. Switching test circuit

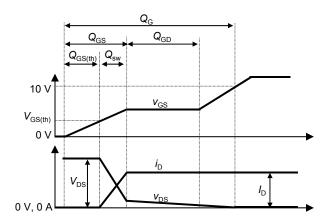


Figure 5. Gate charge waveform

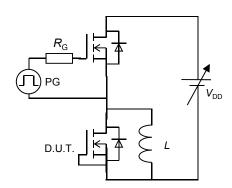


Figure 6. Diode reverse recovery test circuit

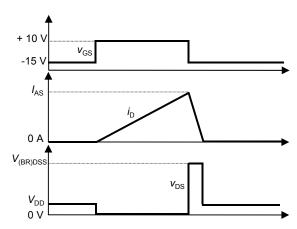


Figure 2. Unclamped inductive waveform

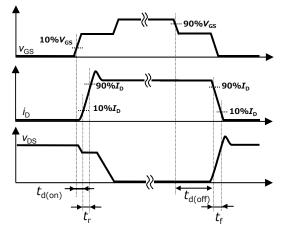


Figure 4. Switching times waveform

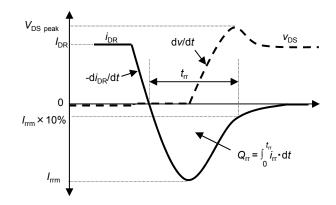
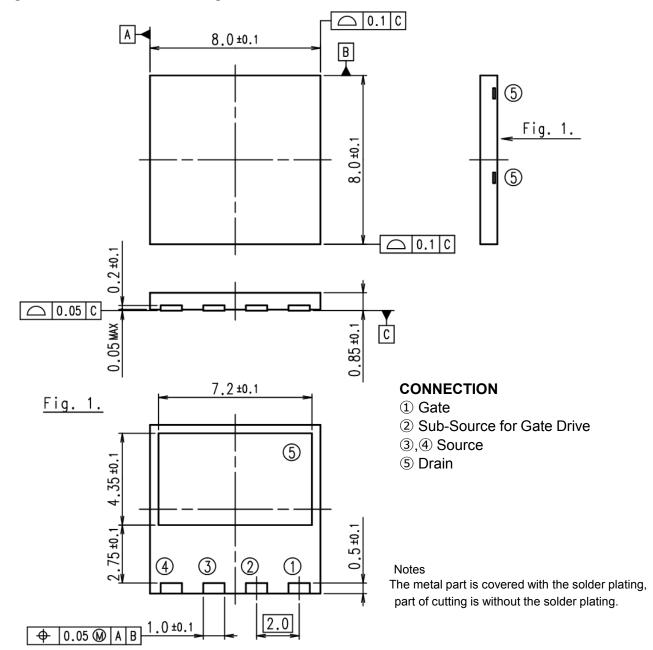
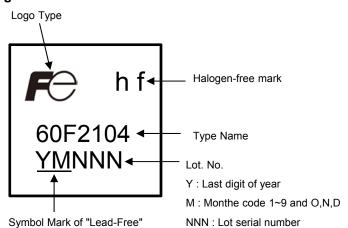


Figure 7. Diode reverse recovery waveform

#### ■ Package Dimensions : DFN8x8 Package

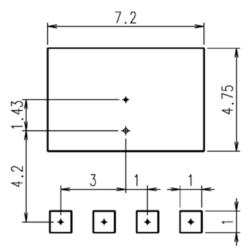


#### Marking



<sup>\*</sup> The font (font type,size) and the trademark-size might be actually different.

#### ■ Recommended footprint



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