

FML60N093S2FDHF

Super J MOS[®] S2 series

N-Channel enhancement mode power MOSFET

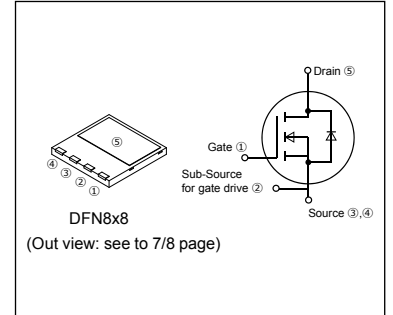
Features

- Pb-free lead terminal
- RoHS compliant
- Halogen-free molding compound
- MSL:1, Reflow available

Applications

- For switching

Package and Internal circuit chart



Absolute Maximum Ratings at $T_c=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	$V_{GS}=-30V$
Continuous Drain Current	I_D	42.3	A	$T_c=25^\circ\text{C}$ Note*1,2
		26.8	A	$T_c=100^\circ\text{C}$ Note*1,2
Pulsed Drain Current	I_{DP}	125.6	A	Note *2
Gate-Source Voltage	V_{GS}	± 30	V	
Non-Repetitive Maximum Avalanche Current	I_{AS}	5.5	A	Note *3
Non-Repetitive Maximum Avalanche Energy	E_{AS}	964.2	mJ	Note *4
Maximum MOSFET dv/dt	dv_{DS}/dt	50	V/ns	$V_{GS} \leq 600V$
Continuous Diode Forward Current	I_{DR}	42.3	A	$T_c=25^\circ\text{C}$ Note*1,2
		26.8	A	$T_c=100^\circ\text{C}$ Note*1,2
Pulsed Diode Forward Current	I_{DRP}	125.6	A	Note *2
Peak Diode Recovery dv/dt	dv/dt	30	V/ns	Note *5
Peak Diode Recovery $-di_{DR}/dt$	$-di_{DR}/dt$	100	A/ μs	Note *6
Maximum Power Dissipation	P_{tot}	263	W	$T_c=25^\circ\text{C}$
		2.78	W	$T_a=25^\circ\text{C}$
Operating Channel Temperature	T_{ch}	150	$^\circ\text{C}$	
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$	

Note *1 : Maximum duty cycle $D=0.55$

Note *2 : Limited by maximum channel temperature.

Note *3 : $T_{ch} \leq 150^\circ\text{C}$, See Figure 1 and 2.

Note *4 : Starting $T_{ch} = 25^\circ\text{C}$, $I_{AS} = 3.3\text{ A}$, $L = 162\text{ mH}$, $V_{DD} = 60\text{ V}$, $R_G = 50\ \Omega$, See Figure 1 and 2.

E_{AS} limited by maximum channel temperature and avalanche current.

Note *5 : $I_{DR} \leq 37.1\text{ A}$, $-di_{DR}/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq 600\text{ V}$, $T_{ch} \leq 150^\circ\text{C}$.

Note *6 : $I_{DR} \leq 37.1\text{ A}$, $dv/dt \leq 30\text{ V/ns}$, $V_{DS\text{ peak}} \leq 600\text{ V}$, $T_{ch} \leq 150^\circ\text{C}$.

■ Electrical Characteristics at $T_c=25^\circ\text{C}$ (unless otherwise specified)

• Static characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$ $I_D = 250\ \mu\text{A}$	600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 5.6\ \text{mA}$	3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$ $V_{GS} = 0\text{ V}$ $T_{ch} = 25^\circ\text{C}$	-	-	25	μA
		$V_{DS} = 480\text{ V}$ $V_{GS} = 0\text{ V}$ $T_{ch} = 125^\circ\text{C}$	-	-	270	
Gate-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}$ $V_{GS} = \pm 30\text{ V}$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 9.3\ \text{A}$	-	0.083	0.093	Ω
Gate resistance	r_g	$f = 1\ \text{MHz}$, open drain	-	7.2	-	Ω

• Dynamic characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}$ $I_D = 18.6\ \text{A}$	7.5	30	-	S
Input Capacitance	C_{iss}	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 250\ \text{kHz}$	-	1950	-	μF
Output Capacitance	C_{oss}		-	67	-	
Reverse Transfer Capacitance	C_{rss}		-	8.6	-	
Effective output capacitance, energy related (Note *7)	$C_{o(er)}$	$V_{DS} = 0 \dots 400\text{ V}$ $V_{GS} = 0\text{ V}$	-	160	-	pF
Effective output capacitance, time related (Note *8)	$C_{o(tr)}$	$V_{DS} = 0 \dots 400\text{ V}$ $V_{GS} = 0\text{ V}$ $I_D = \text{constant}$	-	660	-	
Turn-On Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$, $V_{GS} = 10\text{ V}$ $I_D = 18.6\ \text{A}$, $R_G = 18\ \Omega$	-	31	-	ns
	t_t		-	20	-	
Turn-Off Time	$t_{d(off)}$	See Figure 3 and 4	-	247	-	
	t_t		-	23	-	
Total Gate Charge	Q_G	$V_{DD} = 400\text{ V}$, $V_{GS} = 10\text{ V}$	-	93	-	nC
Gate-Source Charge	Q_{GS}	$I_D = 37.1\ \text{A}$	-	31	-	
Gate-Drain Charge	Q_{GD}	See Figure 5	-	43	-	

Note *7 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

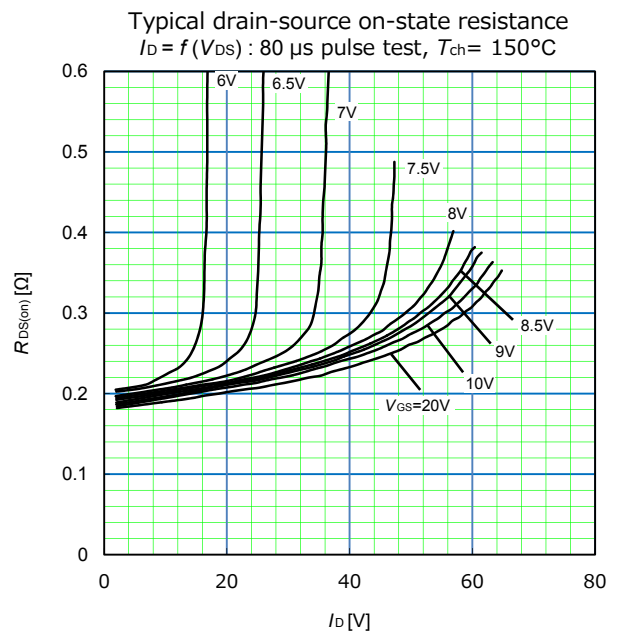
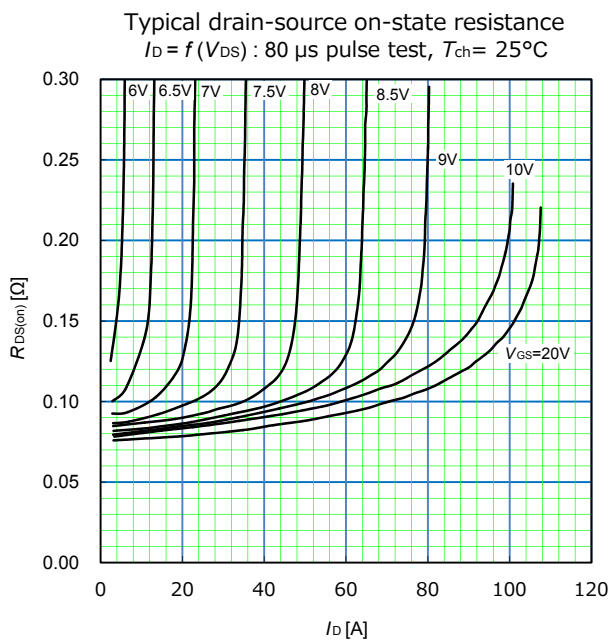
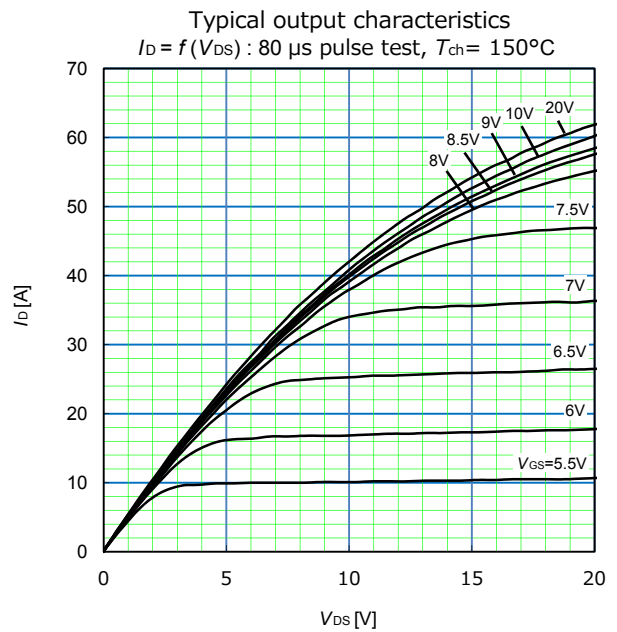
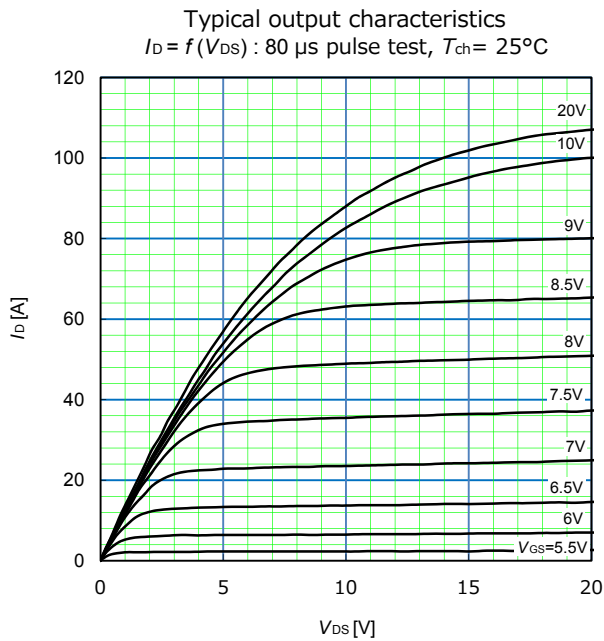
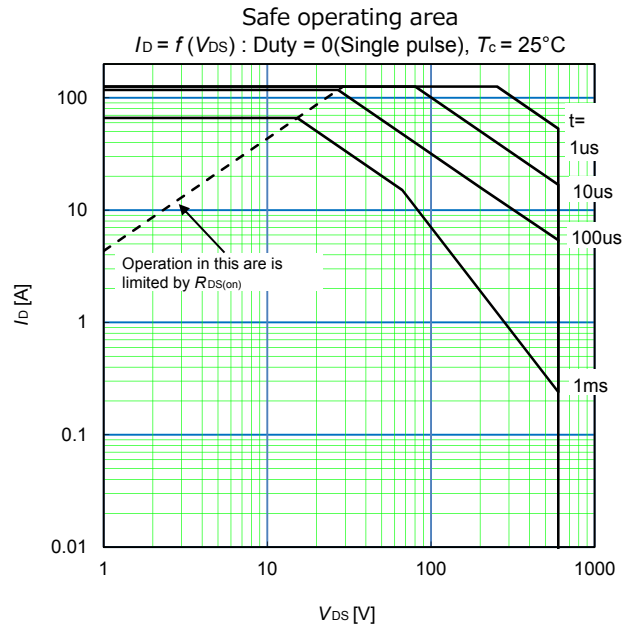
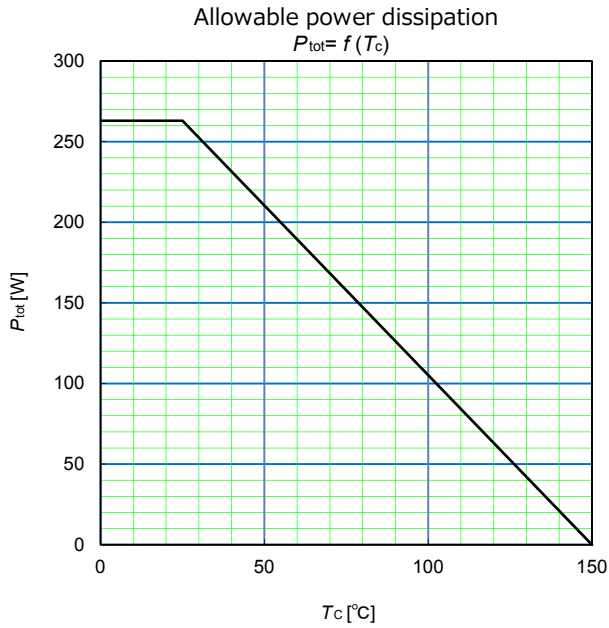
Note *8 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400 V.

• Reverse diode characteristics

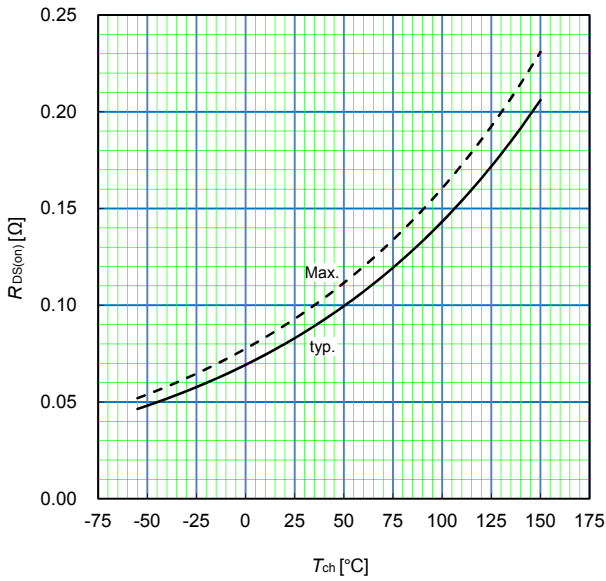
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode Forward On-Voltage	V_{DSR}	$I_{DR} = 37.1\ \text{A}$, $V_{GS} = 0\text{ V}$ $T_{ch} = 25^\circ\text{C}$	-	1.00	1.35	V
Reverse Recovery Time	t_{rr}	$V_{DD} = 400\text{ V}$ $I_{DR} = 37.1\ \text{A}$ $V_{GS} = 0\text{ V}$ $-di_{DR}/dt = 100\ \text{A}/\mu\text{s}$ $T_{ch} = 25^\circ\text{C}$	-	190	-	ns
Reverse Recovery Charge	Q_{rr}		-	1.6	-	μC
Peak Reverse Recovery Current	I_{rrm}		See Figure 6 and 7	-	16	-

■ Thermal Resistance

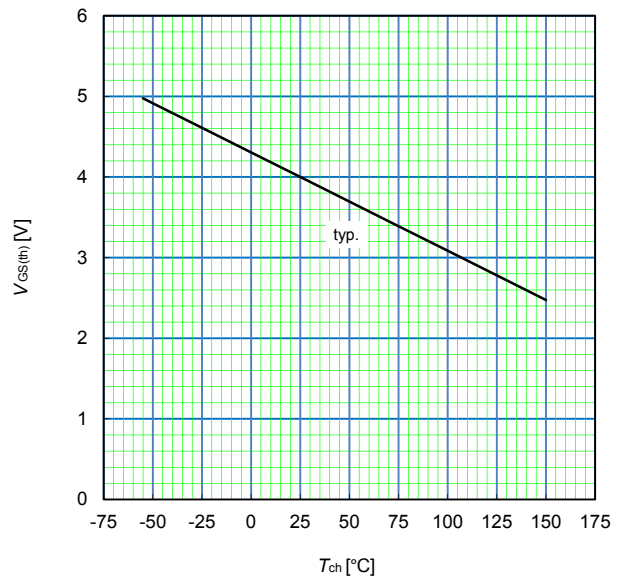
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance, Channel – Ambient	$R_{th(ch-a)}$	Device mounted on PCB (FR4) Size: 40mm*40mm*1.5mm with 6cm ² copper area (one layer, 70 μm thickness) for drain connection and cooling.	-	-	45	$^\circ\text{C}/\text{W}$
Thermal Resistance, Channel – Case	$R_{th(ch-c)}$		-	-	0.475	$^\circ\text{C}/\text{W}$



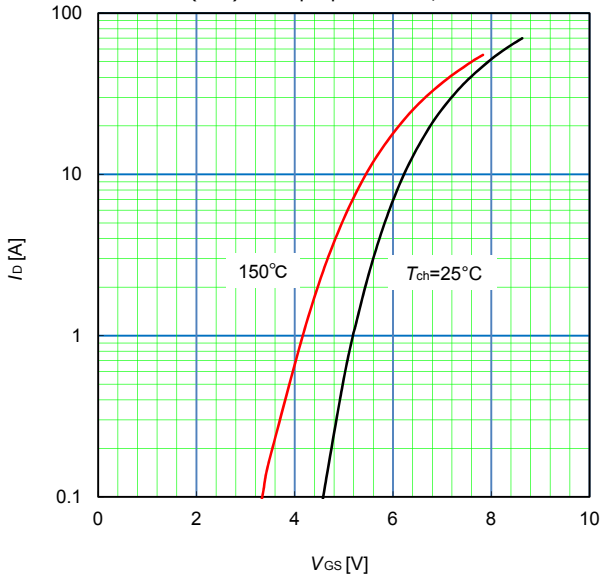
Drain-source on-state resistance
 $R_{DS(on)} = f(T_{ch}) : I_D = 18.6 \text{ A}, V_{GS} = 10 \text{ V}$



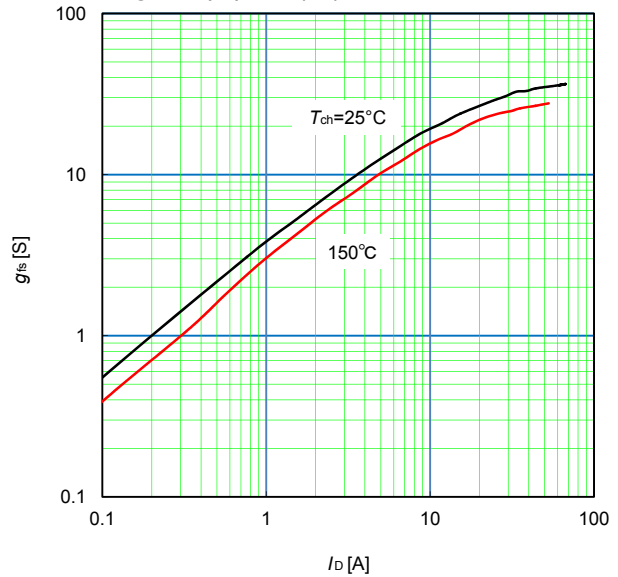
Gate threshold voltage
 $V_{GS(th)} = f(T_{ch}) : V_{DS} = V_{GS}, I_D = 5.6 \text{ mA}$



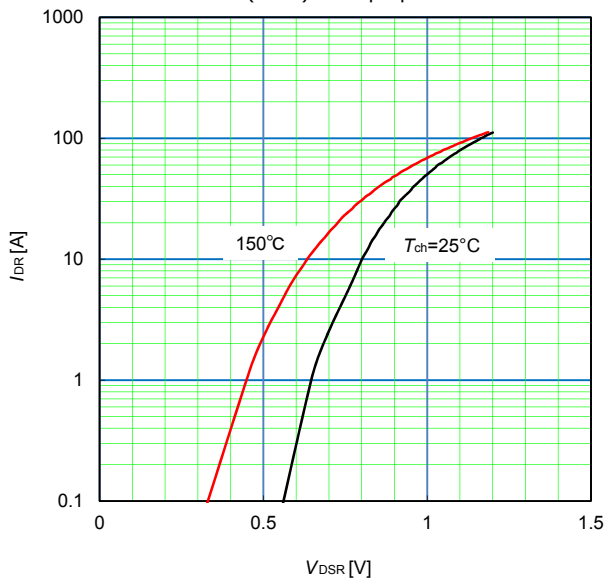
Typical transfer characteristic
 $I_D = f(V_{GS}) : 80 \mu\text{s pulse test}, V_{DS} = 25 \text{ V}$



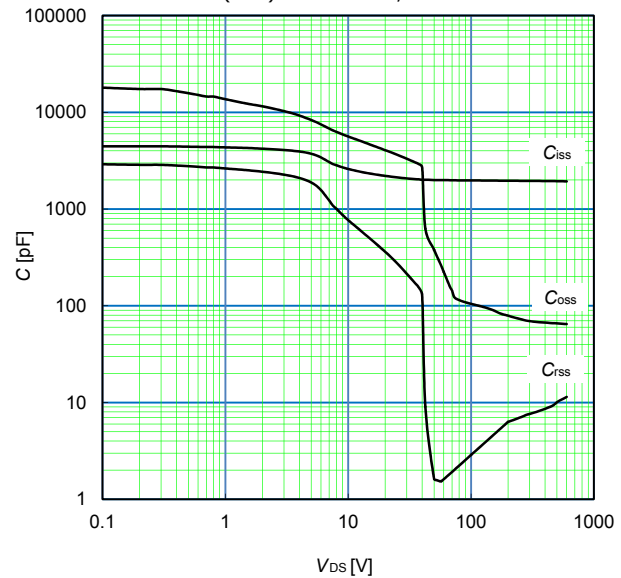
Typical transconductance
 $g_{fs} = f(I_D) : 80 \mu\text{s pulse test}, V_{DS} = 25 \text{ V}$



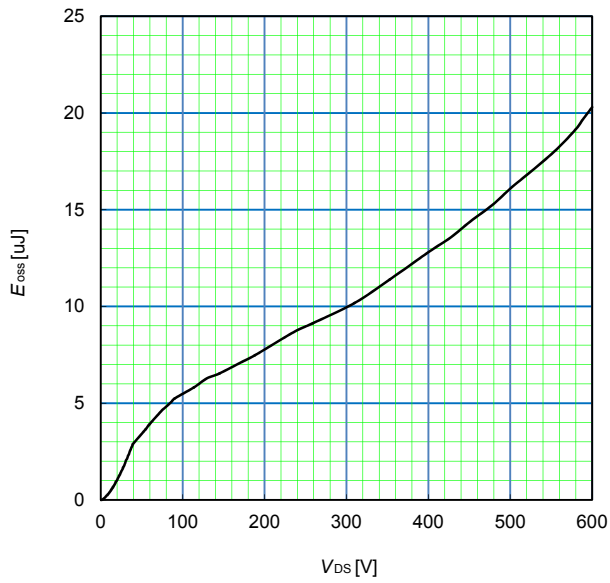
Typical forward characteristics of reverse diode
 $I_{DR} = f(V_{DSR}) : 80 \mu\text{s pulse test}$



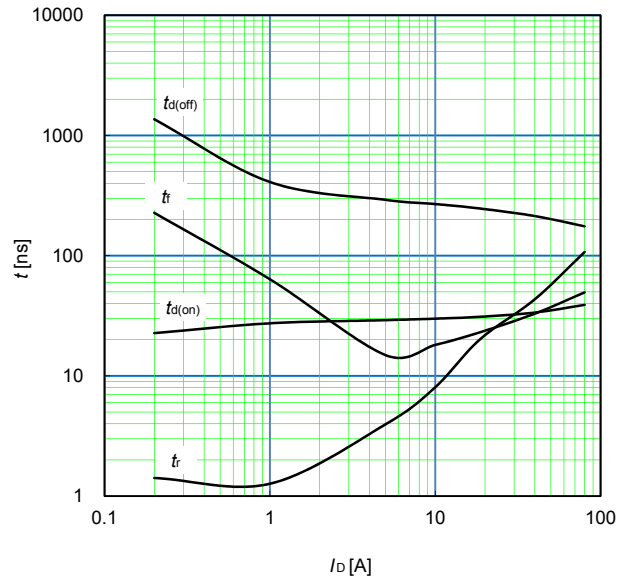
Typical capacitance
 $C = f(V_{DS}) : V_{GS} = 0 \text{ V}, f = 250 \text{ kHz}$



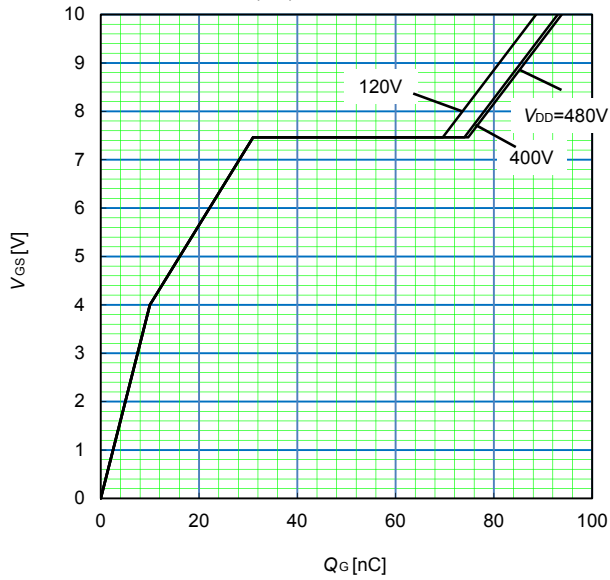
Typical C_{oss} stored energy



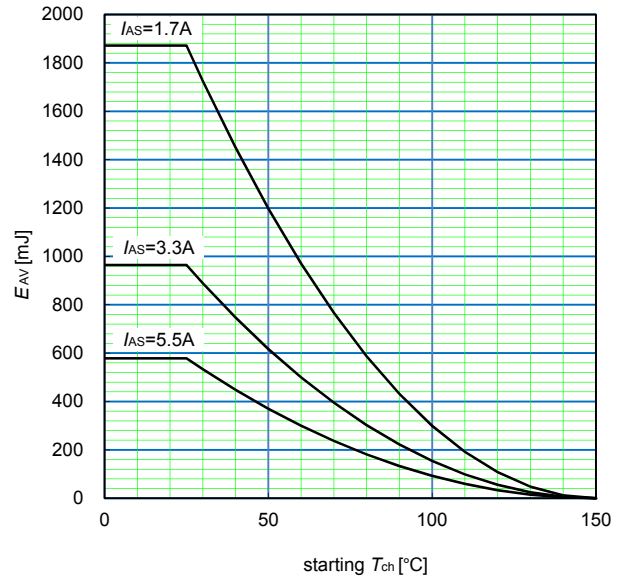
Typical switching times vs. I_D
 $t = f(I_D) : V_{DD} = 400 \text{ V}, V_{GS} = 10 \text{ V/0 V}, R_G = 18 \Omega, T_{ch} = 25^\circ\text{C}$



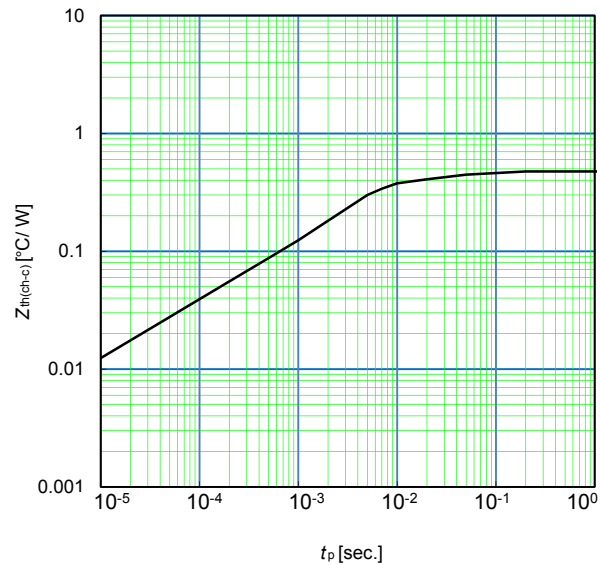
Typical gate charge
 $V_{GS} = f(Q_G) : I_D = 37.1 \text{ A}, T_{ch} = 25^\circ\text{C}$



Maximum Avalanche Energy
 $E_{AV} = f(\text{starting } T_{ch}) : V_{DD} = 60 \text{ V}, I_{AS} \leq 5.5 \text{ A}$



Transient Thermal Impedance
 $Z_{th(ch-c)} = f(t) : D = 0$



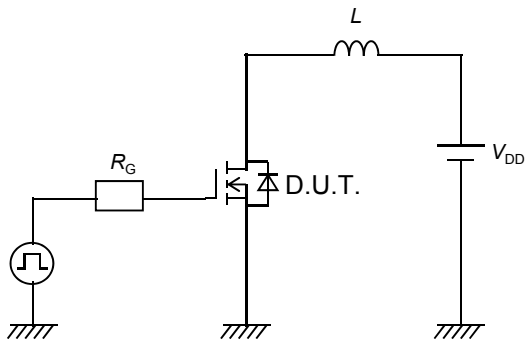


Figure 1. Unclamped inductive load test circuit

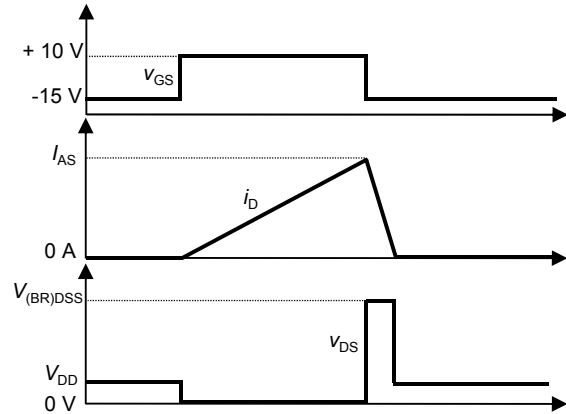


Figure 2. Unclamped inductive waveform

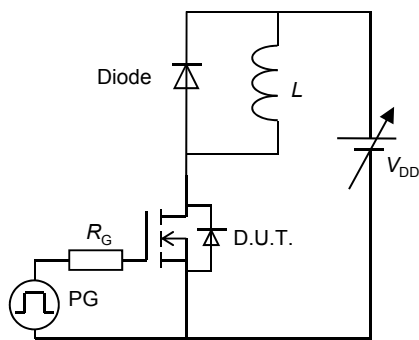


Figure 3. Switching test circuit

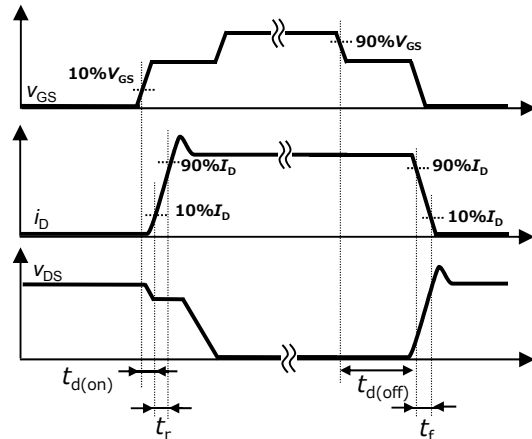


Figure 4. Switching times waveform

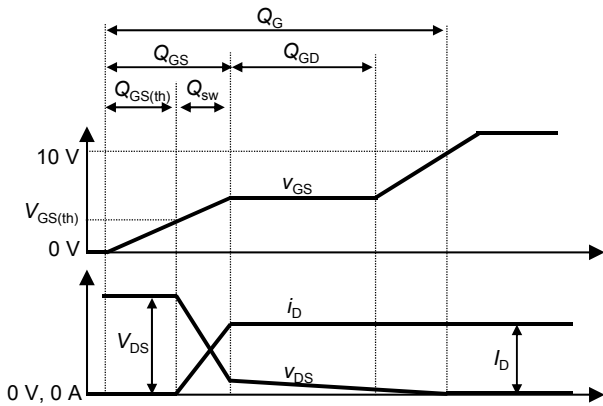
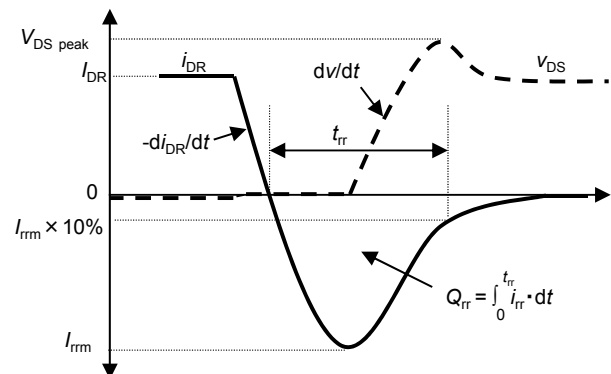
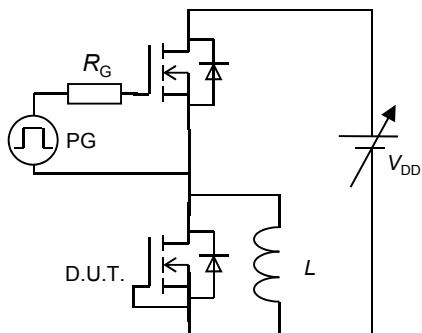
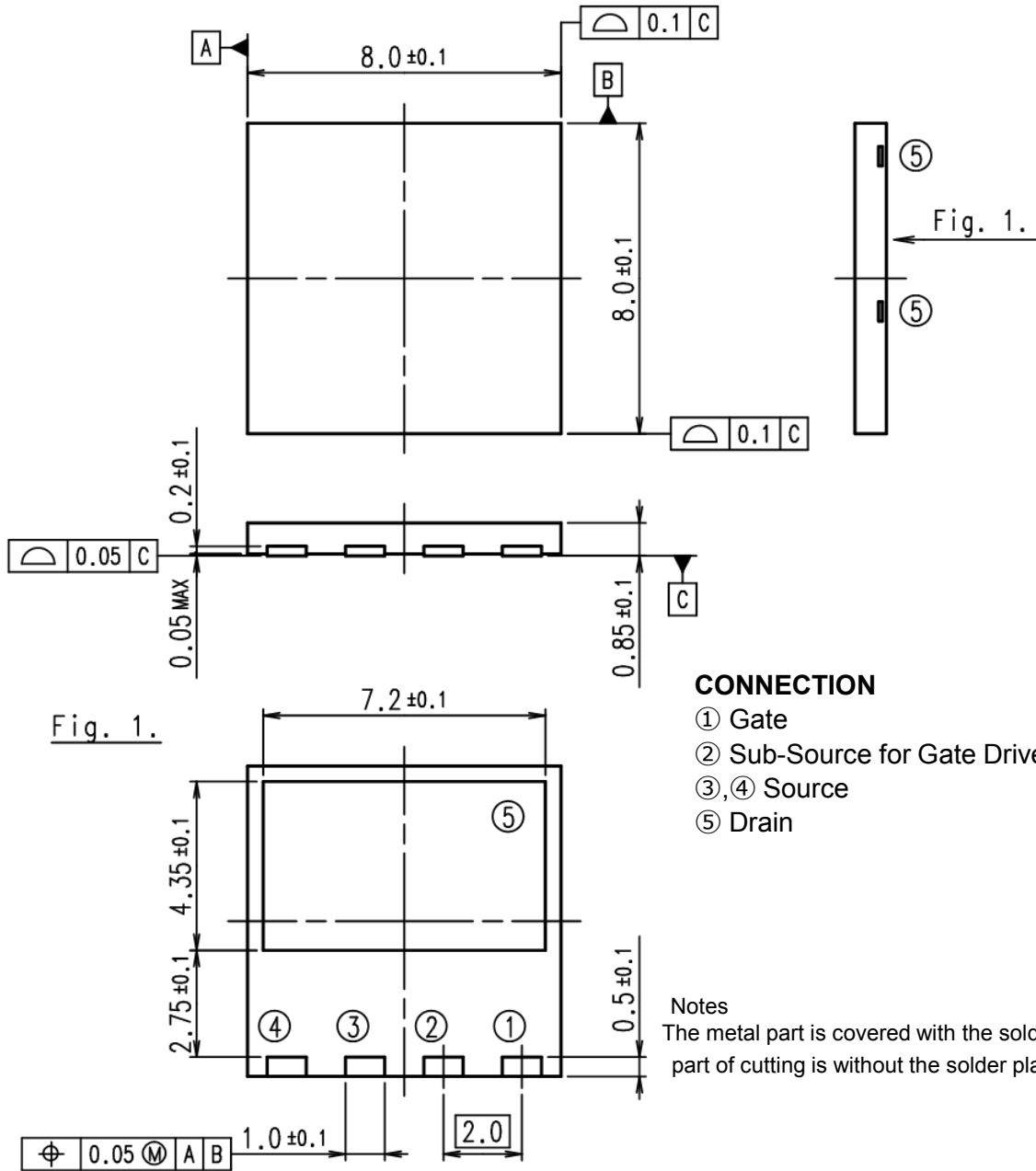


Figure 5. Gate charge waveform



■ Package Dimensions : DFN8x8 Package



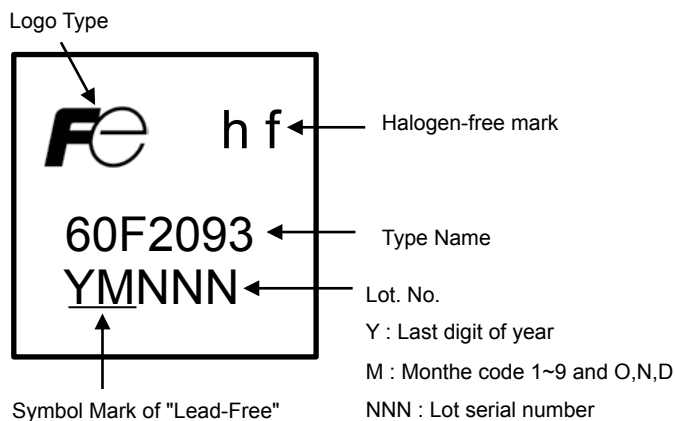
CONNECTION

- ① Gate
- ② Sub-Source for Gate Drive
- ③,④ Source
- ⑤ Drain

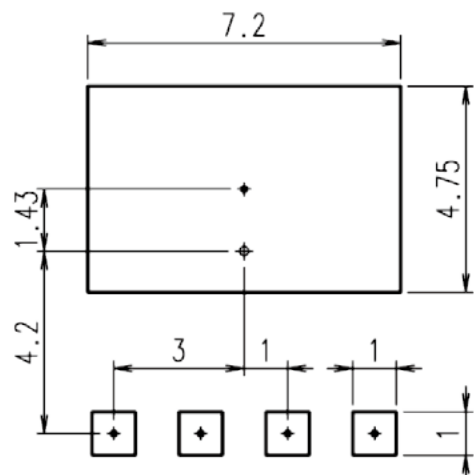
Notes

The metal part is covered with the solder plating, part of cutting is without the solder plating.

■ Marking



■ Recommended footprint



DIMENSIONS ARE IN MILLIMETERS

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