FMW60N190S2HF

http://www.fujielectric.com/products/semiconductor/
FUJI POWER MOSFET

Super J MOS® S2 series

N-Channel enhancement mode power MOSFET

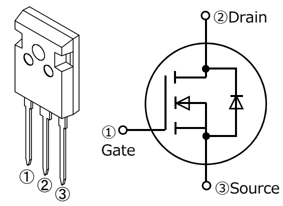
Features

Pb-free lead terminal
RoHS compliant
uses Halogen-free molding compound

Applications

For switching

Equivalent circuit schematic



Absolute Maximum Ratings at T_C=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	V_{GS}=-30V
Continuous Drain Current	I_D	20	A	T_C=25°C Note*1,2
		12.6	A	T_C=100°C Note*1,2
Pulsed Drain Current	I_{DP}	62	A	Note *2
Gate-Source Voltage	V_{GS}	±30	V	
Non-Repetitive Maximum Avalanche Current	I_{AS}	2.3	A	Note *3
Non-Repetitive Maximum Avalanche Energy	E_{AS}	559	mJ	Note *4
Maximum Drain-Source dV/dt	dV_{DS}/dt	50	V/ns	V_{DS}≤ 600V
Continuous Diode Forward Current	I_{SD}	20	A	T_C=25°C Note*1,2
		12.6	A	T_C=100°C Note*1,2
Pulsed Diode Forward Current	I_{SDP}	62	A	Note *2
Peak Diode Recovery dV/dt	dV/dt	15	V/ns	Note *5
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *6
Maximum Power Dissipation	P_D	2.5	W	T_a=25°C
		94		T_C=25°C
Operating and Storage Temperature range	T_{ch}	150	°C	
	T_{stg}	-55 to +150	°C	

Note *1 : Maximum duty cycle D=0.65
Note *2 : Limited by maximum channel temperature.
Note *3 : T_{ch}≤150°C, See Fig.1 and Fig.2
Note *4 : Starting T_{ch}=25°C, I_{AS}=1.4A, L=559mH, V_{DD}=60V, R_G=50Ω, See Fig.1 and Fig.2
E_{AS} limited by maximum channel temperature and avalanche current.
Note *5 : I_{SD}≤15.5A, -di/dt≤100A/μs, $V_{DS\ peak}$≤ 600V, T_{ch}≤150°C.
Note *6 : I_{SD}≤15.5A, dV/dt≤15V/ns, $V_{DS\ peak}$≤ 600V, T_{ch}≤150°C.

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MARCH 2017

Electrical Characteristics at T_c=25°C (unless otherwise specified)

• Static Ratings

Parameter	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA		600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=250μA		2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=600V V_{GS}=0V	T_{ch}=25°C	-	-	25	μA
		V_{DS}=480V V_{GS}=0V	T_{ch}=125°C	-	-	250	
Gate-Source Leakage Current	I_{GSS}	V_{DS}=0V V_{GS}= ± 30V		-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V I_D=7.8A		-	0.169	0.190	Ω
Gate resistance	R_G	f=1MHz, open drain		-	10.9	-	Ω

• Dynamic Ratings

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g_{fs}	V_{DS}=25V I_D=7.8A	7.2	14.5	-	S
Input Capacitance	C_{iss}	V_{DS}=400V V_{GS}=0V f=250kHz	-	1130	-	pF
Output Capacitance	C_{oss}		-	30	-	
Reverse Transfer Capacitance	C_{rss}		-	4.4	-	
Effective output capacitance, energy related (Note *7)	$C_{o(er)}$	V_{DS}=0…400V V_{GS}=0V	-	69	-	
Effective output capacitance, time related (Note *8)	$C_{o(tr)}$	V_{DS}=0…400V V_{GS}=0V I_D=constant	-	251	-	
Turn-On Time	$t_{d(on)}$	V_{DD}=400V, V_{GS}=10V I_D=7.8A, R_G=18Ω See Fig.3 and Fig.4	-	18	-	ns
	t_r		-	30	-	
Turn-Off Time	$t_{d(off)}$		-	143	-	
	t_f		-	22	-	
Total Gate Charge	Q_G	V_{DD}=400V, V_{GS}=10V I_D=15.5A See Fig.5	-	46	-	nC
Gate-Source Charge	Q_{GS}		-	12	-	
Gate-Drain Charge	Q_{GD}		-	14	-	
Drain-Source crossover Charge	Q_{SW}		-	7	-	

Note *7 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
Note *8 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

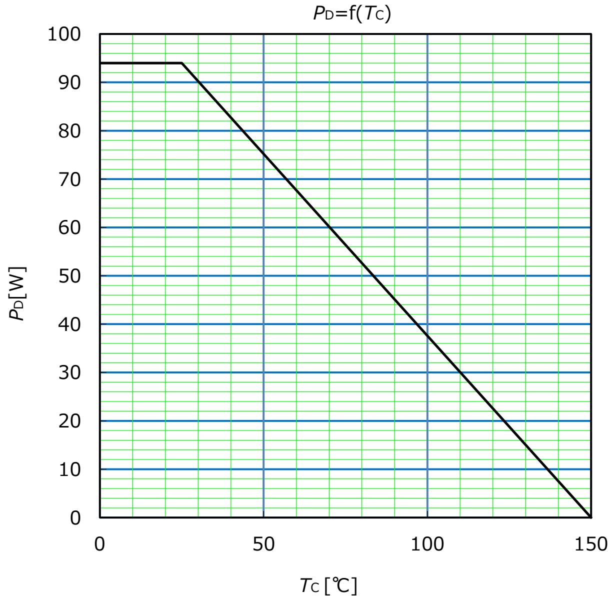
• Reverse Diode

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Diode Forward On-Voltage	V_{SD}	I_{SD}=15.5A, V_{GS}=0V T_{ch}=25°C	-	0.90	1.35	V
Reverse Recovery Time	t_{rr}	V_{DD}=400V, I_{SD}=15.5A -di/dt=100A/μs T_{ch}=25°C See Fig.6 and Fig.7	-	328	-	ns
Reverse Recovery Charge	Q_{rr}		-	4.2	-	μC
Peak Reverse Recovery Current	I_{rp}		-	25	-	A

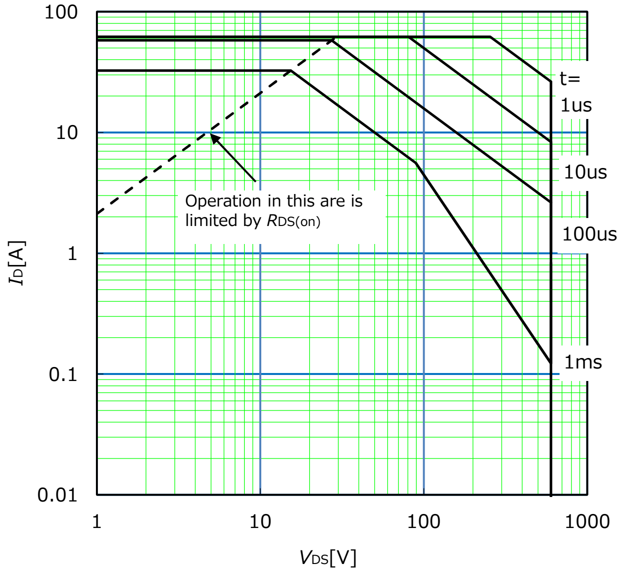
Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	$R_{th(ch-c)}$	-	-	1.33	°C/W
Channel to Ambient	$R_{th(ch-a)}$	-	-	50	°C/W

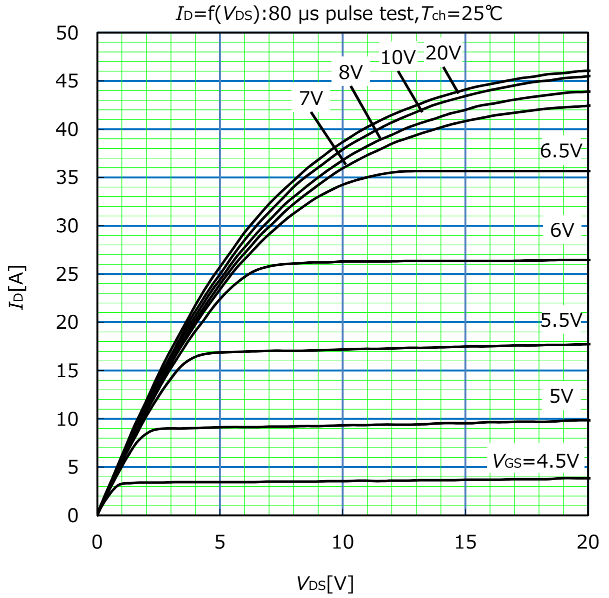
Allowable Power Dissipation
PD=f(TC)



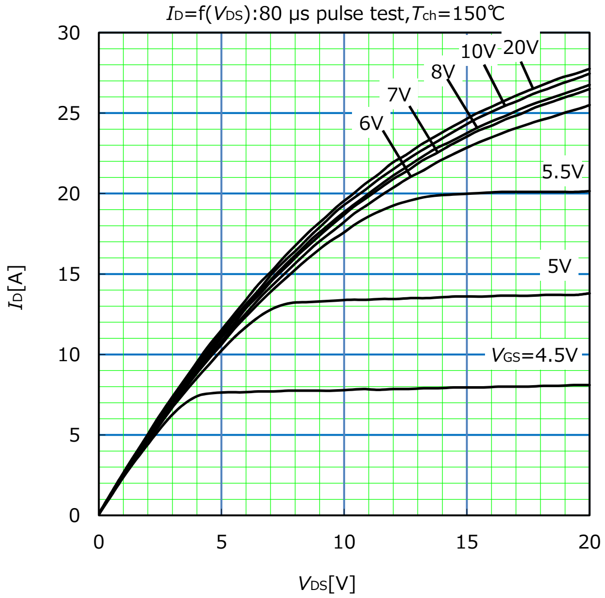
Safe Operating Area
ID=f(VDS):Duty=0(Single pulse),TC=25℃



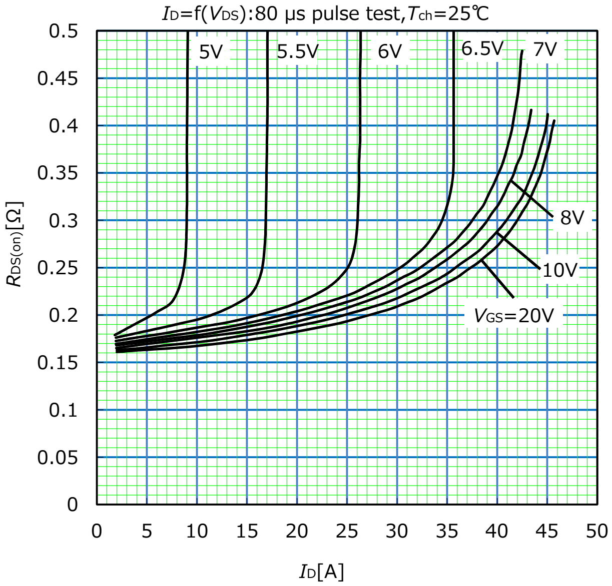
Typical Output Characteristics
ID=f(VDS):80 μs pulse test,Tch=25℃



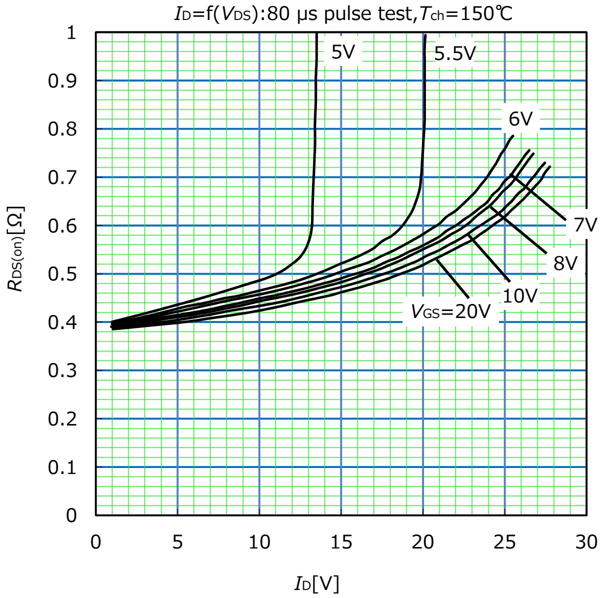
Typical Output Characteristics
ID=f(VDS):80 μs pulse test,Tch=150℃



Typical Output Characteristics
ID=f(VDS):80 μs pulse test,Tch=25℃

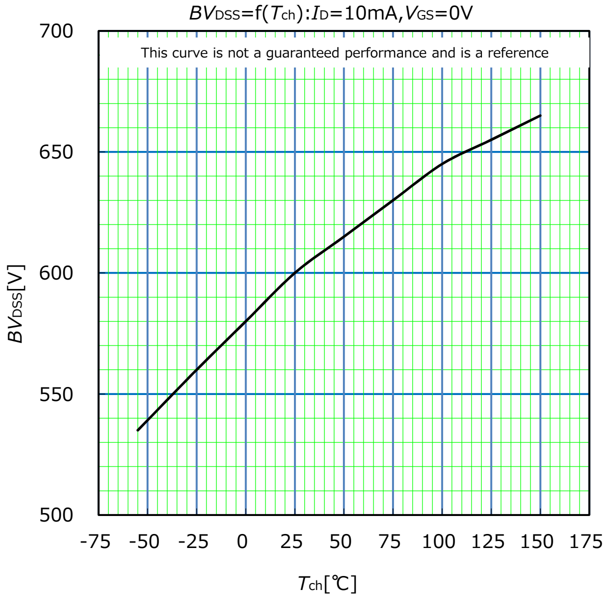


Typical Output Characteristics
ID=f(VDS):80 μs pulse test,Tch=150℃



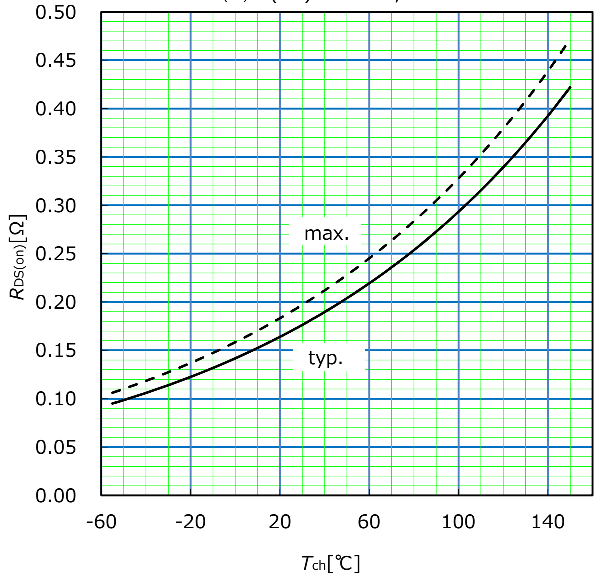
Drain-Source Breakdown Voltage

BV_{DSS}=f(T_{ch}):I_D=10mA,V_{GS}=0V



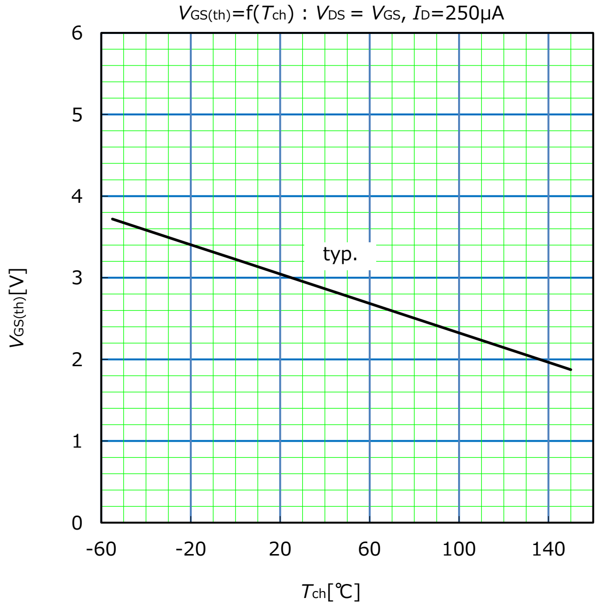
Drain-Source On-state Resistance

$R_{DS(on)}$=f(T_{ch}):I_D=7.8A,V_{GS}=10V



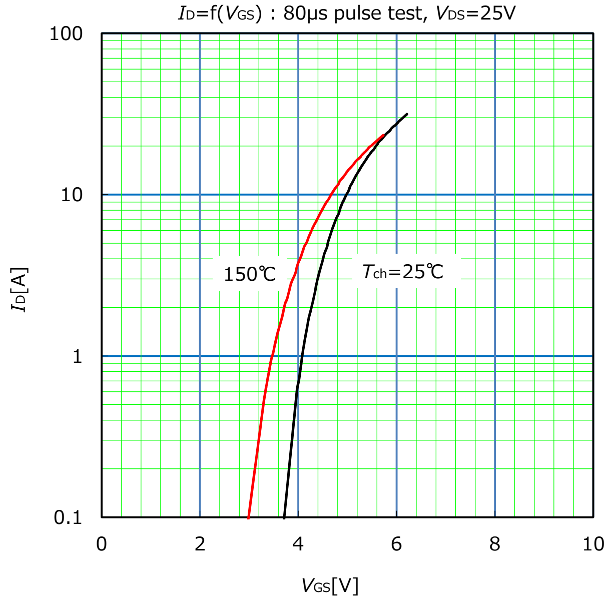
Gate Threshold Voltage vs. T_{ch}

$V_{GS(th)}$=f(T_{ch}) : V_{DS} = V_{GS}, I_D=250μA



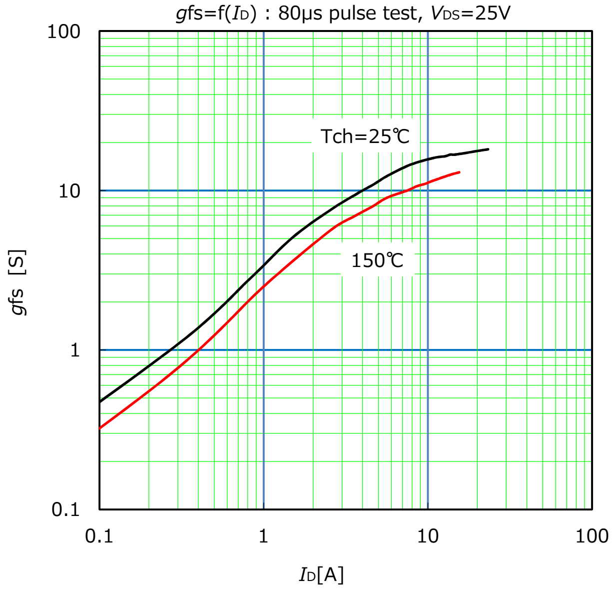
Typical Transfer Characteristic

I_D=f(V_{GS}) : 80μs pulse test, V_{DS}=25V



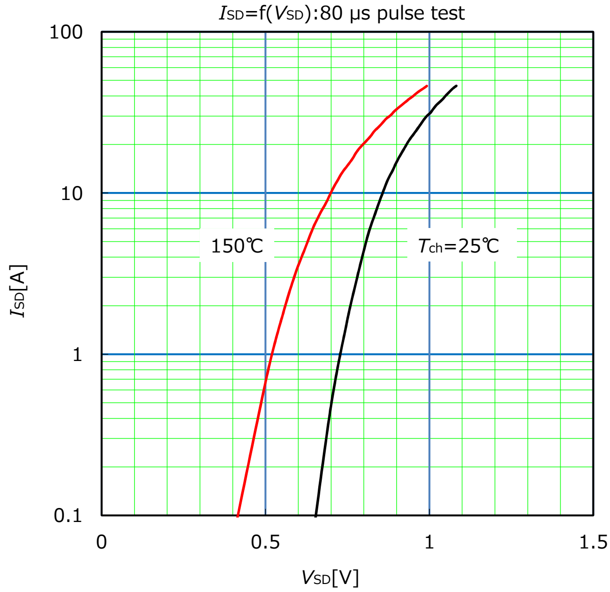
Typical Transconductance

g_{fs}=f(I_D) : 80μs pulse test, V_{DS}=25V

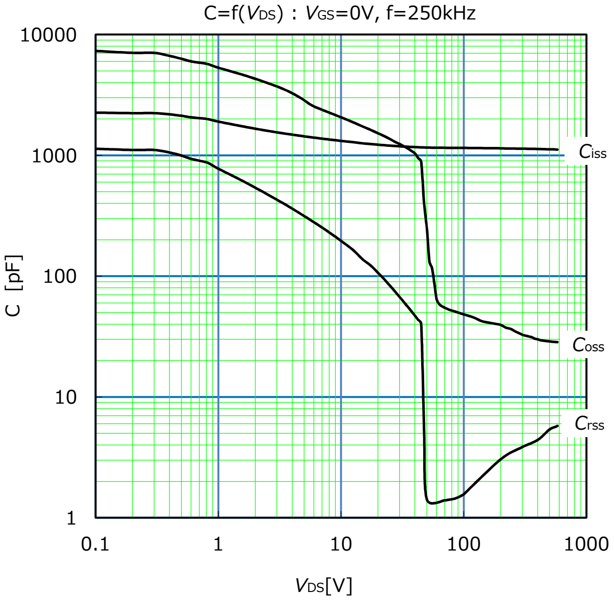


Typical Forward Characteristics of Reverse Diode

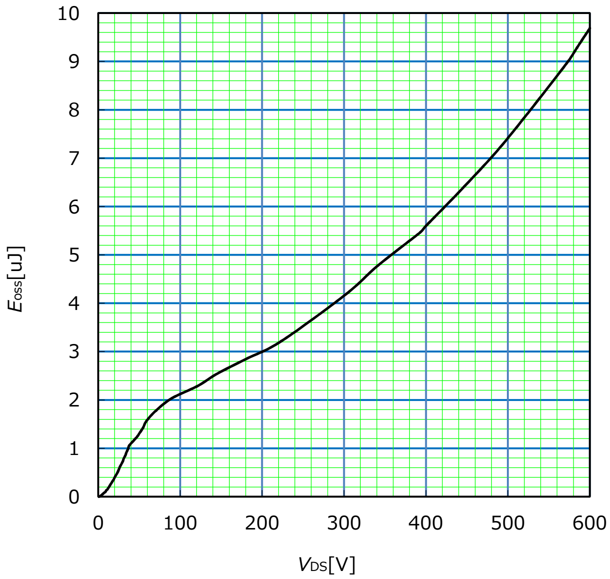
I_{SD}=f(V_{SD}):80 μs pulse test



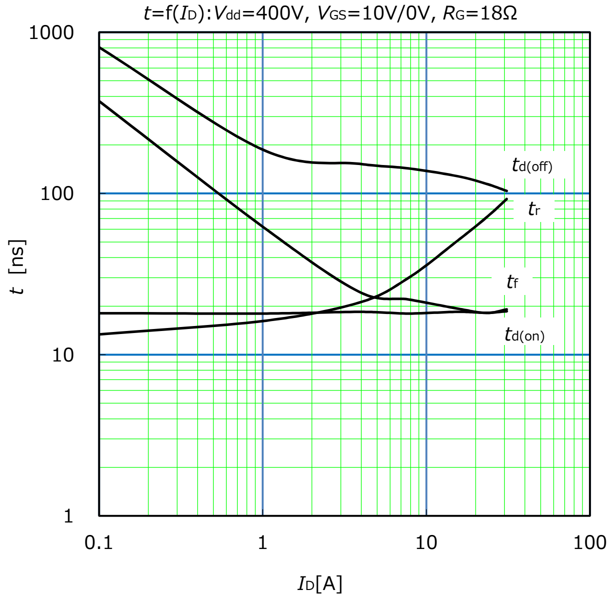
Typical Capacitance
C=f(VDS) : VGS=0V, f=250kHz



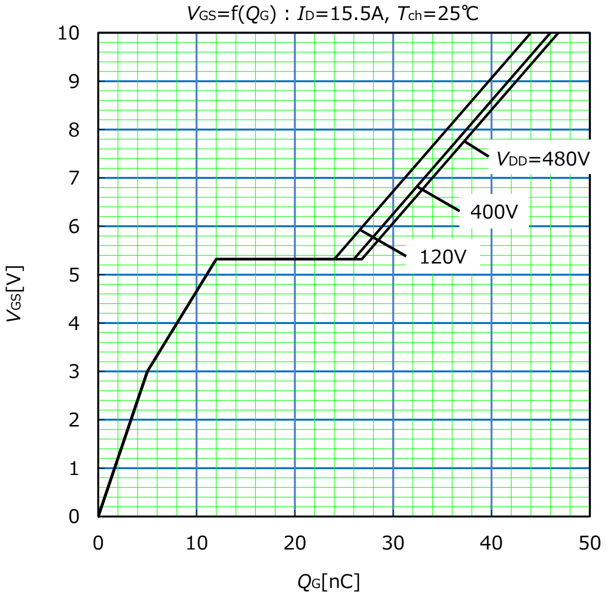
Typical Coss stored energy



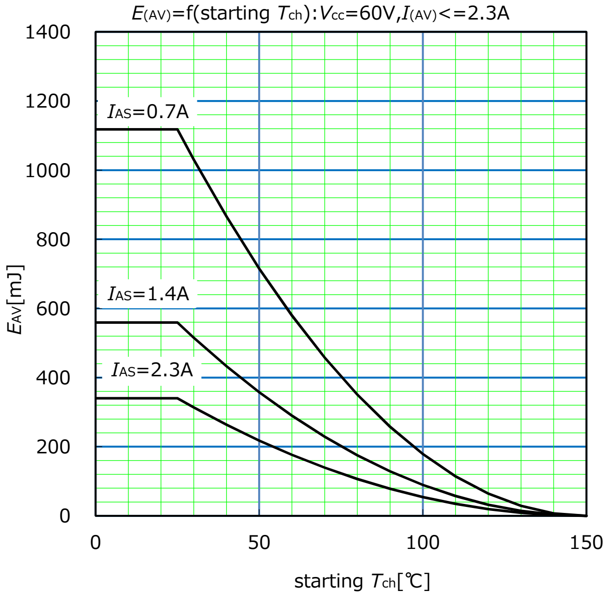
Typical Switching Characteristics vs. ID Tch=25℃
t=f(ID):Vdd=400V, VGS=10V/0V, RG=18Ω



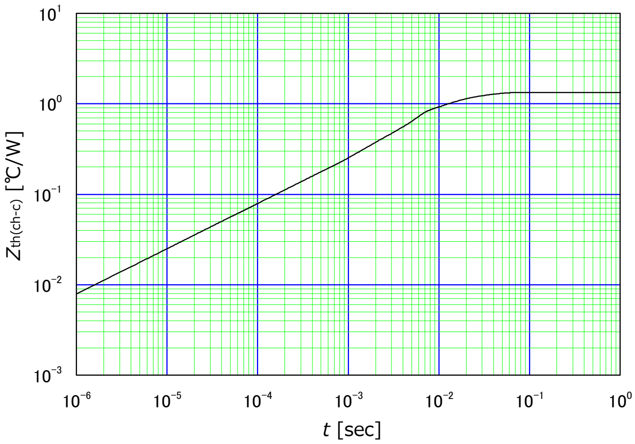
Typical Gate Charge Characteristics
VGS=f(QG) : ID=15.5A, Tch=25℃



Maximum Avalanche Energy vs. starting Tch
E(AV)=f(starting Tch):Vcc=60V,I(AV)<=2.3A



Transient Thermal Impedance
Zth(ch-c)=f(t):D=0



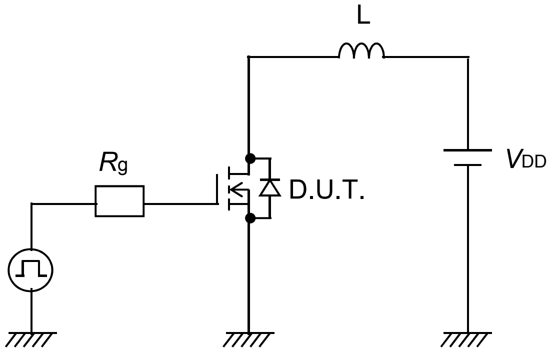


Fig.1 Avalanche Test circuit

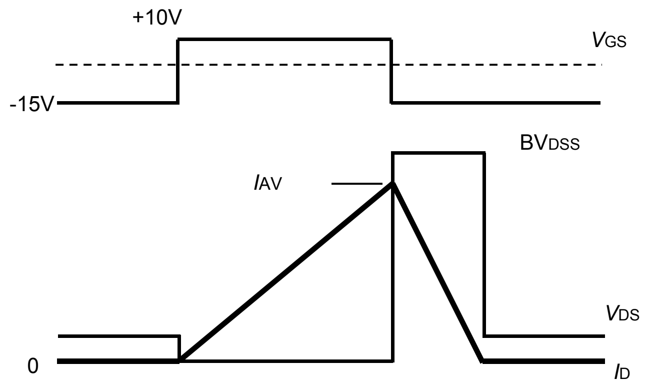


Fig.2 Operating waveforms of Avalanche Test

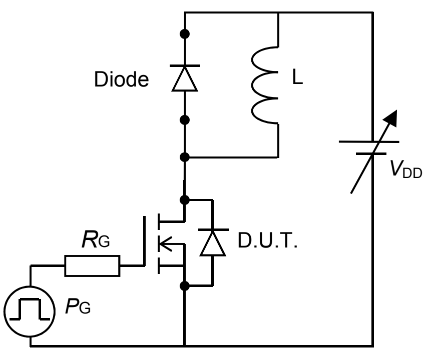


Fig.3 Switching Test circuit

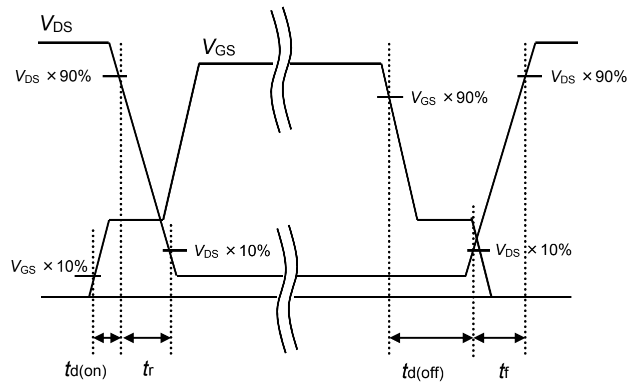


Fig.4 Operating waveform of Switching Test

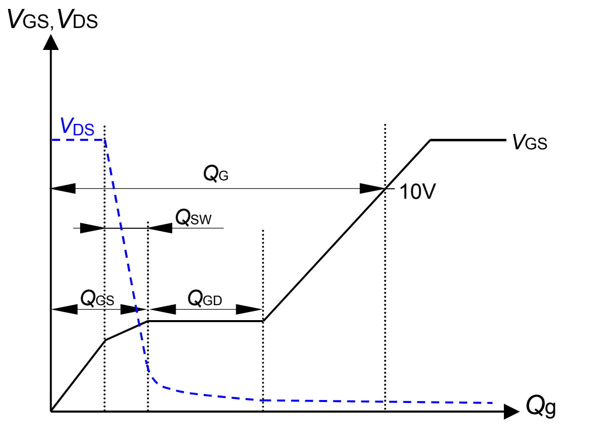


Fig.5 Operating waveform of Gate charge Test

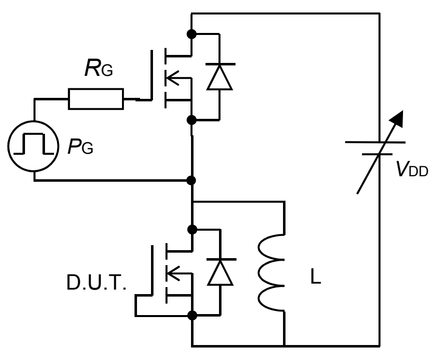


Fig.6 Reverse recovery Test circuit

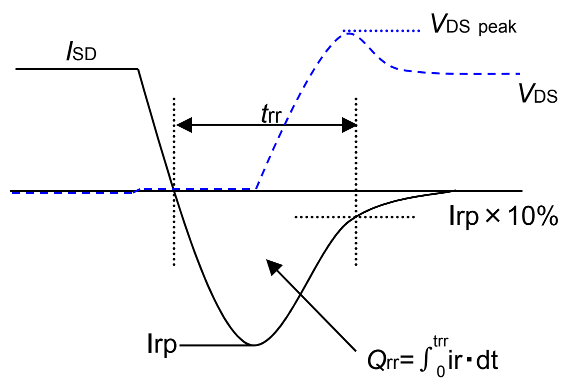
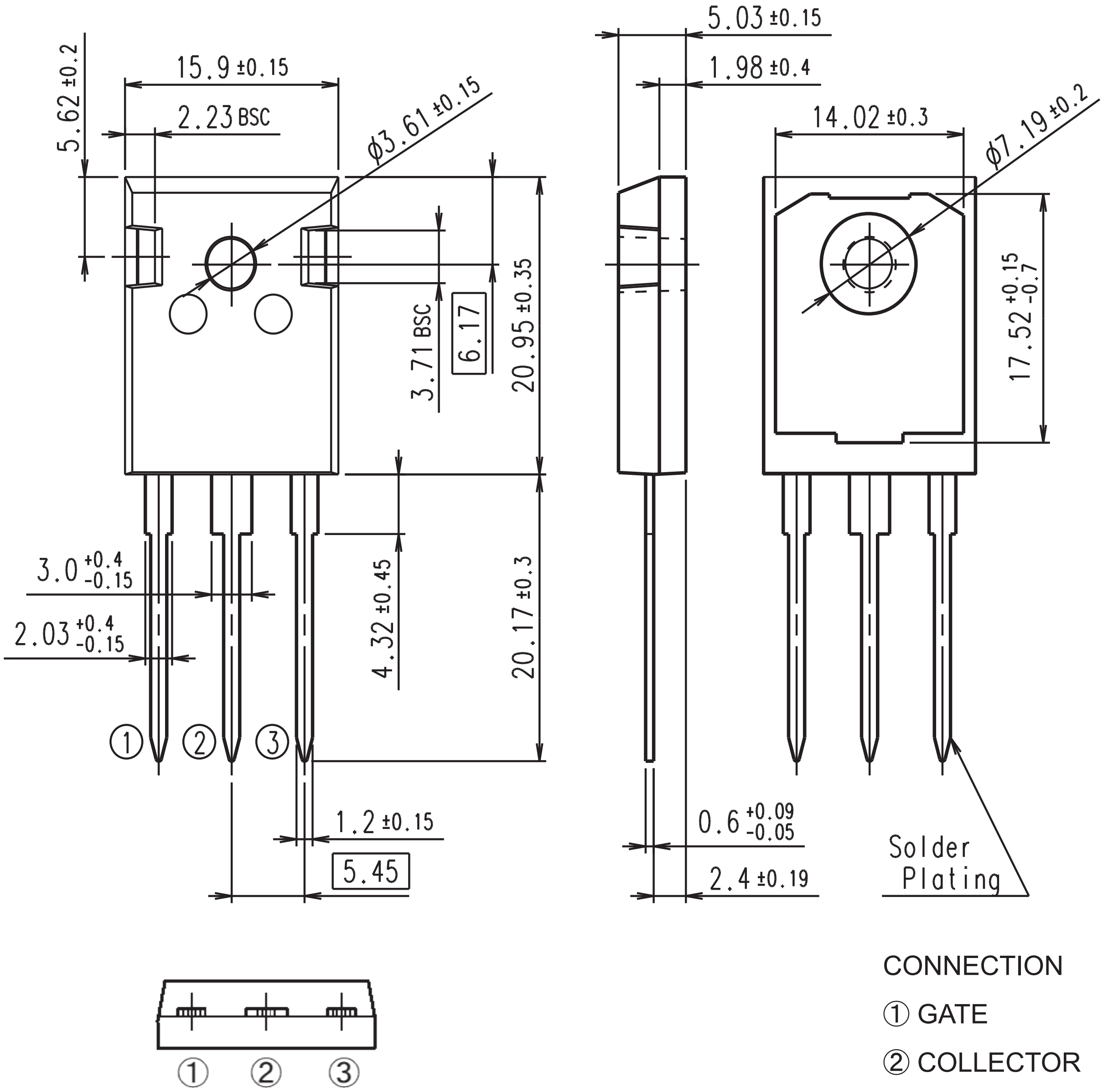


Fig.7 Operating waveform of Reverse recovery Test

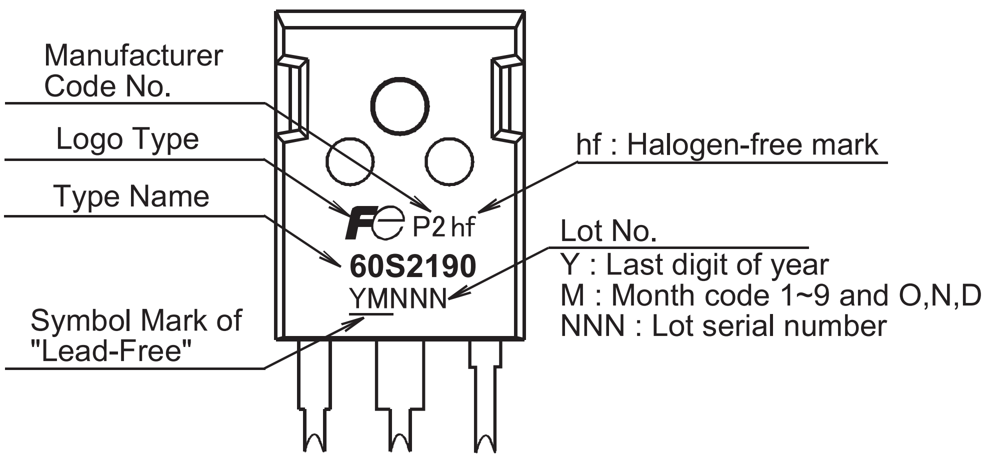
Outview: TO-247-P/TO-247-P2 Package



CONNECTION
① GATE
② COLLECTOR
③ EMITTER

DIMENSIONS ARE IN MILLIMETERS.

Marking



* The font (font type,size) and the logo type size might be actually different.

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• Medical equipment

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