

Innovating Energy Technology

http://www.fujielectric.com/products/semiconductor/ **FUJI POWER MOSFET**

Super J MOS[®] S2 series

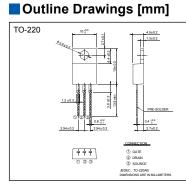
N-Channel enhancement mode power MOSFET

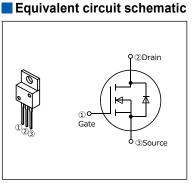
Features

Pb-free lead terminal **RoHS** compliant uses Halogen-free molding compound

Applications

For switching





Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain Course Valtere	VDS	600	V	
Drain-Source Voltage	VDSX	600	V	V _{GS} =-30V
Continuous Drain Current	,	42.3	А	Tc=25°C Note*1,2
Continuous Drain Current	I _D	26.8	А	Tc=100°C Note*1,2
Pulsed Drain Current	I DP	131	А	Note *2
Gate-Source Voltage	V _{GS}	±30	V	
Non-Repetitive Maximum Avalanche Current	las	4.9	А	Note *3
Non-Repetitive Maximum Avalanche Energy	Eas	1018	mJ	Note *4
Maximum Drain-Source dV/dt	d <i>V</i> ⊳s/dt	50	V/ns	<i>V</i> _{DS} ≤ 600V
Continuous	,	42.3	А	Tc=25°C Note*1,2
Diode Forward Current	Isd	26.8	А	Tc=100°C Note*1,2
Pulsed Diode Forward Current	ISDP	131	А	Note *2
Peak Diode Recovery dV/dt	dV/dt	30	V/ns	Note *5
Peak Diode Recovery -di/dt	-di/dt	100	A/µs	Note *6
Maximum Power Discipation	PD	2.02	W	<i>T</i> _a =25°C
Maximum Power Dissipation	r D	235	vv	<i>T</i> c=25°C
Operating and Storage Temperature range	Tch	150	°C	
Operating and Storage Temperature range	T _{stg}	-55 to +150	°C	

Note *1 : Maximum duty cycle D=0.6

Note *1 : Imited by maximum channel temperature. Note *3 : T_{ch}≤150°C, See Fig.1 and Fig.2 Note *4 : Starting T_{ch}=25°C, I_As=3A, L=207mH, V_{DD}=60V, R_G=50Ω, See Fig.1 and Fig.2 E_{AS} limited by maximum channel temperature and avalanche current. Note *5 : I_{SD}≤32.8A, -di/dt≤100A/µs, V_{DS peak}≤ 600V, T_{ch}≤150°C. Note *6 : I_{SD}≤32.8A, dV/dt≤30V/ns, V_{DS peak}≤ 600V, T_{ch}≤150°C.

Electrical Characteristics at Tc=25°C (unless otherwise specified) Static Ratings

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V₅s=0V /₀=250µA		600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =4.9mA		3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	IDSS	V _{DS} =600V V _{GS} =0V	T _{ch} =25°C	-	-	25	μA
		V _{DS} =480V V _{GS} =0V	<i>T</i> _{ch} =125°C	-	48	-	
Gate-Source Leakage Current	Igss	V _{DS} =0V V _{GS} = ± 30V	·	-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V I _D =16.4A		-	0.084	0.094	Ω
Gate resistance	RG	f=1MHz, open drain		-	7.5	-	Ω

Dynamic Ratings

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Forward Transconductance	g _{fs}	V _{DS} =25V I _D =16.4A	11	22	-	S
Input Capacitance	Ciss	V _{DS} =400V	-	1720	-	
Output Capacitance	Coss	V _{GS} =0V	-	60	-	
Reverse Transfer Capacitance	Crss	f=250kHz	-	7.9	-	
Effective output capacitance, energy related (Note *7)	C _{o(er)}	V _{DS} =0400V V _{GS} =0V	-	139	-	pF
Effective output capacitance, time related (Note *8)	C o(tr)	V _{DS} =0400V V _{GS} =0V I _D =constant	-	569	-	
Turne Our Time talon	t _{d(on)}	$V_{DD}=400V, V_{GS}=10V$ $I_{D}=16.4A,$ $R_{G}=15\Omega$ See Fig.3 and Fig.4	-	32	-	- ns
Turn-On Time	tr		-	119	-	
	t _{d(off)}		-	158	-	
Turn-Off Time	<i>t</i> r		-	27	-	
Total Gate Charge	QG	V₀₀=400V, V₀₅=10V /₀=32.8A See Fig.5	-	83	-	nC
Gate-Source Charge	Q _{GS}		-	35	-	
Gate-Drain Charge	QGD		-	39	-	
Drain-Source crossover Charge	Qsw		-	25	-	

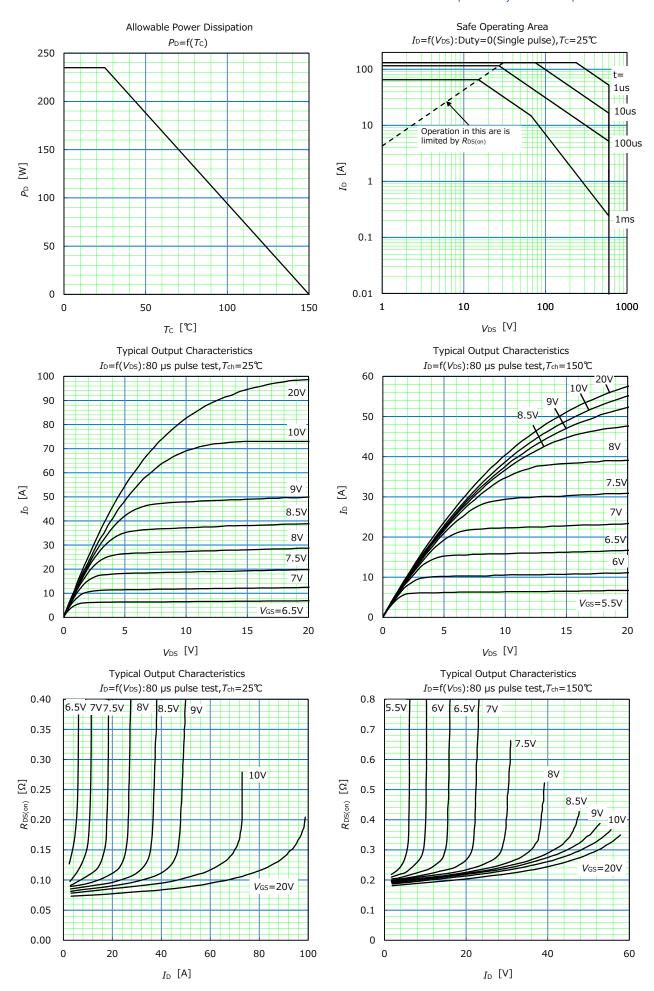
Note *7 : $C_{0(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{Os} is rising from 0 to 400V. Note *8 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{Os} is rising from 0 to 400V.

Reverse Diode

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Diode Forward On-Voltage	V _{SD}	I _{SD} =32.8A, V _{GS} =0V T _{ch} =25°C	-	0.95	1.35	V
Reverse Recovery Time	trr	- V₀₀=400V, /₅₀=32.8A -di/dt=100A/μs T₅h=25°C See Fig.6 and Fig.7	-	185	-	ns
Reverse Recovery Charge	Qrr		-	1.6	-	μC
Peak Reverse Recovery Current	Irp		-	15.8	-	А

Thermal Resistance

Parameter	Symbol	Min.	Тур.	Max.	Unit
Channel to Case	Rth(ch-c)	-	-	0.53	°C/W
Channel to Ambient	Rth(ch-a)	-	-	62	°C/W



100

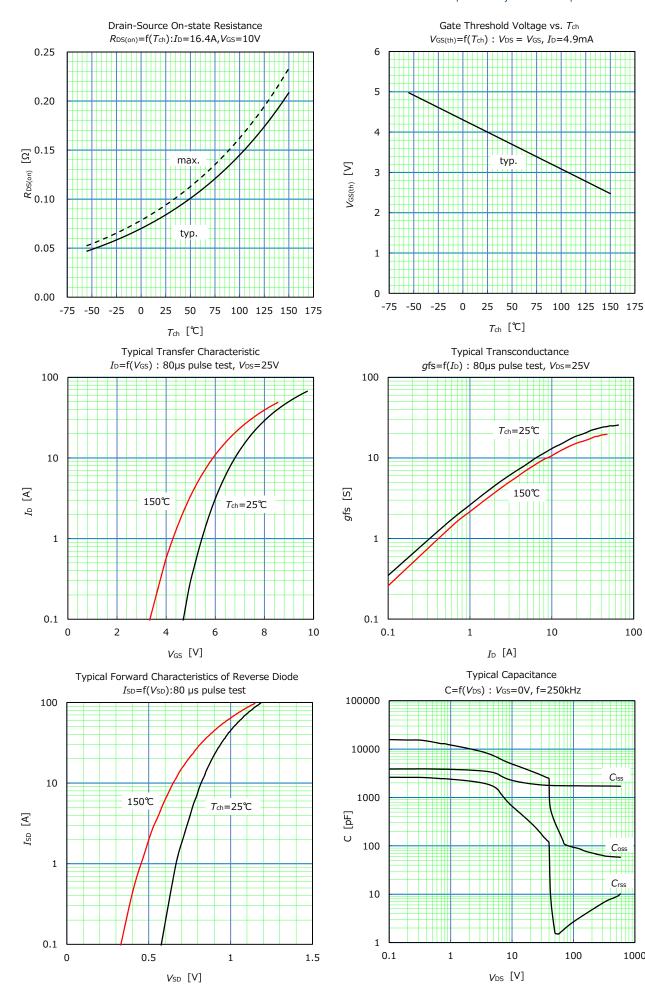
Ciss

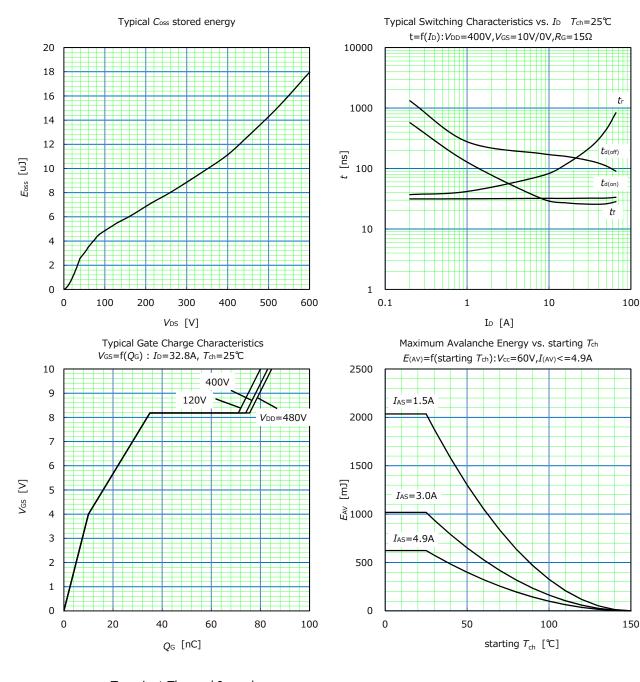
Cos

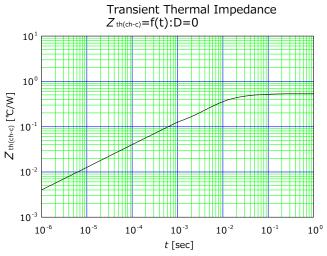
 C_{rss}

1000

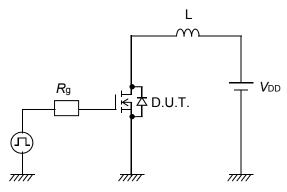
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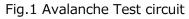






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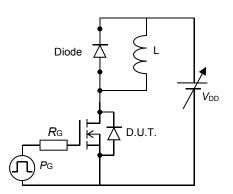


Fig.3 Switching Test circuit

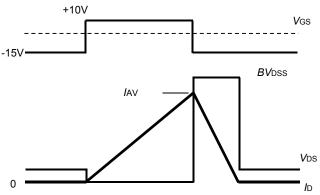


Fig.2 Operating waveforms of Avalanche Test

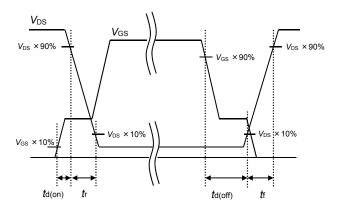


Fig.4 Operating waveform of Switching Test

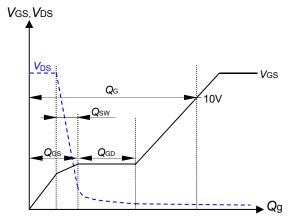
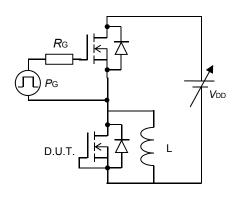


Fig.5 Operating waveform of Gate charge Test



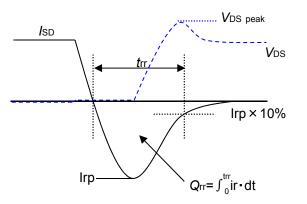
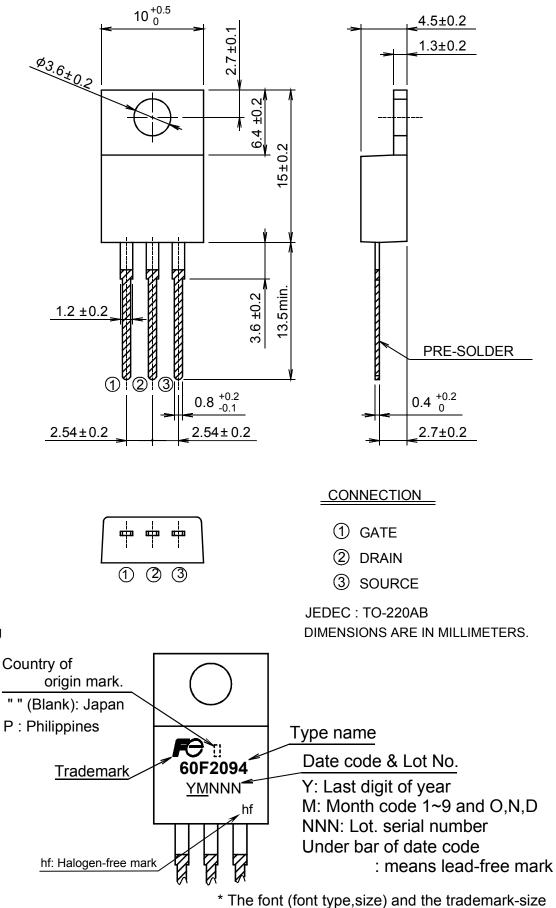


Fig.6 Reverse recovery Test circuit

Fig.7 Operating waveform of Reverse recovery Test

Outview: TO-220 Package

Marking



might be actually different.

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