

MOSFETs Silicon N-Channel MOS (DTMOSIV)

TK17V65W

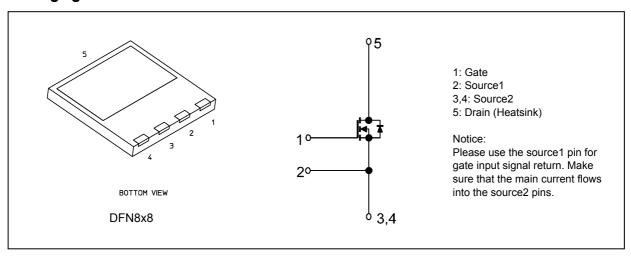
1. Applications

· Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)}$ = 0.175 Ω (typ.) by using Super Junction Structure : DTMOS
- (2) Easy to control Gate switching
- (3) Enhancement mode: V_{th} = 2.5 to 3.5 V (V_{DS} = 10 V, I_{D} = 0.9 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Rating	Unit		
Drain-source voltage			V_{DSS}	650	V
Gate-source voltage			V _{GSS}	±30	
Drain current (DC)		(Note 1)	I _D	17.3	Α
Drain current (pulsed)		(Note 1)	I _{DP}	69.2	
Power dissipation ((T _c = 25 °C)		P _D	156	W
Single-pulse avalanche energy		(Note 2)	E _{AS}	210	mJ
Avalanche current			I _{AR}	4.4	Α
Reverse drain current (DC)		(Note 1)	I_{DR}	17.3	
Reverse drain current (pulsed)		(Note 1)	I _{DRP}	69.2	
Channel temperature			T _{ch}	150	°C
Storage temperature			T _{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production



5. Thermal Characteristics

Characteristics		Max	Unit
Channel-to-case thermal resistance	R _{th(ch-c)}	0.8	°C/W

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: V_{DD} = 90 V, T_{ch} = 25 °C (initial), L = 19.2 mH, R_G = 25 Ω , I_{AR} = 4.4 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μΑ
Drain cut-off current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V	_	_	10	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	650	_	_	V
Gate threshold voltage	V _{th}	V _{DS} = 10 V, I _D = 0.9 mA	2.5	_	3.5	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 8.7 A	_	0.175	0.21	Ω

6.2. Dynamic Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 300 V, V _{GS} = 0 V, f = 1 MHz	_	1800	_	pF
Reverse transfer capacitance	C _{rss}		_	7	_	
Output capacitance	C _{oss}		_	40	_	
Effective output capacitance	C _{o(er)}	V _{DS} = 0 to 400 V, V _{GS} = 0 V	_	65	_	
Gate resistance	r _g	V _{DS} = OPEN , f = 1 MHz	_	1.5	_	Ω
Switching time (rise time)	t _r	See Figure 6.2.1	_	15	_	ns
Switching time (turn-on time)	t _{on}		_	50	_	
Switching time (fall time)	t _f		_	6	_	
Switching time (turn-off time)	t _{off}		_	100	_	
MOSFET dv/dt ruggedness	dv/dt	V _{DD} = 0 to 400 V, I _D = 8.7 A	50	_	_	V/ns

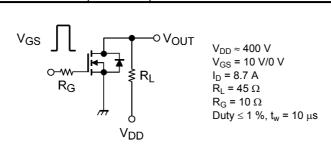


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 17.3 \text{ A}$		45		nC
Gate-source charge 1	Q _{gs1}			11		
Gate-drain charge	Q_{gd}		_	20		

6.4. Source-Drain Characteristics ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	V_{DSF}	I _{DR} = 17.3 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 8.7 A, V _{GS} = 0 V	_	300	_	ns
Reverse recovery charge	Q_{rr}	-dI _{DR} /dt = 50 A/μs	_	2.7	_	μС
Peak reverse recovery current	I _{rr}		_	16	_	Α
Diode dv/dt ruggedness	dv/dt	I _{DR} = 8.7 A, V _{GS} = 0 V, V _{DD} = 400 V	15	_	_	V/ns



7. Marking

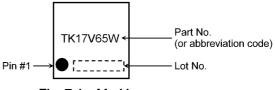


Fig. 7.1 Marking

8. Characteristics Curves (Note)

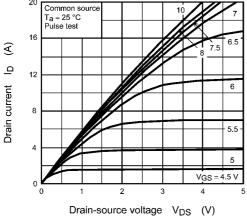
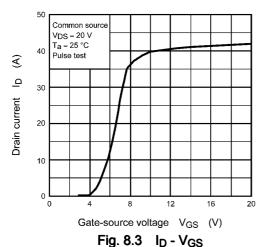


Fig. 8.1 I_D - V_{DS}



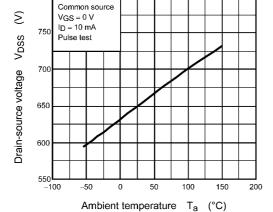


Fig. 8.5 V_{DSS} - T_a

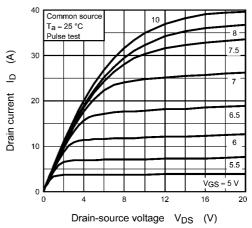


Fig. 8.2 I_D - V_{DS}

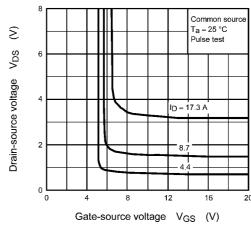


Fig. 8.4 V_{DS} - V_{GS}

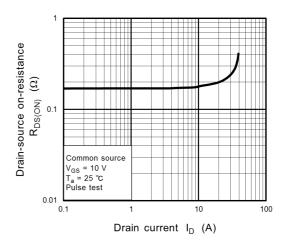


Fig. 8.6 $R_{DS(ON)}$ - I_D

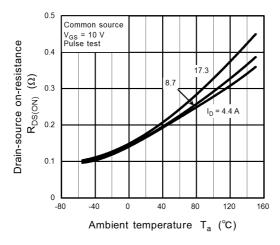


Fig. 8.7 RDS(ON) - Ta

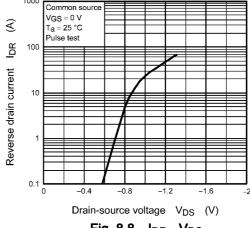


Fig. 8.8 I_{DR} - V_{DS}

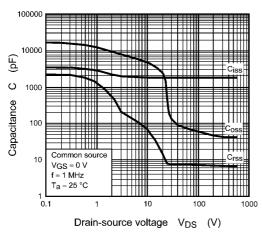


Fig. 8.9 C - V_{DS}

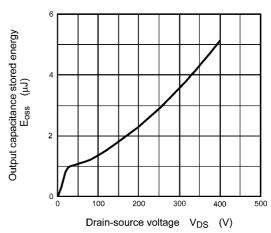


Fig. 8.10 E_{oss} - V_{DS}

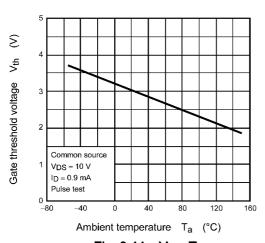


Fig. 8.11 V_{th} - T_a

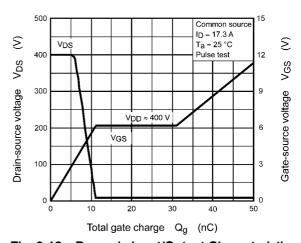


Fig. 8.12 Dynamic Input/Output Characteristics

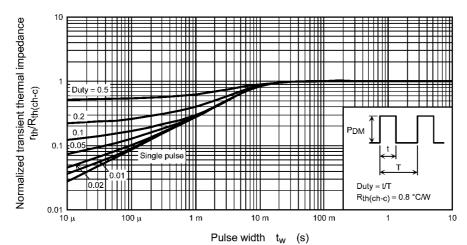


Fig. 8.13 r_{th} - t_w (Guaranteed Maximum)

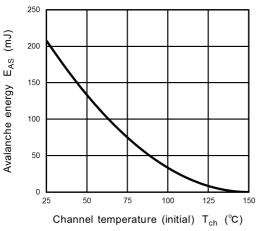


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)

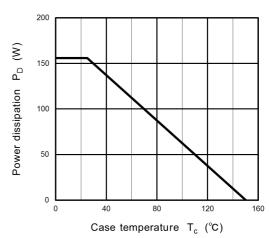


Fig. 8.15 P_D - T_c (Guaranteed Maximum)

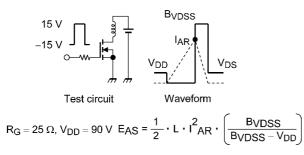


Fig. 8.16 Test Circuit/Waveform

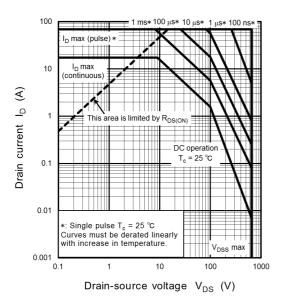


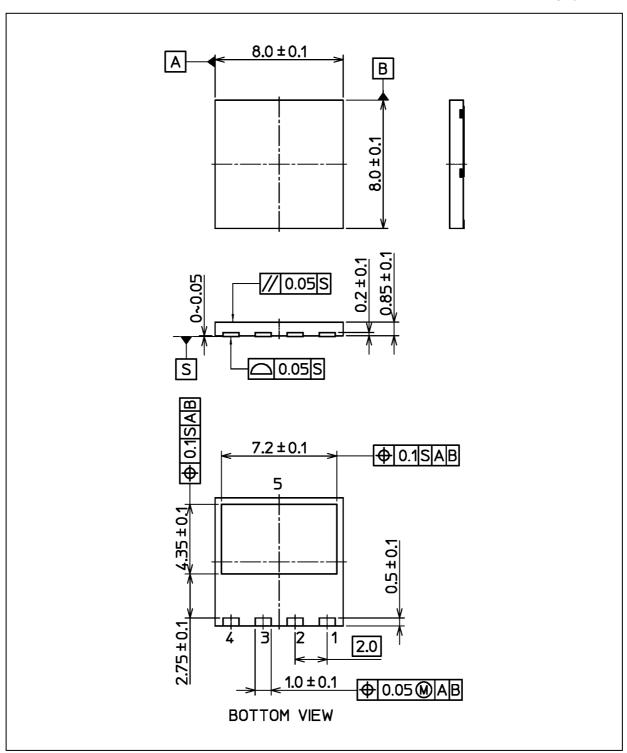
Fig. 8.17 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 0.175 g (typ.)

	Package Name(s)
TOSHIBA: 2-8T1A	
Nickname: DFN8x8	



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