

## N-channel 600 V, 0.28 $\Omega$ typ., 12 A MDmesh™ M2 Power MOSFET in TO-220 and IPAK packages

Datasheet - production data

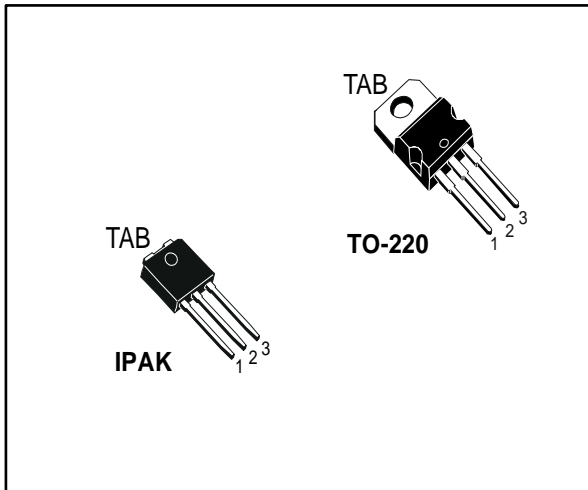
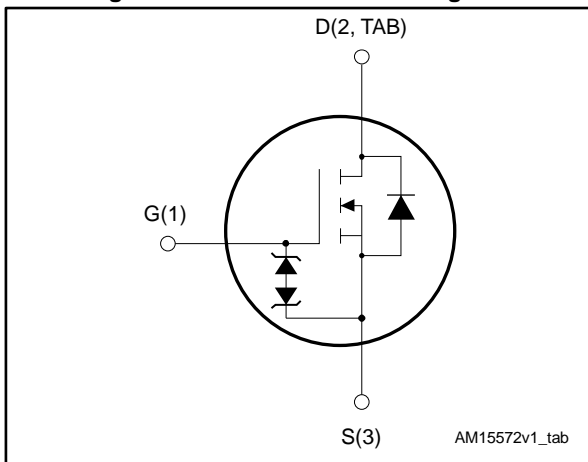


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STP16N60M2	600 V	0.32 $\Omega$	12 A
STU16N60M2			

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP16N60M2	16N60M2	TO-220	Tube
STU16N60M2		IPAK	

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	12	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	7.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

**Notes:**

(1) Pulse width limited by safe operating area.

(2)  $I_{SD} \leq 12\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

(3)  $V_{DS} \leq 480\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value		Unit
		TO-220	IPAK	
$R_{thj\text{-case}}$	Thermal resistance junction-case max.	1.14		$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient max.	62.5	100	$^\circ\text{C}/\text{W}$

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2.9	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	130	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified).

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 6\text{ A}$		0.28	0.32	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	700	-	pF
$C_{oss}$	Output capacitance		-	38	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	140	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 12\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17: "Gate charge test circuit"</a> )	-	19	-	nC
$Q_{gs}$	Gate-source charge		-	3.3	-	nC
$Q_{gd}$	Gate-drain charge		-	9.5	-	nC

**Notes:**

<sup>(1)</sup>  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 6\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 21: "Switching time waveform"</a> )	-	10.5	-	ns
$t_r$	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	58	-	ns
$t_f$	Fall time		-	18.5	-	ns

Table 8: Source-drain diode

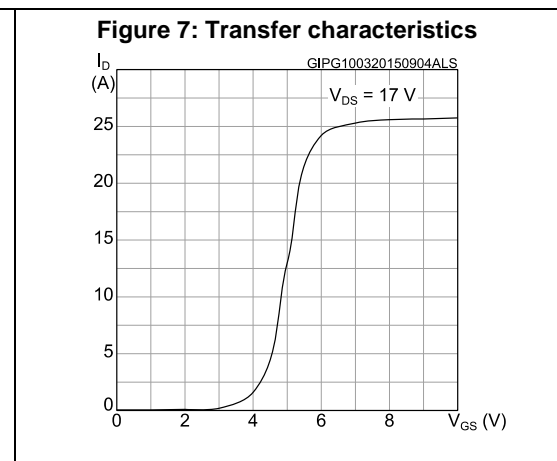
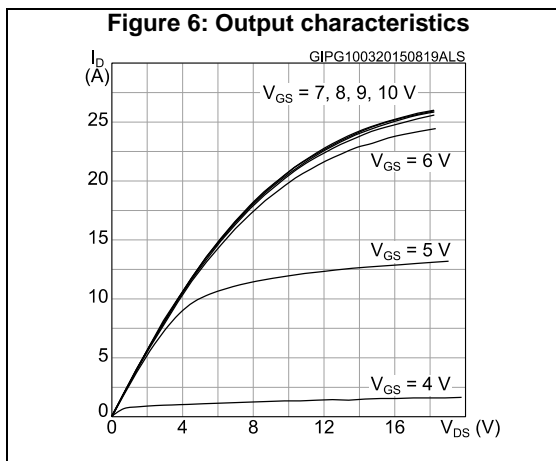
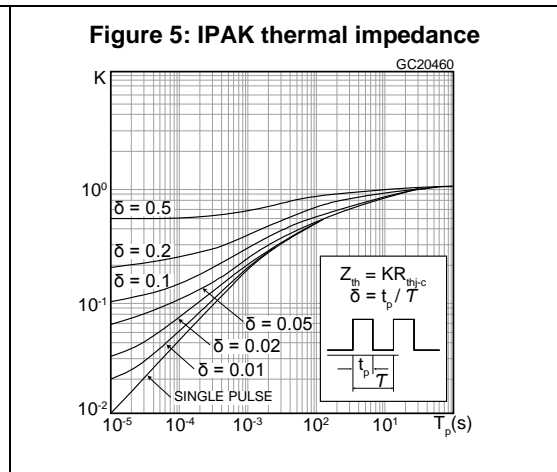
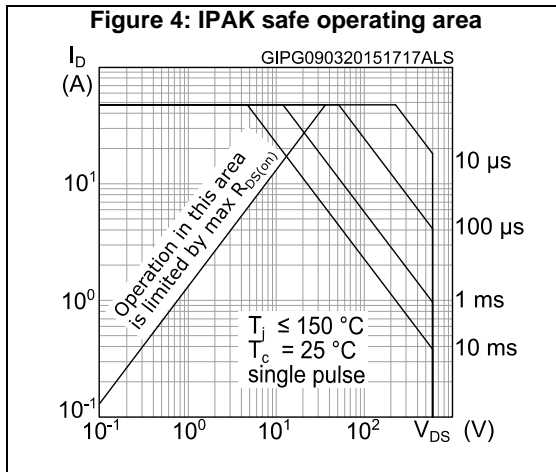
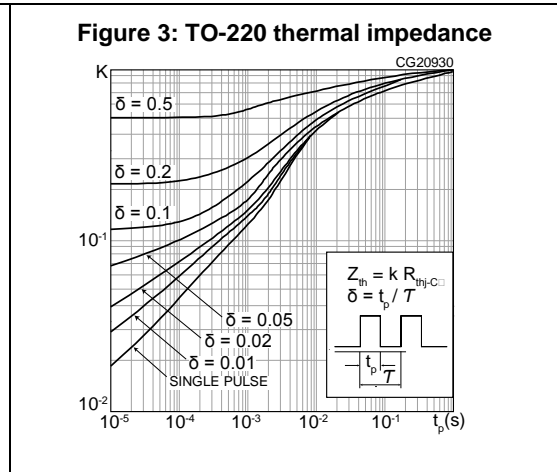
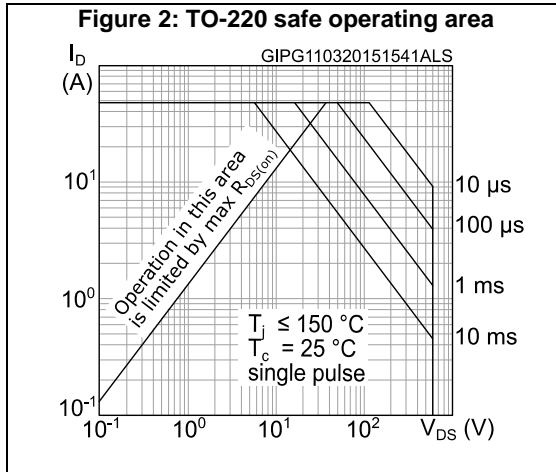
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 12\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 18</a> : "Test circuit for inductive load switching and diode recovery times")	-	316		ns
$Q_{rr}$	Reverse recovery charge		-	3.25		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> : "Test circuit for inductive load switching and diode recovery times")	-	454		ns
$Q_{rr}$	Reverse recovery charge		-	4.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	21		A

**Notes:**

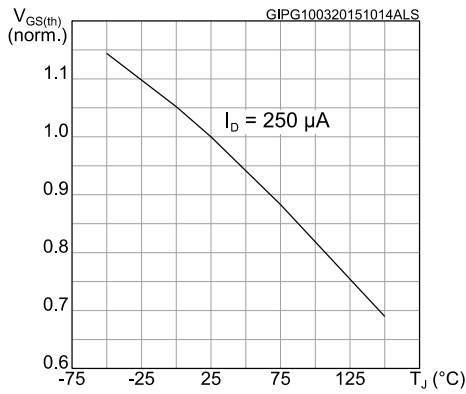
<sup>(1)</sup>Pulse width is limited by safe operating area.

<sup>(2)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

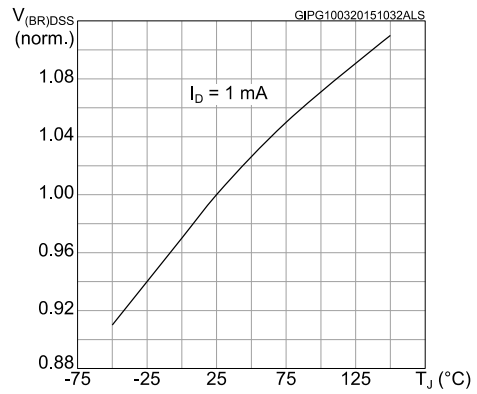
## 2.1 Electrical characteristics (curves)



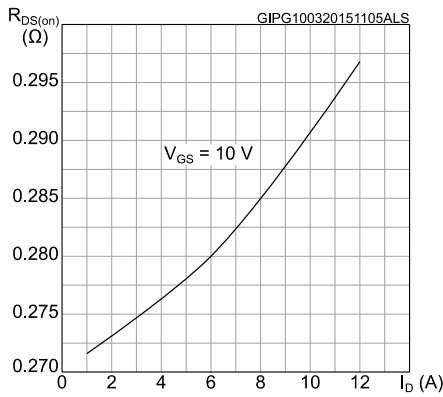
**Figure 8: Normalized gate threshold voltage vs. temperature**



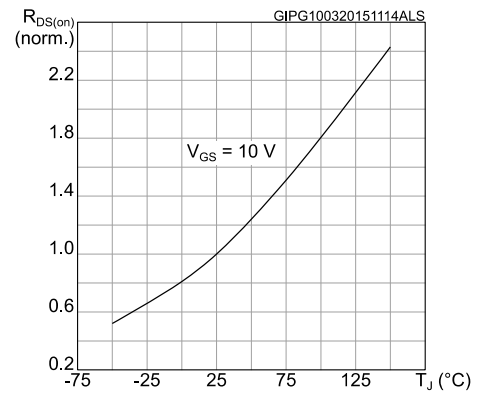
**Figure 9: Normalized  $V_{(BR)DSS}$  vs. temperature**



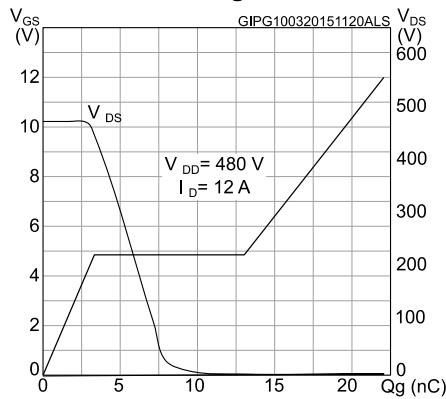
**Figure 10: Static drain-source on-resistance**



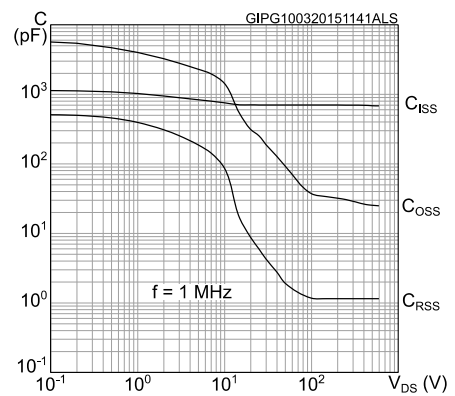
**Figure 11: Normalized on-resistance vs. temperature**



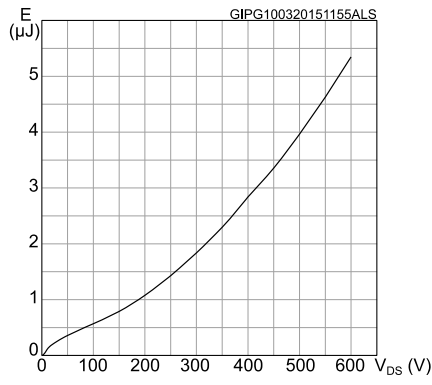
**Figure 12: Gate charge vs. gate-source voltage**



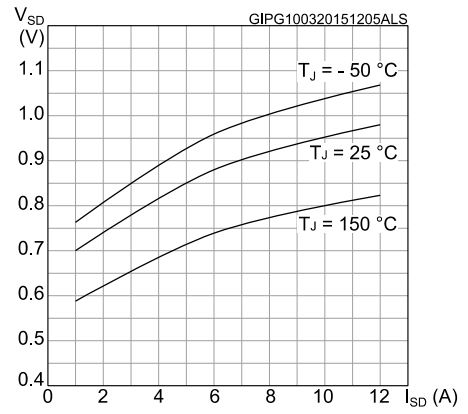
**Figure 13: Capacitance variations**



**Figure 14: Output capacitance stored energy**

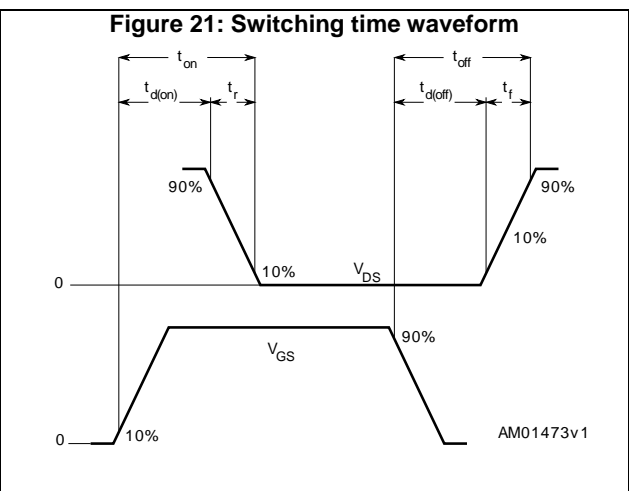
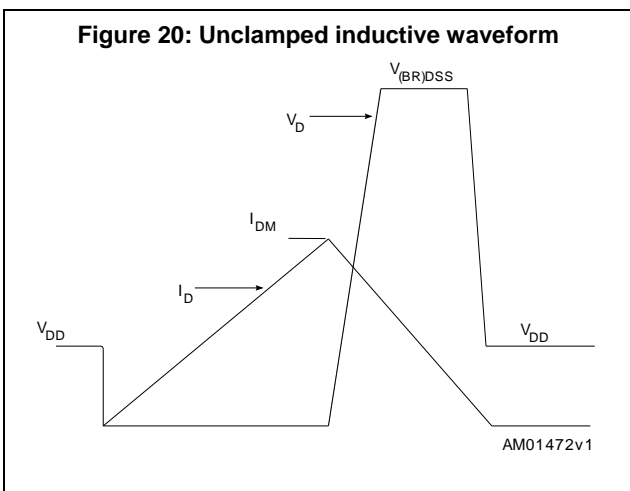
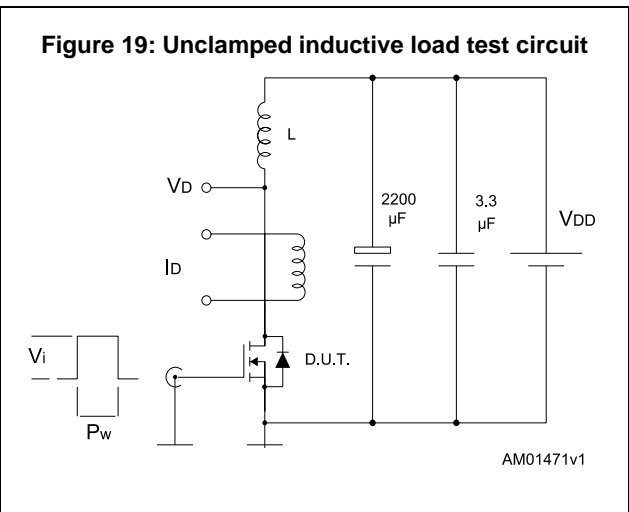
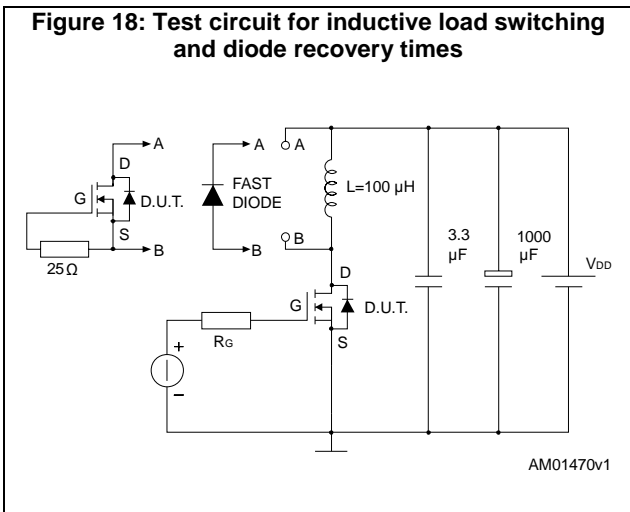
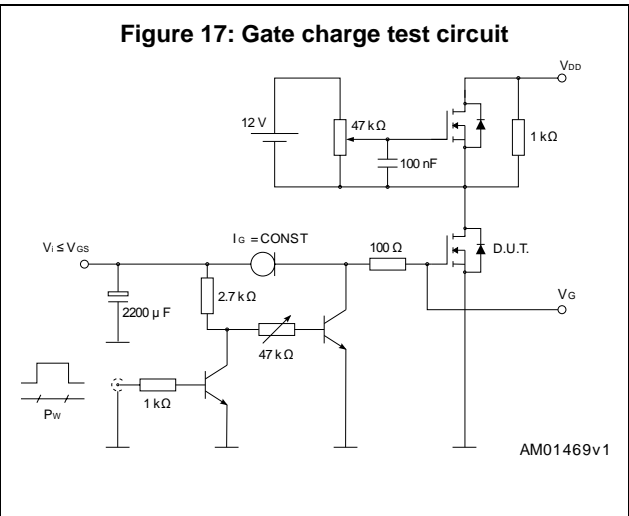
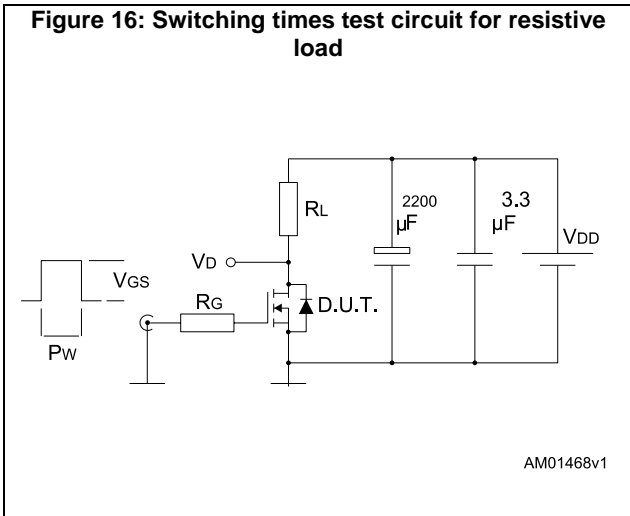


**Figure 15: Source-drain diode forward characteristics**





### 3 Test circuits



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 TO-220 type A package information

Figure 22: TO-220 type A package outline

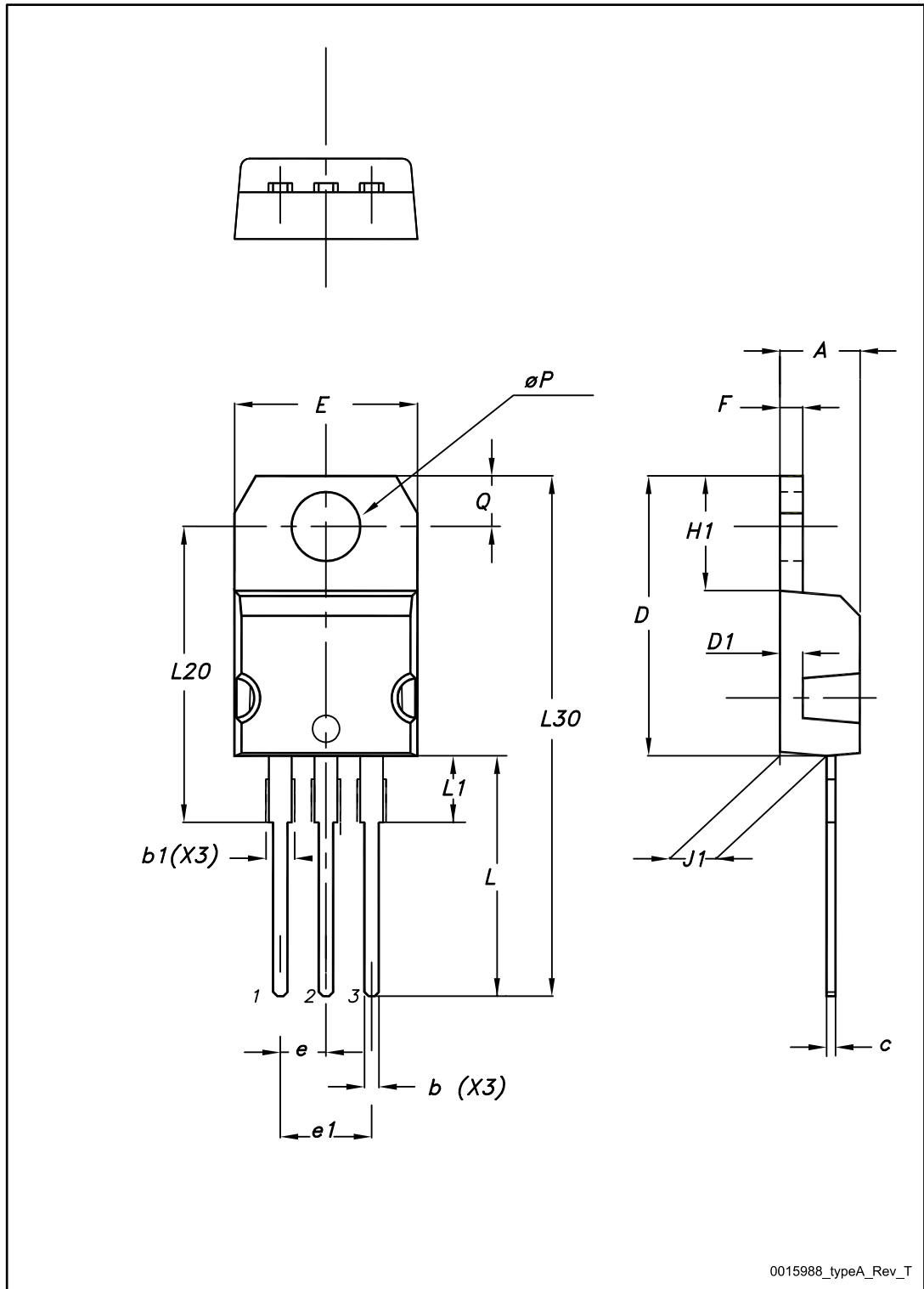


Table 9: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

### 4.2 IPAK (TO-251) Type A package information

Figure 23: IPAK (TO-251) type A drawing

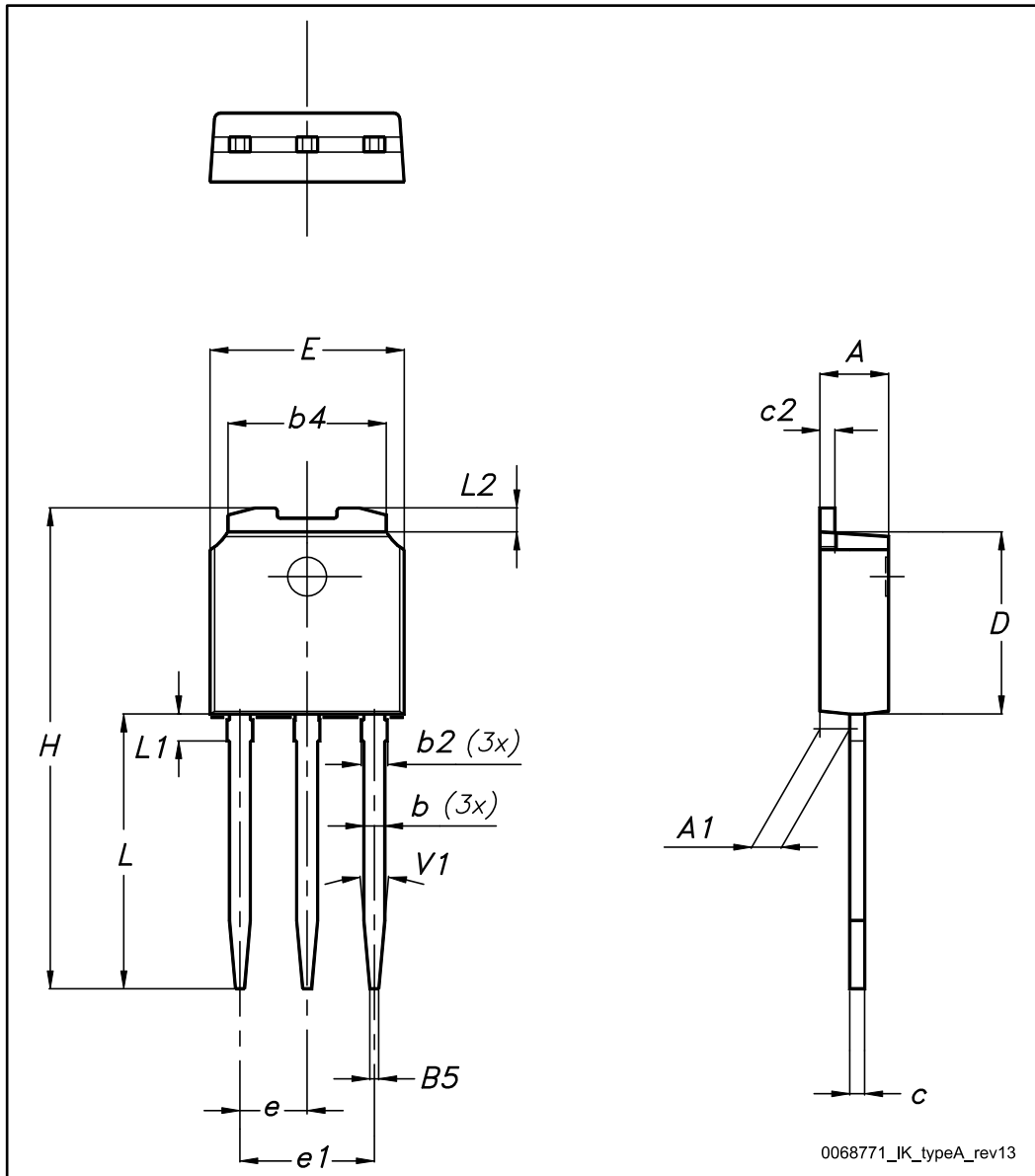


Table 10: IPAK (TO-251) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
11-Mar-2015	1	Initial release.

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