

## E Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	700
$R_{DS(on)}$ typ. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V   0.041
$Q_g$ max. (nC)	371
$Q_{gs}$ (nC)	65
$Q_{gd}$ (nC)	93
Configuration	Single

### FEATURES

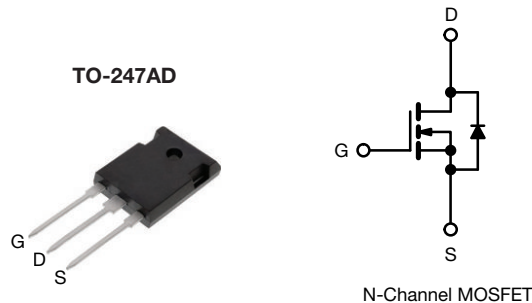
- Fast body diode MOSFET using E series technology
- Reduced  $t_{rr}$ ,  $Q_{rr}$ , and  $I_{RRM}$
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Low switching losses due to reduced  $Q_{rr}$
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Telecommunications
  - Server and telecom power supplies
- Lighting
  - High-intensity lighting (HID)
  - Light emitting diodes (LEDs)
- Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switching mode power supplies (SMPS)
  - Applications using the following topologies
    - LLC
    - Phase shifted bridge (ZVS)
    - 3-level inverter
    - AC/DC bridge



ORDERING INFORMATION	
Package	TO-247AD
Lead (Pb)-Free and Halogen-Free	SiHW61N65EF-GE3


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	199	
Linear Derating Factor		4.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	1142	mJ
Maximum Power Dissipation	$P_D$	520	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	$T_J = 125$ °C	V/ns
Reverse Diode dV/dt <sup>d</sup>		50	
Soldering Recommendations (Peak temperature) <sup>c</sup>	For 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 9$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 500$  A/ $\mu$ s, starting  $T_J = 25$  °C.



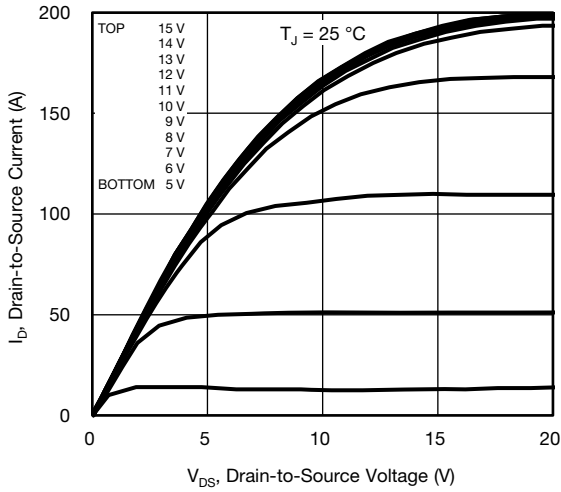
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.24	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 10\text{ mA}$	-	0.81	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30.5\text{ A}$	-	0.041	0.047	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 30.5\text{ A}$	-	23	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	7407	-	pF
Output Capacitance	$C_{oss}$		-	351	-	
Reverse Transfer Capacitance	$C_{rss}$		-	3	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$	-	233	-	pF
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$		-	939	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 30.5\text{ A}, V_{DS} = 520\text{ V}$	-	247	371	nC
Gate-Source Charge	$Q_{gs}$		-	65	-	
Gate-Drain Charge	$Q_{gd}$		-	93	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 30.5\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$	-	59	89	ns
Rise Time	$t_r$		-	107	161	
Turn-Off Delay Time	$t_{d(off)}$		-	217	326	
Fall Time	$t_f$		-	133	200	
Gate Input Resistance	$R_g$		$f = 1\text{ MHz}, \text{open drain}$	0.5	1	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	64	A
Pulsed Diode Forward Current	$I_{SM}$		-	-	199	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 30.5\text{ A}, V_{GS} = 0\text{ V}$	-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 30.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$	-	212	474	ns
Reverse Recovery Charge	$Q_{rr}$		-	2.1	3.8	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$		-	18	-	A

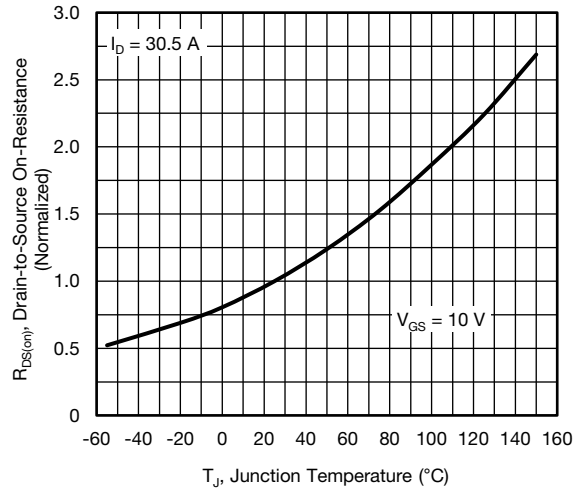
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .
- b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

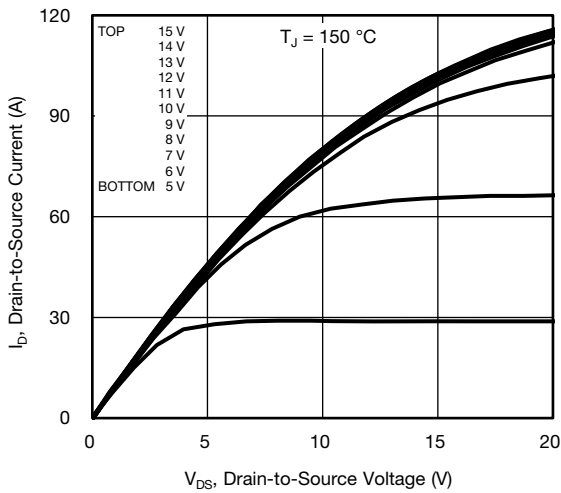
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



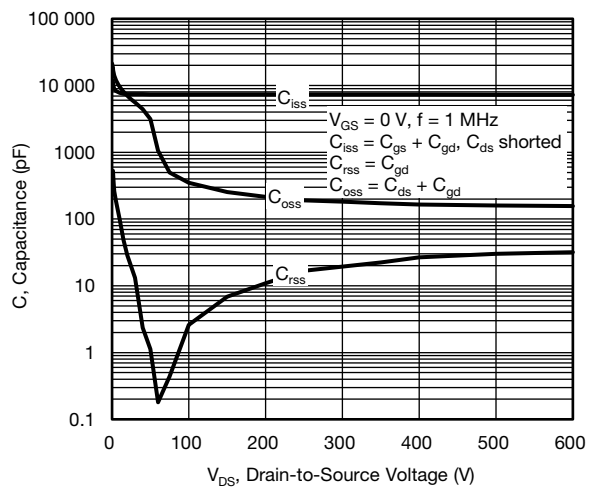
**Fig. 1 - Typical Output Characteristics**



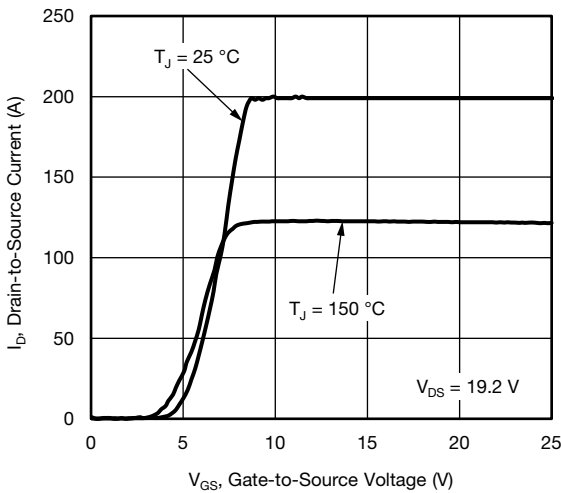
**Fig. 4 - Normalized On-Resistance vs. Temperature**



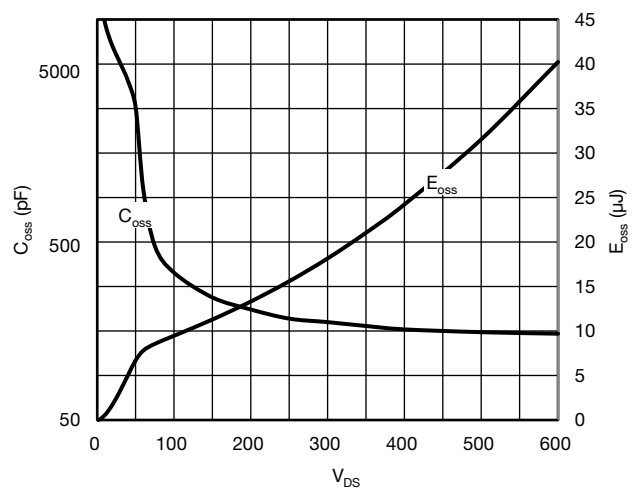
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

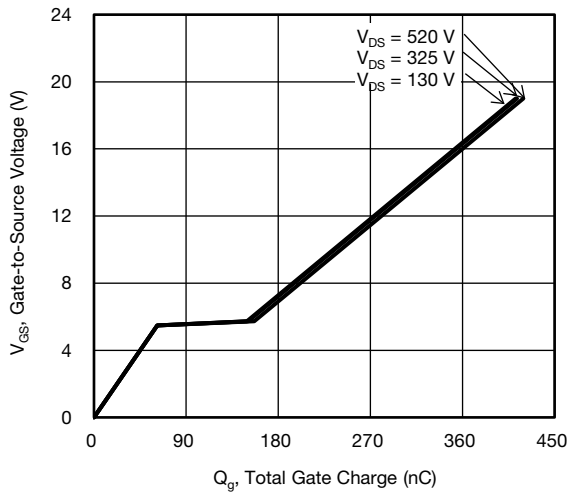


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

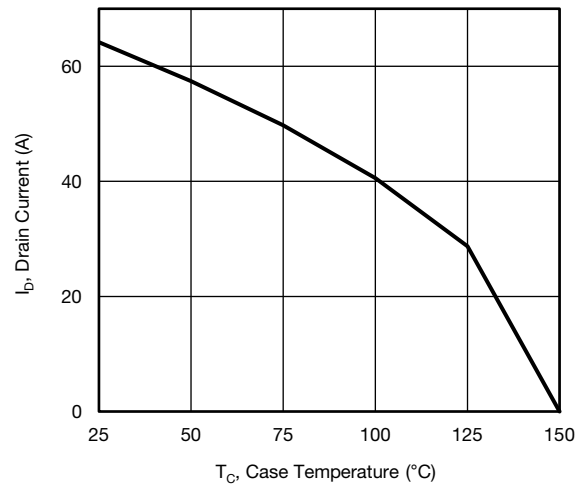


Fig. 10 - Maximum Drain Current vs. Case Temperature

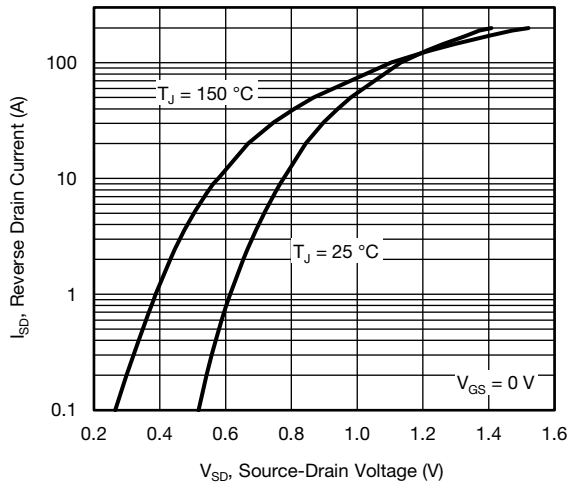


Fig. 8 - Typical Source-Drain Diode Forward Voltage

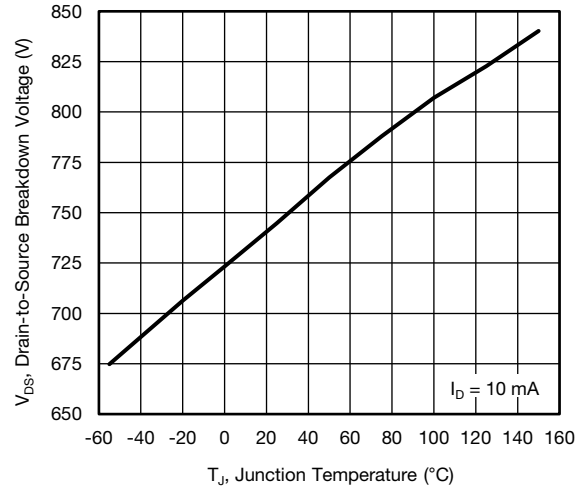


Fig. 11 - Temperature vs. Drain-to-Source Voltage

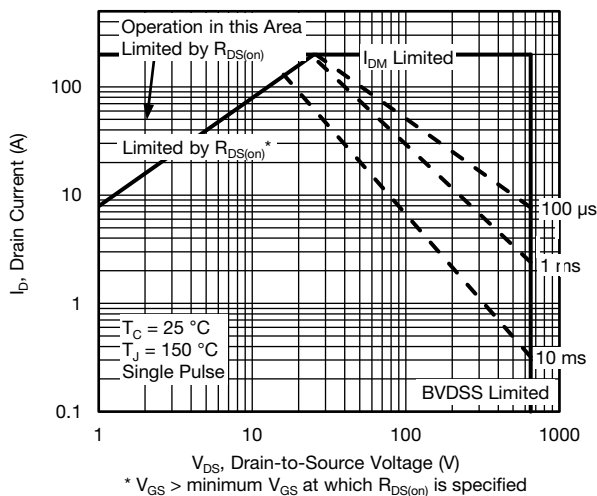


Fig. 9 - Maximum Safe Operating Area

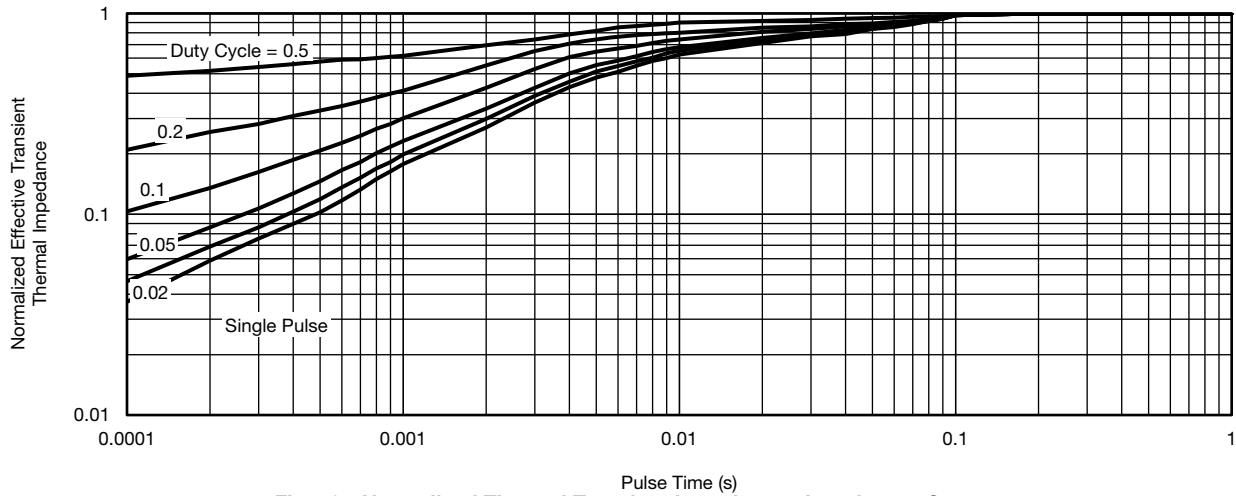


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

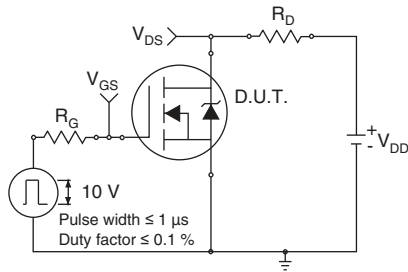


Fig. 13 - Switching Time Test Circuit

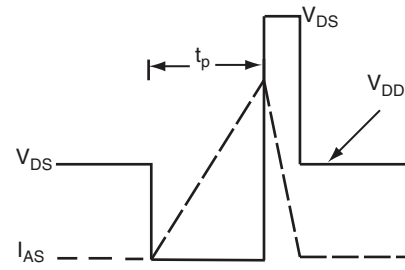


Fig. 16 - Unclamped Inductive Waveforms

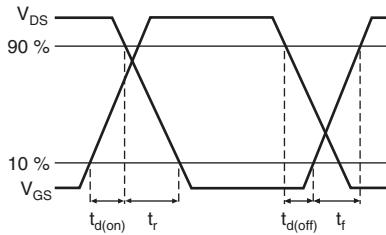


Fig. 14 - Switching Time Waveforms

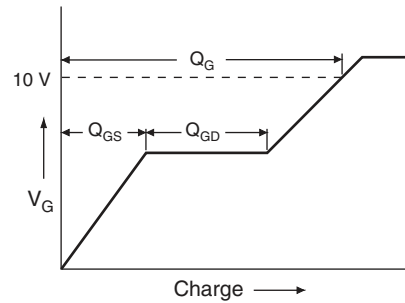


Fig. 17 - Basic Gate Charge Waveform

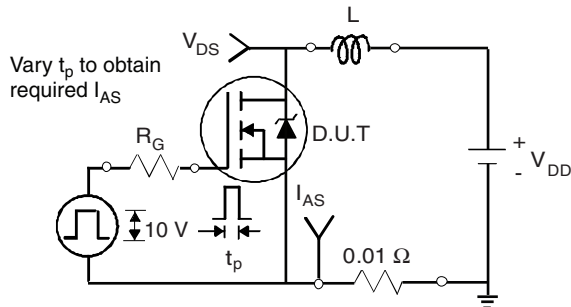


Fig. 15 - Unclamped Inductive Test Circuit

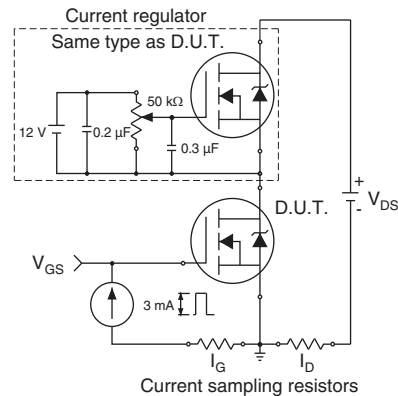


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 19 - For N-Channel

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## TO-247AD (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.31	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.41	0.065	0.095
b4	2.59	3.43	0.102	0.135
c	0.61 BSC		0.024 BSC	
D	20.80	21.46	0.819	0.845
D1	3.68	5.49	0.145	0.216
(e)	5.46 BSC		0.215 BSC	
E	15.49	16.26	0.610	0.640
L	19.81	20.32	0.780	0.800
L1	4.06	4.50	0.160	0.177
Ø p	3.51	3.66	0.138	0.144
ECN: S17-0178-Rev. B, 06-Feb-17				
DWG: 6010				



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