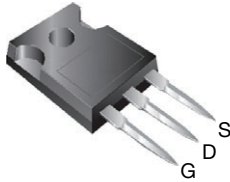


EF Series Power MOSFET With Fast Body Diode

TO-247AC



N-Channel MOSFET

FEATURES

- A specific on resistance ($m\Omega\text{-cm}^2$) reduction of 25 %
- Low figure-of-merit (FOM) $R_{\text{on}} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{\text{DS(on)}}$ typ. (Ω) at 25 °C	$V_{\text{GS}} = 10 \text{ V}$	0.084
Q_g max. (nC)	134	
Q_{gs} (nC)	16	
Q_{gd} (nC)	48	
Configuration	Single	

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free and halogen-free	SiHG35N60EF-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25 \text{ }^\circ\text{C}$, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	600	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150 \text{ }^\circ\text{C}$)	V_{GS} at 10 V	$T_C = 25 \text{ }^\circ\text{C}$	A
		$T_C = 100 \text{ }^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	80	
Linear derating factor		2.0	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	298	mJ
Maximum power dissipation	P_{D}	250	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Drain-source voltage slope	dv/dt	$T_J = 125 \text{ }^\circ\text{C}$	V/ns
Reverse diode dv/dt ^d			
Soldering recommendations (peak temperature) ^c	For 10 s	260	$^\circ\text{C}$

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{\text{DD}} = 140 \text{ V}$, starting $T_J = 25 \text{ }^\circ\text{C}$, $L = 28.2 \text{ mH}$, $R_g = 25 \text{ } \Omega$, $I_{\text{AS}} = 4.6 \text{ A}$
- 1.6 mm from case
- $I_{\text{SD}} = 17 \text{ A}$, $di/dt = 300 \text{ A}/\mu\text{s}$, starting $T_J = 25 \text{ }^\circ\text{C}$



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	0.5	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 10 mA		-	0.66	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 480 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 17 A	-	0.084	0.097	Ω
Forward transconductance ^a	g _{fs}	V _{DS} = 30 V, I _D = 17 A		-	8	-	S
Dynamic							
Input capacitance	C _{iSS}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	2568	-	pF
Output capacitance	C _{oss}			-	113	-	
Reverse transfer capacitance	C _{rSS}			-	7	-	
Effective output capacitance, energy related ^a	C _{o(er)}			-	81	-	
Effective output capacitance, time related ^b	C _{o(tr)}	V _{DS} = 0 V to 480 V, V _{GS} = 0 V		-	421	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 17 A, V _{DS} = 480 V	-	89	134	nC
Gate-source charge	Q _{gs}			-	16	-	
Gate-drain charge	Q _{gd}			-	48	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 480 V, I _D = 17 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	28	56	ns
Rise time	t _r			-	85	170	
Turn-off delay time	t _{d(off)}			-	96	192	
Fall time	t _f			-	61	122	
Gate input resistance	R _g	f = 1 MHz, open drain		0.2	0.5	1.0	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	32	A
Pulsed diode forward current	I _{SM}			-	-	80	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 17 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 17 A, di/dt = 100 A/μs, V _R = 400 V		-	150	300	ns
Reverse recovery charge	Q _{rr}			-	1.1	2.2	μC
Reverse recovery current	I _{RRM}			-	14	-	A

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

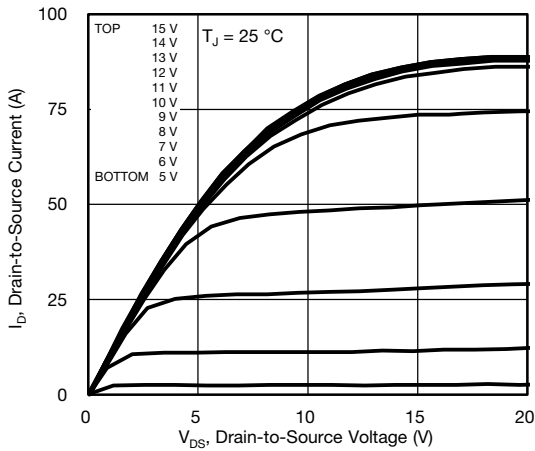


Fig. 1 - Typical Output Characteristics

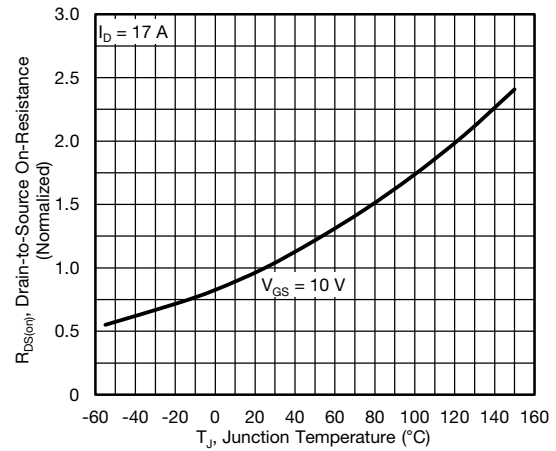


Fig. 4 - Normalized On-Resistance vs. Temperature

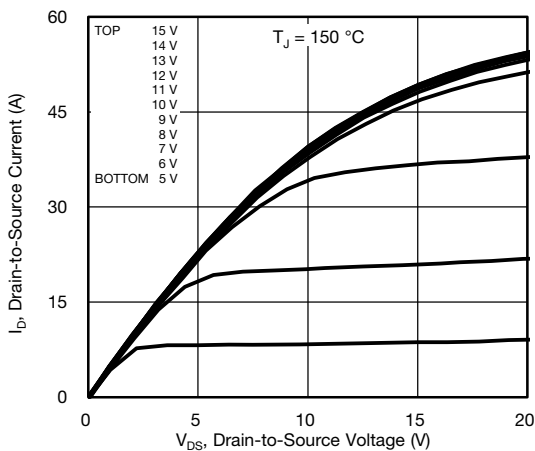


Fig. 2 - Typical Output Characteristics

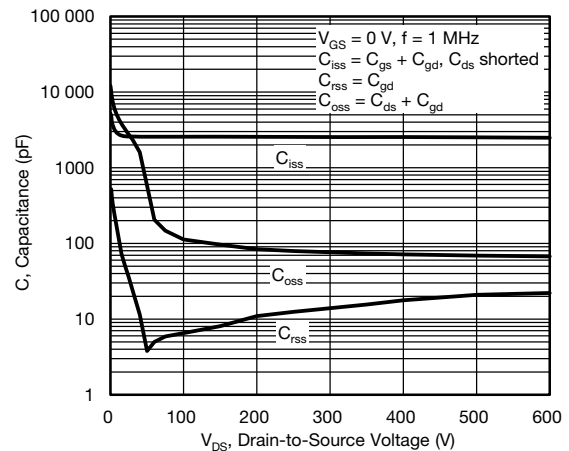


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

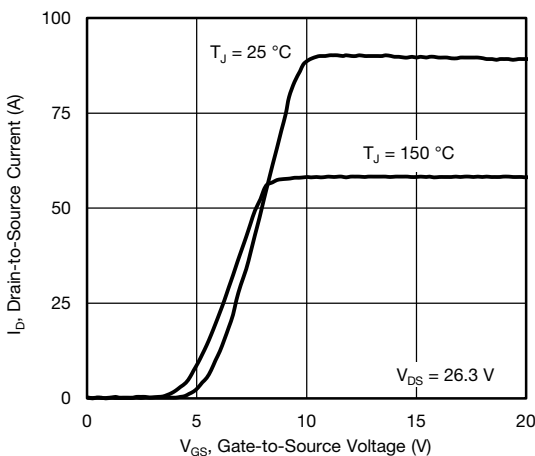


Fig. 3 - Typical Transfer Characteristics

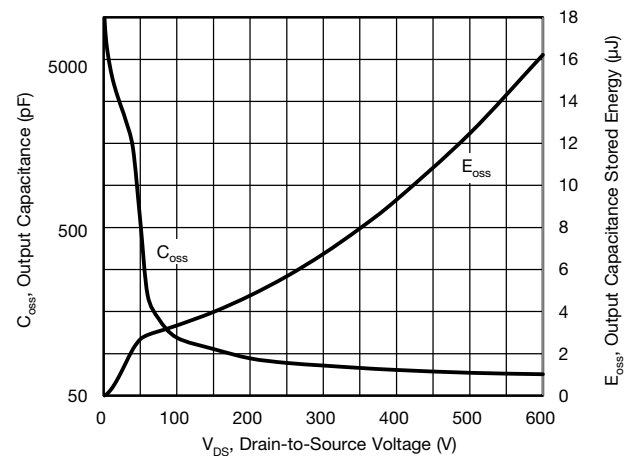


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

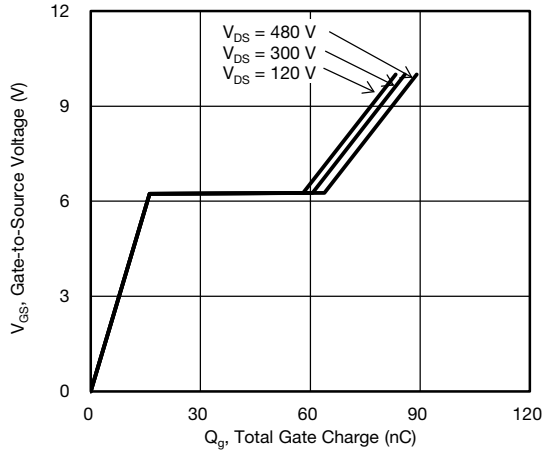


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

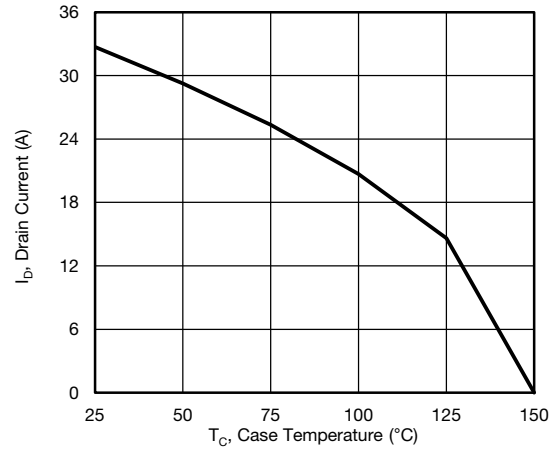


Fig. 10 - Maximum Drain Current vs. Case Temperature

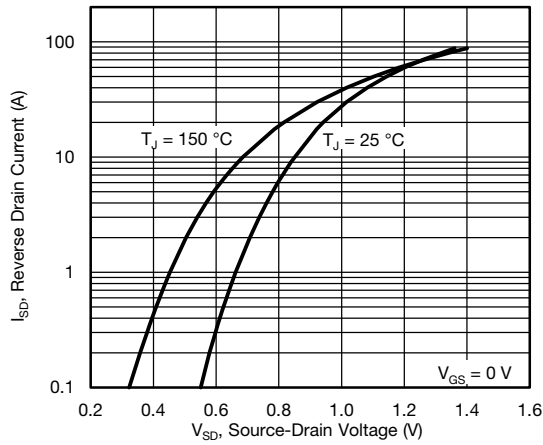


Fig. 8 - Typical Source-Drain Diode Forward Voltage

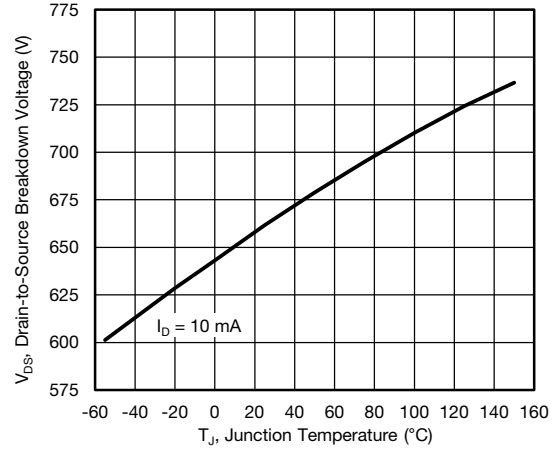


Fig. 11 - Temperature vs. Drain-to-Source Voltage

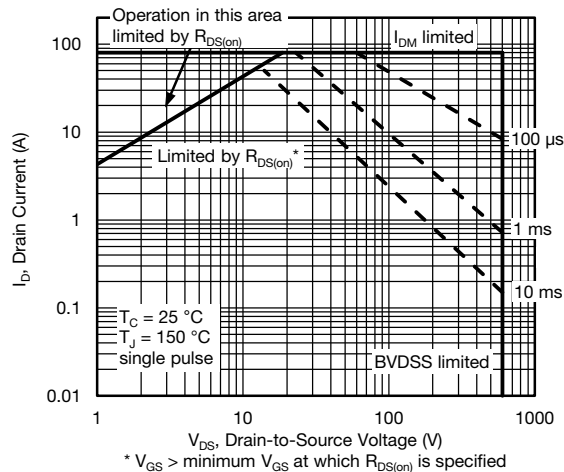


Fig. 9 - Maximum Safe Operating Area

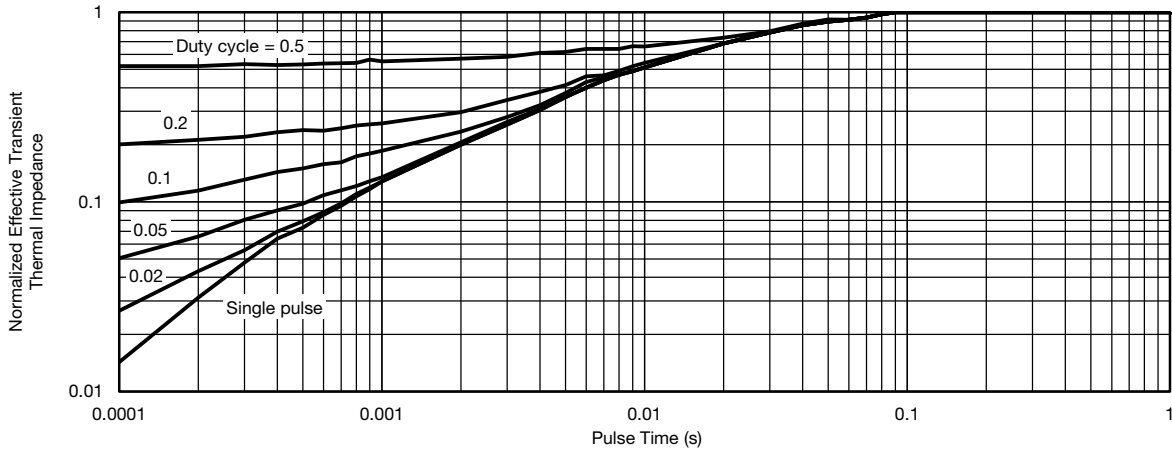


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit



Fig. 16 - Unclamped Inductive Waveforms

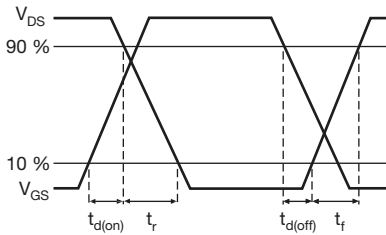


Fig. 14 - Switching Time Waveforms

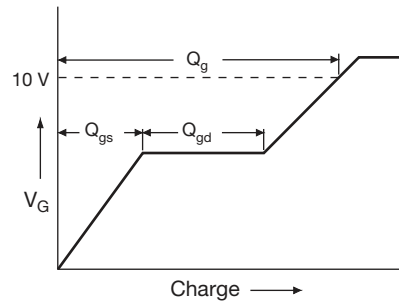


Fig. 17 - Basic Gate Charge Waveform



Fig. 15 - Unclamped Inductive Test Circuit

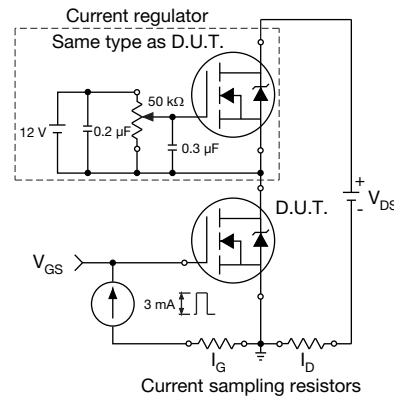


Fig. 18 - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon

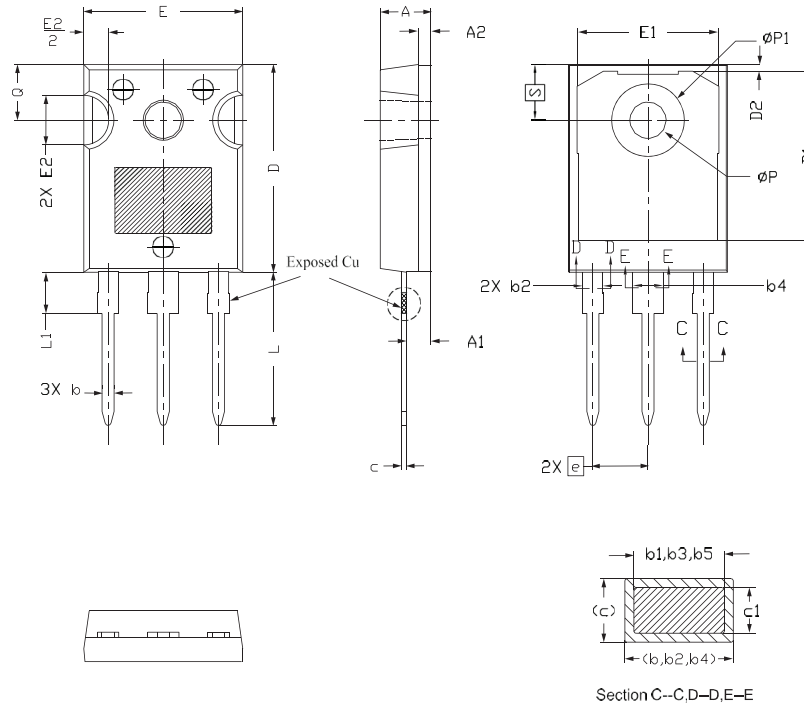


Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?92109.



TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



DIM.	MILLIMETERS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

DIM.	MILLIMETERS			NOTES
	MIN.	NOM.	MAX.	
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



VERSION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
 DWG: 5971

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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