



USG40N10

Preliminary

POWER MOSFET

**48A, 100V N-CHANNEL
POWER MOSFET**

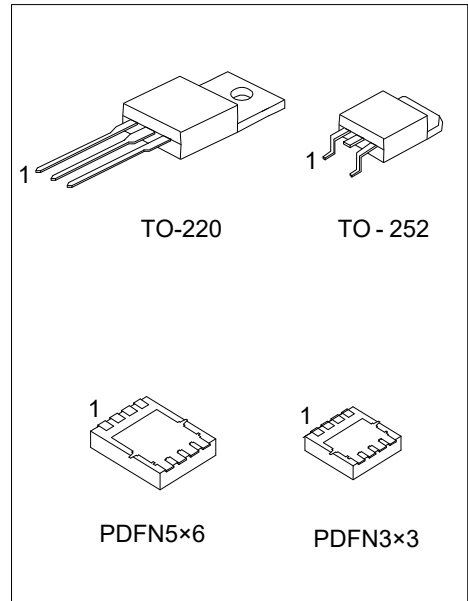
■ DESCRIPTION

The UTC **USG40N10** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

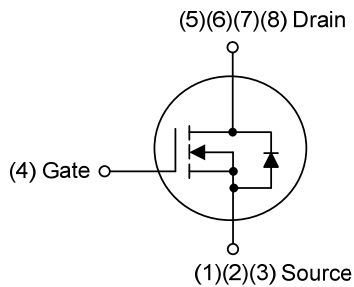
The UTC **USG40N10** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

■ FEATURES

- * $R_{DS(ON)} \leq 16 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=20\text{A}$
- $R_{DS(ON)} \leq 28 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=10\text{A}$
- * High Frequency Switching
- * Synchronous Rectification



■ SYMBOL



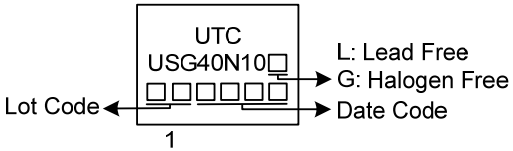
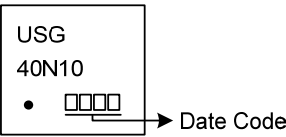
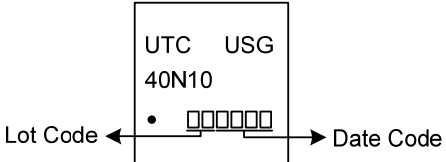
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
USG40N10L-TA3-T	USG40N10G-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
USG40N10L-TN3-R	USG40N10G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
USG40N10L-P3030-R	USG40N10G-P3030-R	PDFN3x3	S	S	S	G	D	D	D	D	Tape Reel
USG40N10L-P5060-R	USG40N10G-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>USG40N10G-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TN3: TO-252, P3030: PDFN3x3 P5060: PDFN5x6</p> <p>(3) G: Halogen Free and Lead Free L: Lead Free</p>
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MARKING

PACKAGE	MARKING
TO-220 / TO-252	 <p> UTC USG40N10 Lot Code → [][][][] → Date Code 1 L: Lead Free G: Halogen Free </p>
PDFN3x3	 <p> USG 40N10 • [][][][] → Date Code </p>
PDFN5x6	 <p> UTC USG 40N10 • [][][][][][] → Date Code Lot Code ← </p>

■ ABSOLUTE MAXIMUM RATING ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V_{DSS}	100	V	
Gate-Source Voltage		V_{GSS}	± 20	V	
Drain Current	Continuous	I_D	$T_C=25^\circ\text{C}$	48	A
			$T_C=100^\circ\text{C}$	28	A
	Pulsed (Note 2)		I_{DM}	80	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	20	mJ	
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.5	V/ns	
Power Dissipation	TO-220	P_D	80	W	
	TO-252		42	W	
	PDFN3×3		25	W	
	PDFN5×6		35	W	
Junction Temperature		T_J	+150	$^\circ\text{C}$	
Storage Temperature Range		T_{STG}	-20 ~ +150	$^\circ\text{C}$	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=20\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
	TO-252		110	$^\circ\text{C}/\text{W}$
	PDFN3×3		130	$^\circ\text{C}/\text{W}$
	PDFN5×6		65	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	1.56	$^\circ\text{C}/\text{W}$
	TO-252		2.97 (Note)	$^\circ\text{C}/\text{W}$
	PDFN3×3		5 (Note)	$^\circ\text{C}/\text{W}$
	PDFN5×6		3.57 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

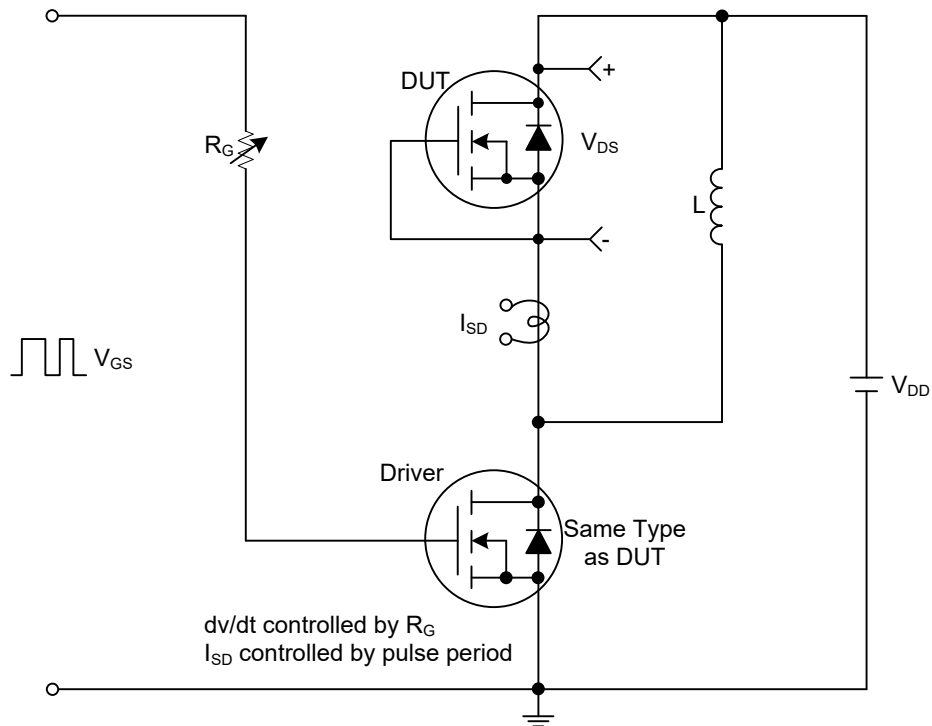
■ ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	100			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS} V _{GS} =+20V, V _{DS} =0V V _{GS} =-20V, V _{DS} =0V			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.8	2.5	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		14	16	mΩ
		V _{GS} =4.5V, I _D =10A		22	28	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		1212		pF
Output Capacitance	C _{OSS}			525		pF
Reverse Transfer Capacitance	C _{RSS}			58		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =80V, V _{GS} =10V, I _D =40A, (Note 1, 2)		32		nC
Gate to Source Charge	Q _{GS}			10		nC
Gate to Drain Charge	Q _{GD}			7		nC
Turn-on Delay Time (Note 1)	t _{D(ON)}	V _{DD} =50V, V _{GS} =10V, I _D =40A, R _G =3.3Ω (Note 1, 2)		8		ns
Rise Time	t _R			16		ns
Turn-off Delay Time	t _{D(OFF)}			23		ns
Fall-Time	t _F			17		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				48	A
Maximum Body-Diode Pulsed Current	I _{SM}				80	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =20A, V _{GS} =0V		0.88	1.2	V
Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V,		130		nS
Reverse Recovery Charge	Q _{rr}	dI _F /dt = 100A/μs		160		nC

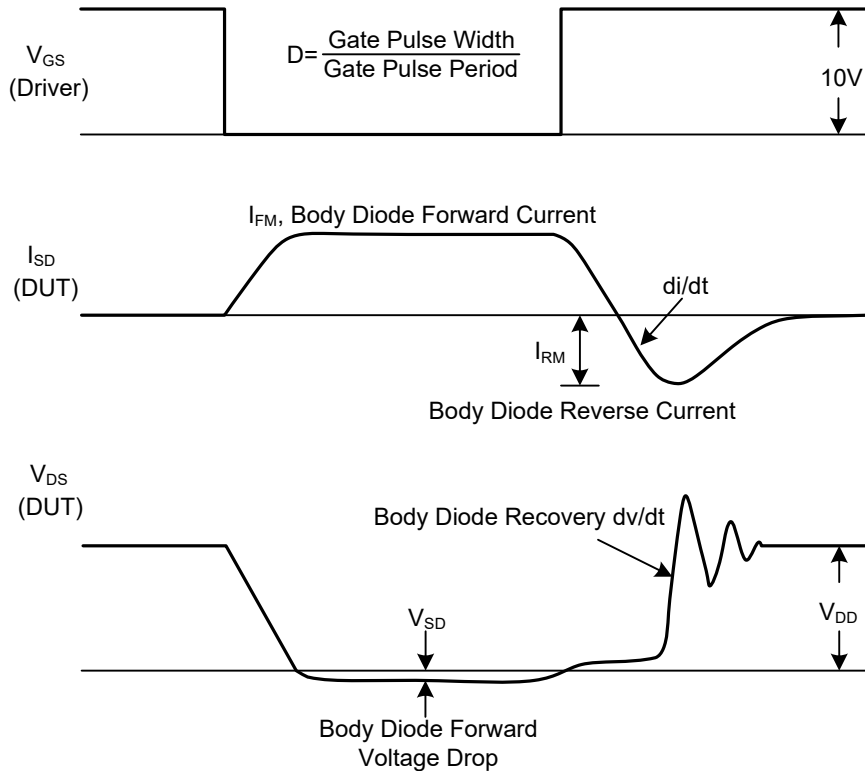
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



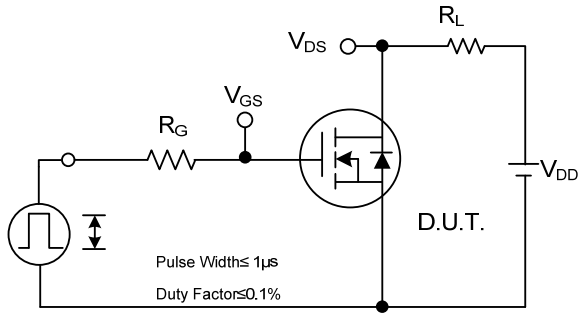
Peak Diode Recovery dv/dt Test Circuit



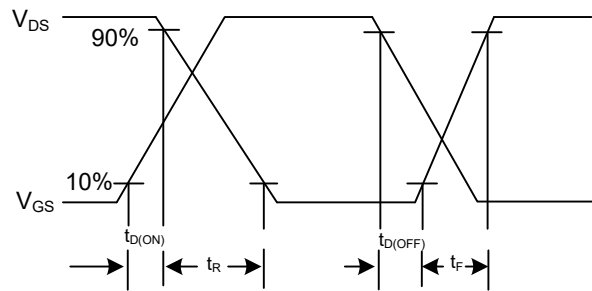
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

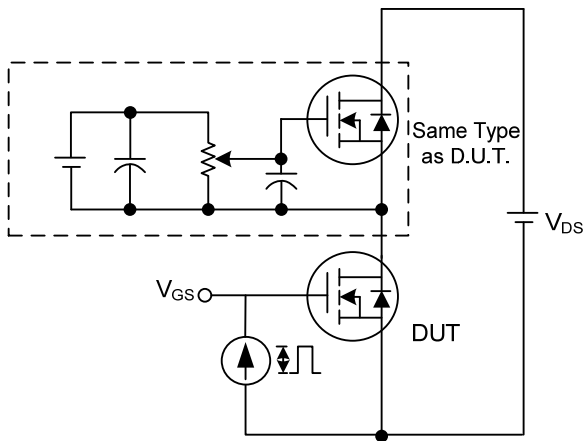
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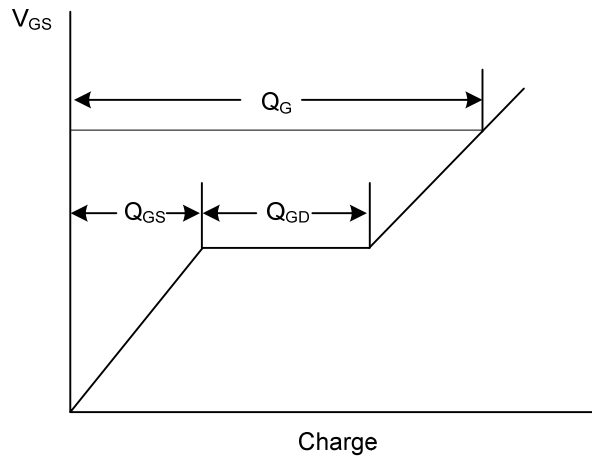
Switching Test Circuit



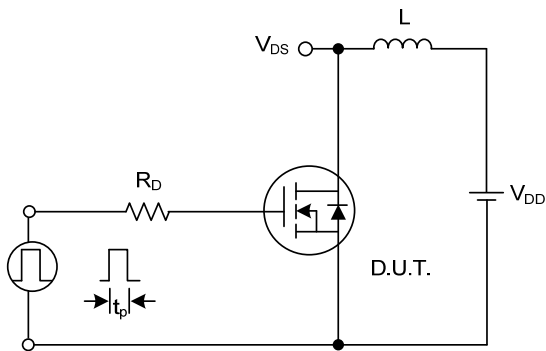
Switching Waveforms



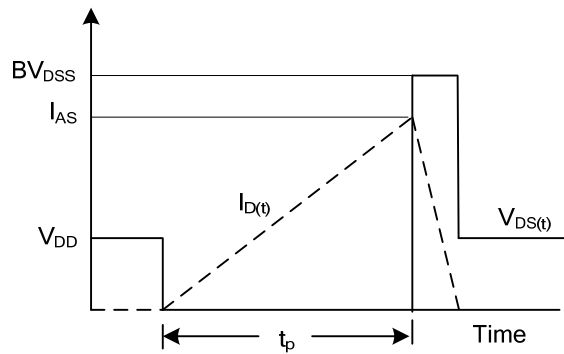
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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