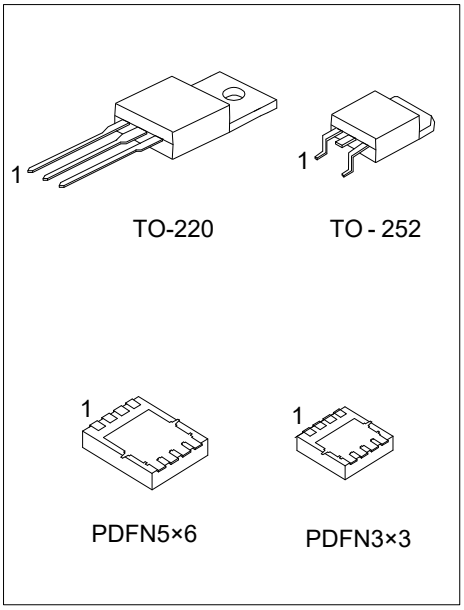
48A, 100V N-CHANNEL POWER MOSFET



■ DESCRIPTION

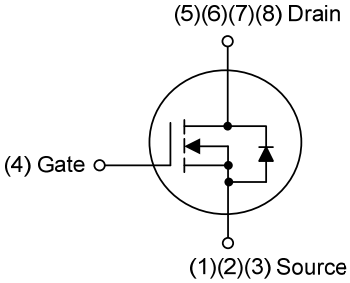
The UTC **USG40N10** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

The UTC **USG40N10** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

■ FEATURES

* $R_{DS(ON)}$ ≤ 16 mΩ @ V_{GS}=10V, I_D=20A
  $R_{DS(ON)}$ ≤ 28 mΩ @ V_{GS}=4.5V, I_D=10A
* High Frequency Switching
* Synchronous Rectification

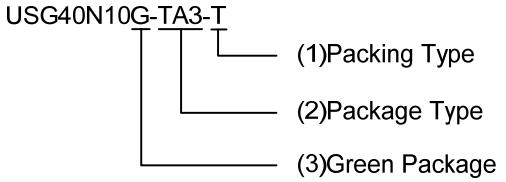
■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
USG40N10L-TA3-T	USG40N10G-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
USG40N10L-TN3-R	USG40N10G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
USG40N10L-P3030-R	USG40N10G-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel
USG40N10L-P5060-R	USG40N10G-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

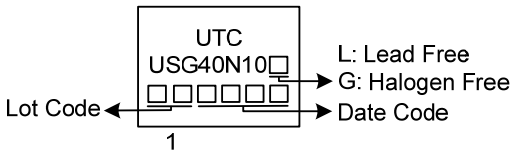
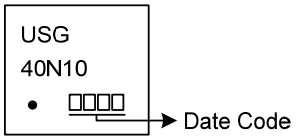
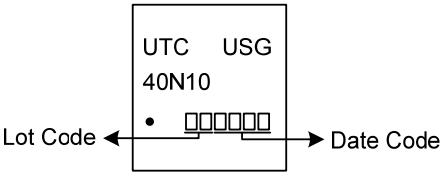


(1) T: Tube, R: Tape Reel

(2) TA3: TO-220, TN3: TO-252, P3030: PDFN3×3
P5060: PDFN5×6

(3) G: Halogen Free and Lead Free L: Lead Free

■ MARKING

PACKAGE	MARKING
TO-220 / TO-252	
PDFN3×3	
PDFN5×6	

■ ABSOLUTE MAXIMUM RATING (T_C=25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	100	V
Gate-Source Voltage			V_{GSS}	±20	V
Drain Current	Continuous	T_C=25°C	I_D	48	A
		T_C=100°C		28	A
	Pulsed (Note 2)		I_{DM}	80	A
Single Pulsed Avalanche Energy (Note 3)			E_{AS}	20	mJ
Peak Diode Recovery dv/dt (Note 4)			dv/dt	3.5	V/ns
Power Dissipation	TO-220		P_D	80	W
	TO-252			42	W
	PDFN3×3			25	W
	PDFN5×6			35	W
Junction Temperature			T_J	+150	°C
Storage Temperature Range			T_{STG}	-20 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L=0.1mH, I_{AS}=20A, V_{DD}=50V, R_G=25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 30A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	°C/W
	TO-252		110	°C/W
	PDFN3×3		130	°C/W
	PDFN5×6		65	°C/W
Junction to Case	TO-220	θ_{JC}	1.56	°C/W
	TO-252		2.97 (Note)	°C/W
	PDFN3×3		5 (Note)	°C/W
	PDFN5×6		3.57 (Note)	°C/W

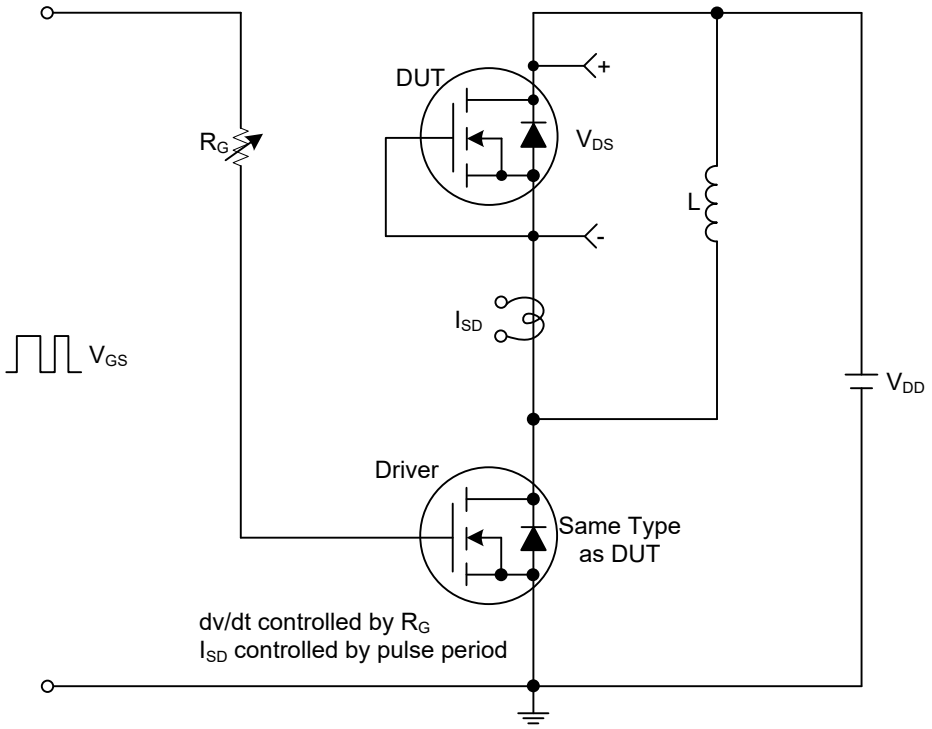
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

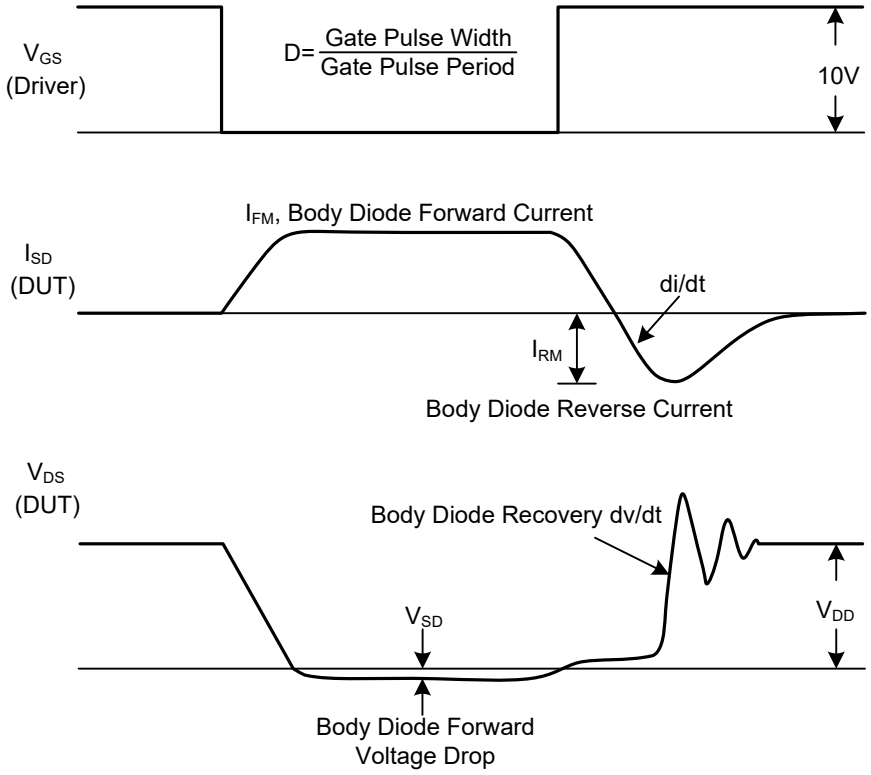
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=100V, V_{GS}=0V			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	1.8	2.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		14	16	mΩ
			V_{GS}=4.5V, I_D=10A		22	28	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz		1212		pF
Output Capacitance		C_{OSS}			525		pF
Reverse Transfer Capacitance		C_{RSS}			58		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	V_{DS}=80V, V_{GS}=10V, I_D=40A, (Note 1, 2)		32		nC
Gate to Source Charge		Q_{GS}			10		nC
Gate to Drain Charge		Q_{GD}			7		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	V_{DD}=50V, V_{GS}=10V, I_D=40A, R_G =3.3Ω (Note 1, 2)		8		ns
Rise Time		t_R			16		ns
Turn-off Delay Time		$t_{D(OFF)}$			23		ns
Fall-Time		t_F			17		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				48	A
Maximum Body-Diode Pulsed Current		I_{SM}				80	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I_S=20A, V_{GS}=0V		0.88	1.2	V
Reverse Recovery Time (Note 1)		t_{rr}	I_S=30A, V_{GS}=0V, dI_F/dt =100A/μs		130		nS
Reverse Recovery Charge		Q_{rr}			160		nC

Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



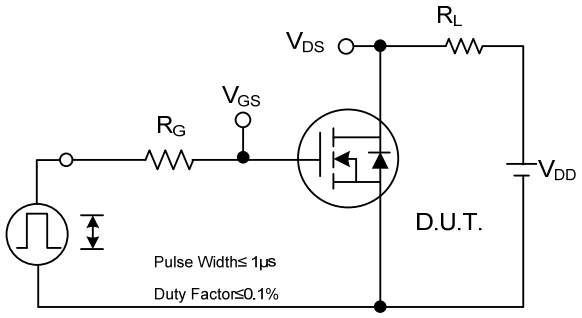
Peak Diode Recovery dv/dt Test Circuit



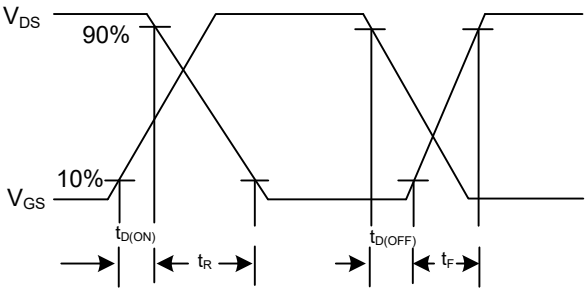
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

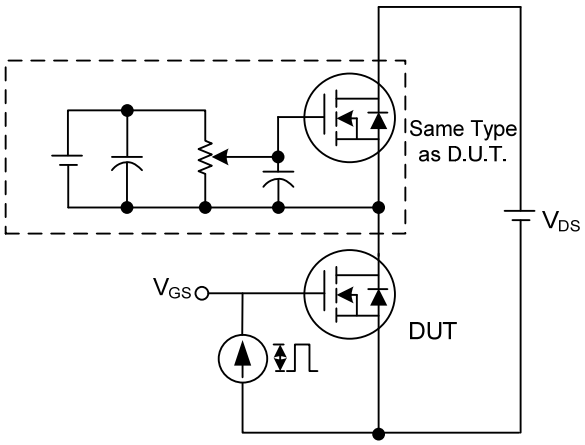
■ TEST CIRCUITS AND WAVEFORMS



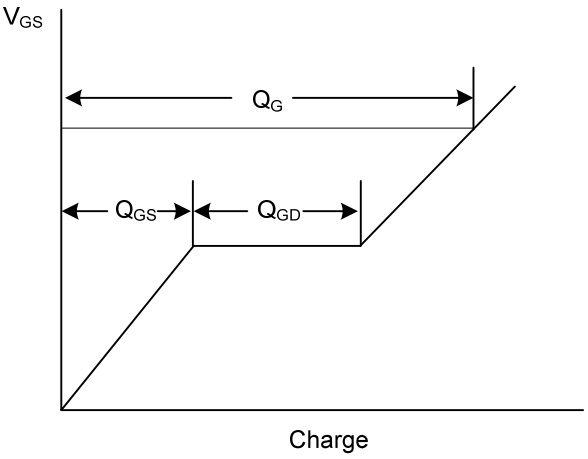
Switching Test Circuit



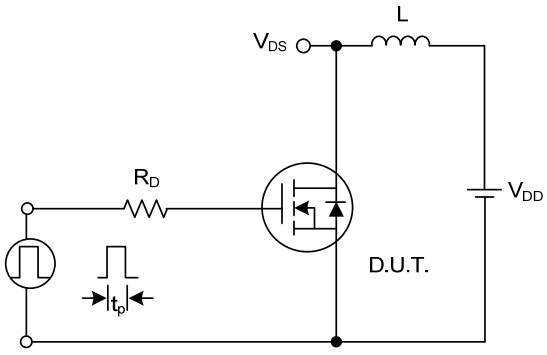
Switching Waveforms



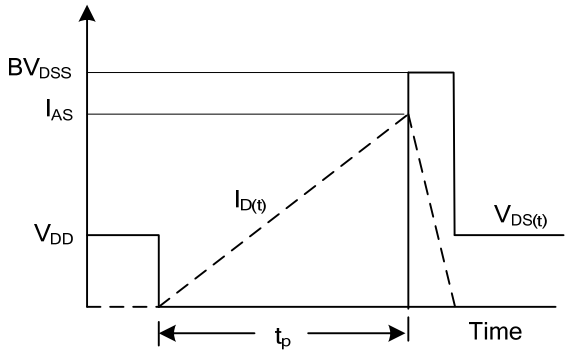
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms