General PWM-IC
FA13842 / 43 / 44 / 45

Datasheet

1. Description

The FA1384X series are CMOS type current mode control ICs for off-line and dc-to-dc converter.
These ICs can reduce start-up circuits loss and are optimum for high efficiency power supply because of low power dissipation of these ICs achieved by CMOS process .
These ICs are can drive a power MOSFET directly.
A high-performance power supply can be designed compactly with minimal external components .

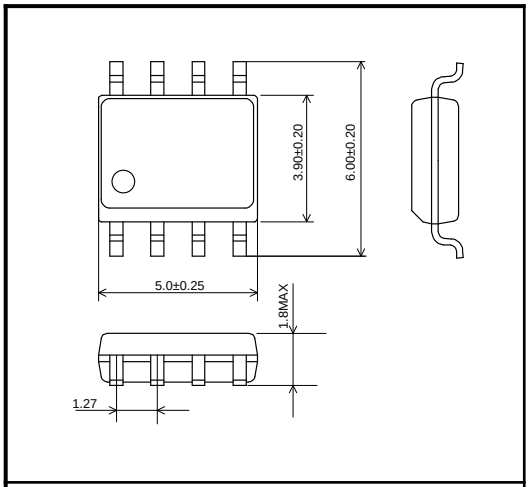
2. Features

- Low-power dissipation by CMOS Process
- Stand-by current 2μA(max.) , start-up current 30μA(max.)
- Pulse-by-pulse current limiting
- 5V bandgap reference
- UVLO with hysteresis
- Maximum duty cycle 96%（FA13842/43）, 48%（FA13844/45）
- Pin-for-pin compatible with UC384X

Notes)

Pins are compatible, but the characteristics are not fully compatible .

When you applies our ICs to power supply circuit designed for other manufacture's 384X series, you must check the characteristics and the safety on your power supply.

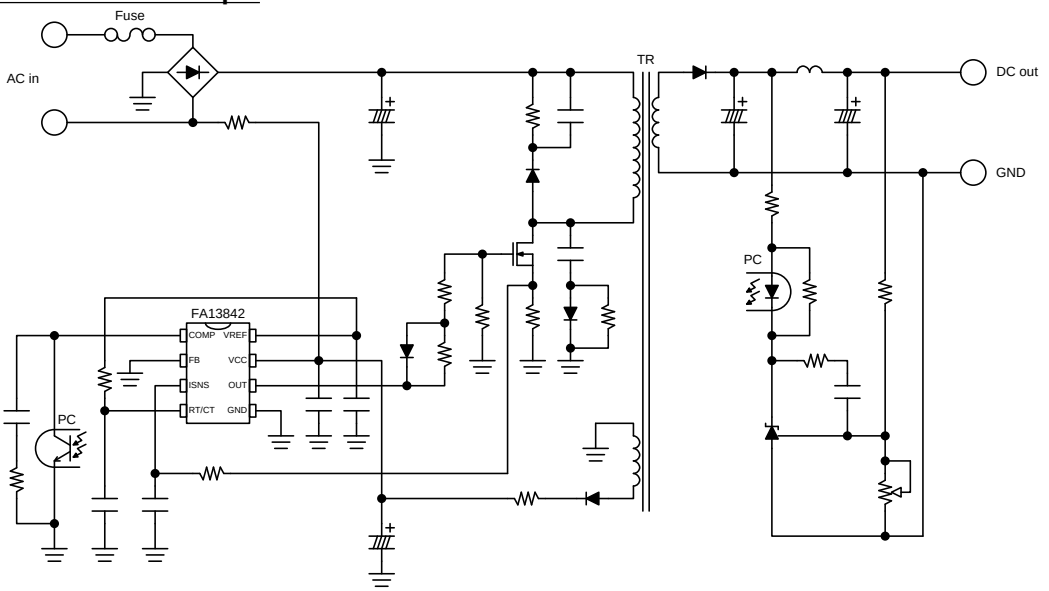


Package：SOP-8

Function list by type

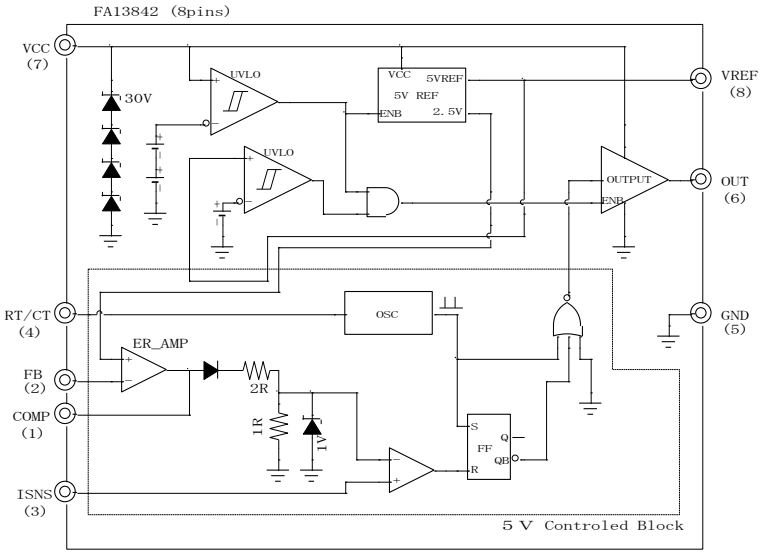
type	UVLO		Maximum duty cycle
	Start Threshold	Stop Threshold	
FA13842N	16.5V±1V	9V±1V	96%
FA13843N	9.6V±1V	9V±1V	96%
FA13844N	16.5V±1V	9V±1V	48%
FA13845N	9.6V±1V	9V±1V	48%

3. Application circuit example

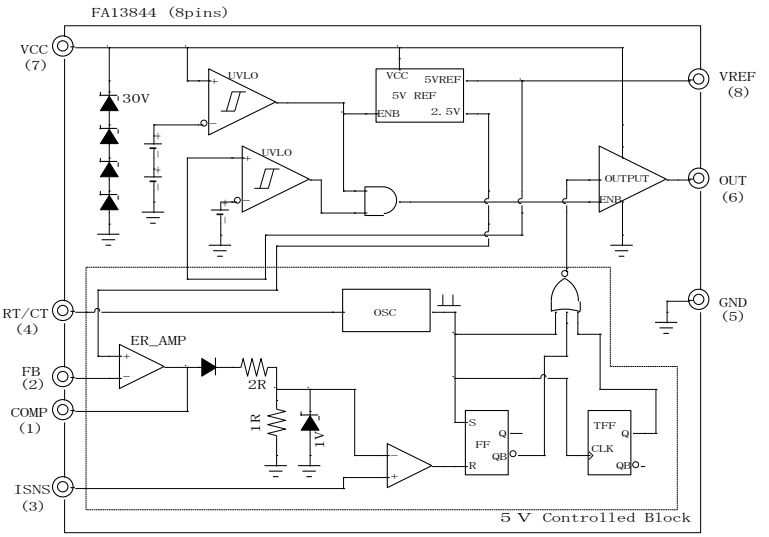


4. Block diagram

FA13842/43

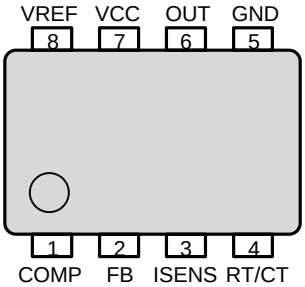


FA13844/45



5. Functional description of pins

Pin No.	Pin name	Pin Function	Note
1	COMP	Compensating	*1, *2
2	FB	Feedback	*3
3	ISENS	Current sense	*1, *2
4	RT/CT	Oscillator control	*1, *2
5	GND	Ground	—
6	OUT	Output	*2
7	VCC	Power supply	*1, *2
8	VREF	5V reference voltage output	*1



Notes)
*1 Connect the capacitor
*2 Connect the resistor
*3 Connect the resistor and capacitor when used error amp

6. Rating & characteristics

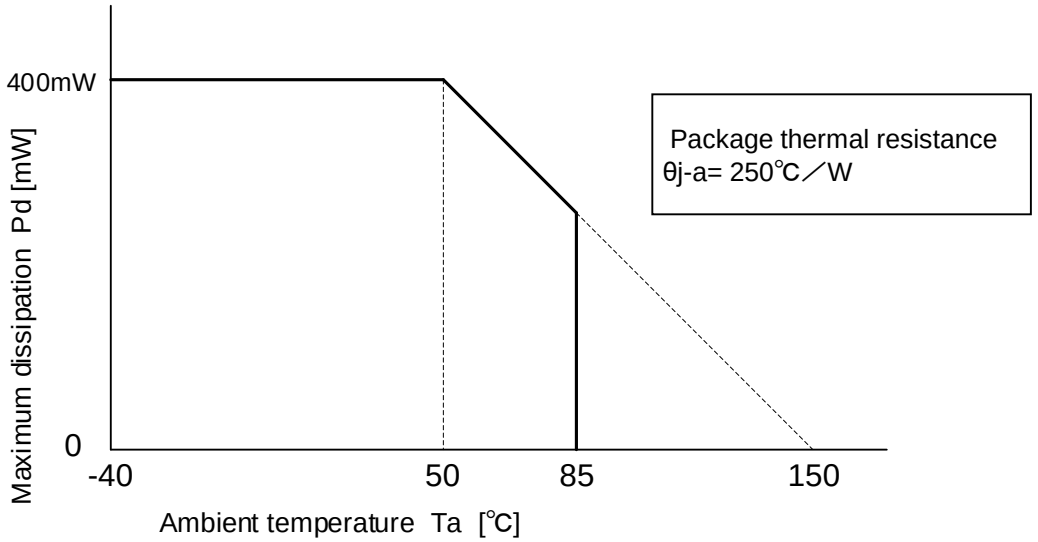
Stress exceeding absolute maximum ratings may malfunction or damage the device.
"-" shows source and "+" shows sink in current descriptions.

(1) Absolute maximum ratings

Item		Symbol	Rating	Unit
Supply voltage *1	When the capacity of low impedance source current supply over than 10mA. (Isource>10mA)	VCC1	-0.3 to 28	V
	Internal zener clamp voltage (ICC<10mA)	VCC2	-0.3 to Self limiting	V
Zener current at VCC pin		IZD	10	mA
Output voltage at OUT pin		VOUT	-0.3 to VCC+0.3	V
Peak current at OUT pin *2	Sink current	IOL	+1.0	A
	Source current	IOH	-400	mA
Input voltage at FB pin, ISNS pin, COMP pin		VFB, VISNS, VCOMP	-0.3 to 5.3	V
Current at FB pin, ISNS pin		IFB, IISNS	±0.1	mA
Source current at COMP pin		IsoCOMP	-2	mA
Sink current at COMP pin		IsiCOMP	25	mA
Voltage at VREF pin		VREF	-0.3 to 7	V
Output current at VREF pin *1		IREF	-25 to 0	mA
Voltage at RT/CT pin		VRTCT	-0.3 to 5.3	V
Sink current at RT/CT pin		IRTCT	15	mA
Power dissipation (Ta=50℃)		Pd	400	mW
Thermal resistance, junction to ambient *3		θj-a	250	℃/W
Operating junction temperature		Tj	-40 to +150	℃
Storage temperature		Tstg	-40 to +150	℃

Notes)
*1 Please consider power supply voltage and current well and use this IC within maximum power dissipation. The IC may cross over maximum power dissipation at normal operating condition by power supply voltage.
*2 Peak current at OUT pin may flow to rated value neither according to VCC voltage nor temperature conditions.
Please consider power supply voltage and load current well and use this IC within maximum power dissipation, operating junction temperature and recommended ambient temperature in operation. The IC may cross over maximum power dissipation at normal operating condition by power supply voltage or load current within peak current absolute maximum rating value
*3 JEDEC STANDARD test board

※Maximum dissipation curve



(2) Recommended operating conditions

Notes)

(1) Recommended value is conditions for guaranteeing that the product operates normally. If it is used out of this condition, there is possibility of have a negative influence on operation and reliability.

(2) Please use it after confirming operation enough with your products when you use it.

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	10	15	25	V
RT resistor	RT	2.0	10	100	kΩ
CT capacitor	CT	0.47	3.3	10	nF
Operating frequency (RT/CT)	fosc	10	―	500	kHz
Threshold voltage of power MOSFET *1	VthMOS	2.0	―	―	V
Ambient temperature in operation	Ta	-40	―	85	℃

*1 When VCC pin voltage is lower than 2V during start up with high temperature, OUT pin output voltage may become HIGH state.
Therefore, please check and confirm the start up operation under high temperature condition with power board.

(3) DC electrical characteristics

The characteristics in this section are those in conditions as follows unless otherwise specified. The voltages described in the conditions are DC input values (not AC input values).

VCC=15V, FB=GND , ISNS=GND , COMP：open , VREF：1uF , OUT：no load , RT：10kΩ, CT：3.3nF, Tj=25℃

Notes）
(1)The item which indicated “*1” are not 100% tested in production but guaranteed by design.
(2)No guaranteed value exists for the column of “—“.
(3)“-” shows source current and “+” shows sink current in current output characteristics

3-1. Reference voltage section (VREF pin)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage		VREF	Tj=25℃,IL=1mA	4.75	5.00	5.25	V
	Line regulation	VREF LINE	Vcc=10～25V	-	±3	±20	mV
	Load regulation *1	VREF LOAD	IL=0～20mA	-	±3	±25	mV
	Temperature stability *1	VdT	Tj=-40～125℃	-	±0.3	-	mV/℃
Output short current *1, *4		IREF	Tj=25℃	-	-60	-	mA

*4 If a short circuit condition to continue, the loss of IC may be exceeded maximum power dissipation. Please consider power supply voltage and current well and use this IC within allowable power dissipation and maximum junction temperature. 。

3-2. Oscillator section (RT/CT pin)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency		fosc	Tj=25℃	49	52	55	kHz
		fosc tmp	Tj=-40～125℃ *1	47	52	57	kHz
	Voltage stability	fosc line	Vcc=10～25V	-	±0.25	±1	%
	Temperature stability *1	fdT	Tj=-40～125℃	-	-0.07	-	%/℃
Amplitude *1		VRTCT	Tj=25℃	-	1.6	-	V
Discharge current		Idis RTCT	Tj=25℃	6.5	8.4	12.5	mA

3-3. Error amp section (COMP pin, FB pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	VFB	VCOMP=2.5V, Tj=25℃	2.4	2.5	2.6	V
Input leak current	IinFB	VFB=0V to VREF	-	-	±2	μA
Open-loop gain *1	Av	VCOMP=2.5V	65	72	90	dB
Unity gain bandwidth *1	fT	VCOMP=2.5V	0.7	1	1.5	MHz
Output source current	IsoCOMP	VFB=2.3V, VCOMP=0V	-1.6	-1.0	-0.8	mA
Output sink current	IsiCOMP	VFB=2.7V, VCOMP=1V	2	15	22	mA
Output voltage	VOH COMP	VFB=2.3V, RL=15kΩ to GND	4.0	4.5	4.9	V
	VOL COMP	VFB=2.7V, RL=15kΩ to VREF	10	80	500	mV

3-4. Current sense section (ISNS pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1	AvIS	Tj=25℃	2.85	3	3.15	V/V
Maximum input signal	VthISNS	VFB=0V	0.9	1.0	1.1	V
Input bias current	IinISNS		-5	-1	1	μA
Delay to output *1	TdISNS	Tj=25℃ *5 ISNS input signals Vpulse:0V to 2V ISNS to OUT:turn off	75	150	300	ns

*5 The input signals of measurement are square wave-form.（tr,tf<10ns）

3-5. Output section (OUT pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output high level	VOH1	Isource=-20mA	14.5	14.75	14.9	V
	VOH2	Isource=-100mA	12	13.5	14.5	V
Output low level	VOL1	Isink=20mA	0.05	0.15	0.3	V
	VOL2	Isink=200mA	0.5	1.5	3	V
Rise time *1	Tr	CL=1nF,Tj=25℃	20	40	150	ns
Fall time *1	Tf	CL=1nF,Tj=25℃	10	20	150	ns

3-6. Under voltage lock out section (VCC pin)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Start-up threshold voltage	VCCON	VCC =Increasing	FA13842/44	15.5	16.5	17.5	V
			FA13843/45	8.6	9.6	10.6	V
Shutdown threshold voltage	VCCOFF	VCC=Decreasing		8	9	10	V
Hysteresis voltage	VhysVCC	VCCON-VCC OFF	FA13842/44	6.5	7.5	8.5	V
			FA13843/45	0.3	0.6	1.0	V

3-7. PWM section (COMP pin , OUT pin)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum duty cycle	DMAX	OUT pin	FA13842/43	94	96	98	%
			FA13844/45	47	48	50	%
Minimum duty cycle	DMIN	VFB=5V, COMP=open		-	-	0	%

3-8. Overall section (VCC pin)

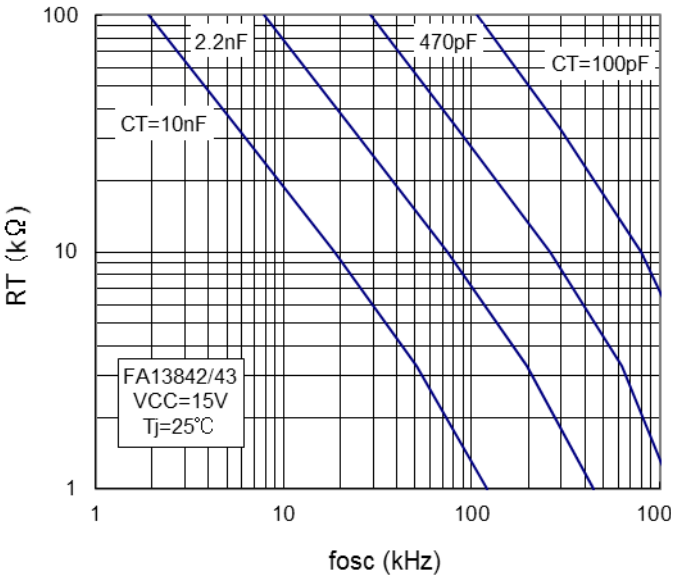
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Standby current	ICCSTB	FA13842/44 : VCC=14V FA13843/45 : VCC=7V	-	-	2	μA
Start-up current *1	ICCSTUP	VCC=VCCON	5	12	30	μA
Operating current	ICCOP	VCC=15V	1	3	5	mA
Zener voltage (VCC)	VZD	ICC=5mA	28	30	34	V

7. Characteristic curve

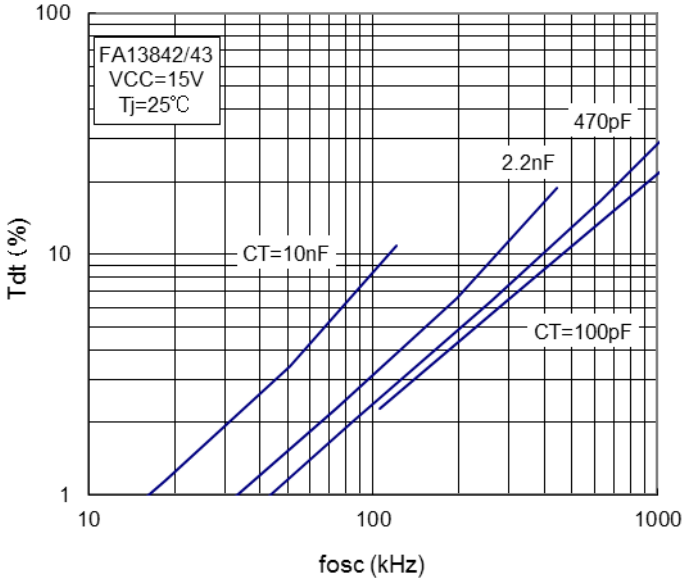
The characteristics in this section are under described conditions as follows unless otherwise specified.
VCC=15V, FB=GND, ISNS=GND, COMP：open, VREF：1uF, OUT：no load, RT：10kΩ, CT：3.3nF, Tj=25℃

Notes）
（1）“-” shows source current and “+” shows sink in current regulations of the current.
（2）The data listed here show the typical characteristics of an IC, and does not guarantee the characteristic.

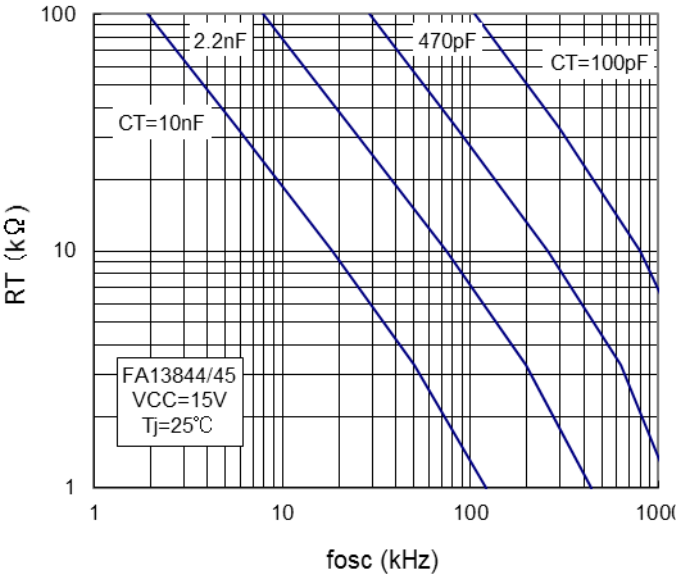
RT timing resistance (RT)
vs. Oscillator frequency (fosc)



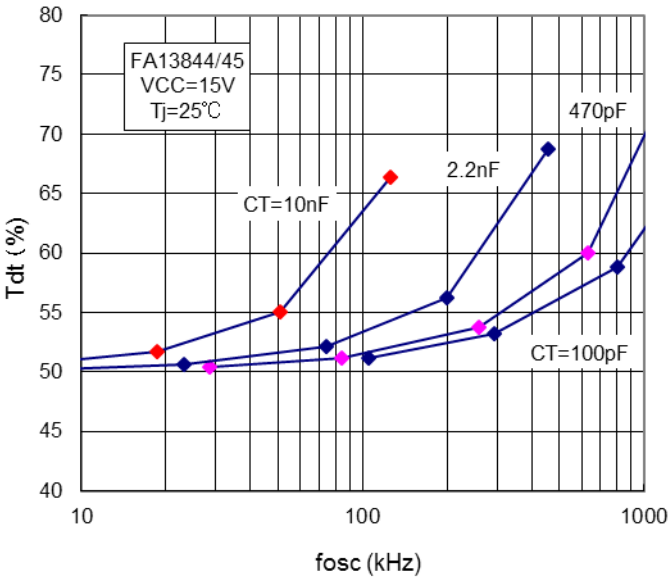
Output dead time (Tdt)
vs. Oscillator frequency (fosc)



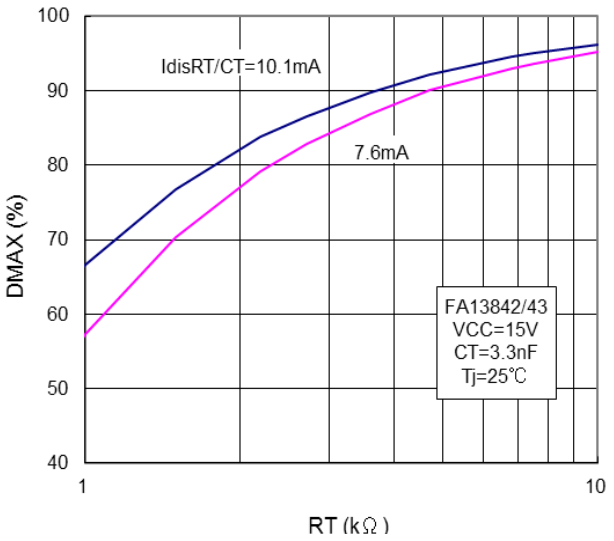
RT timing resistance (RT)
vs. Oscillator frequency (fosc)



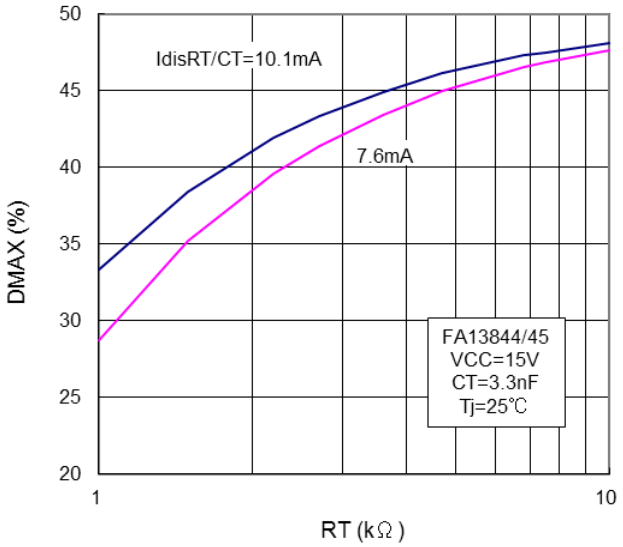
Output dead time (Tdt)
vs. Oscillator frequency (fosc)



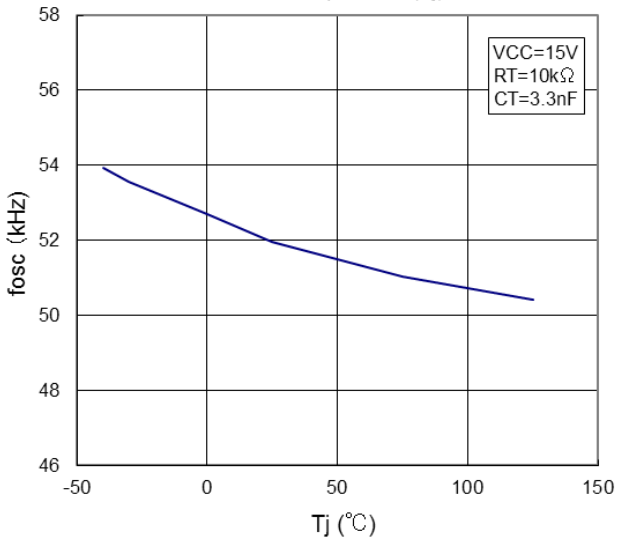
Output maximum duty cycle (DMAX)
vs.RT timing resistance (RT)



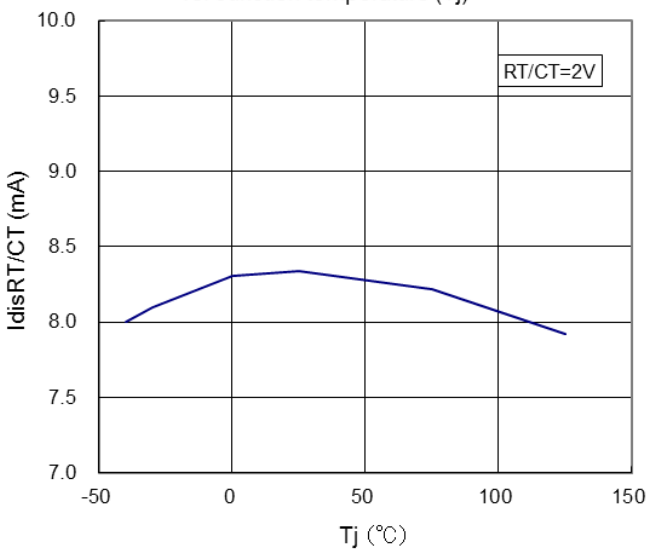
Output maximum duty cycle (DMAX)
vs.RT timing resistance (RT)



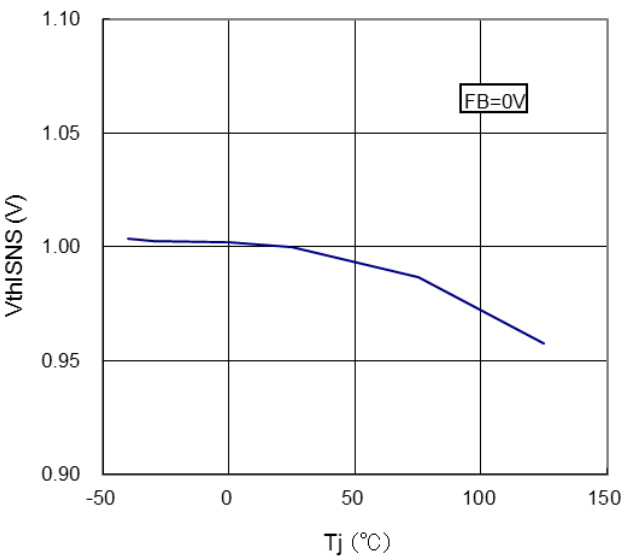
Oscillator frequency (fosc)
vs. Junction temperature (Tj)



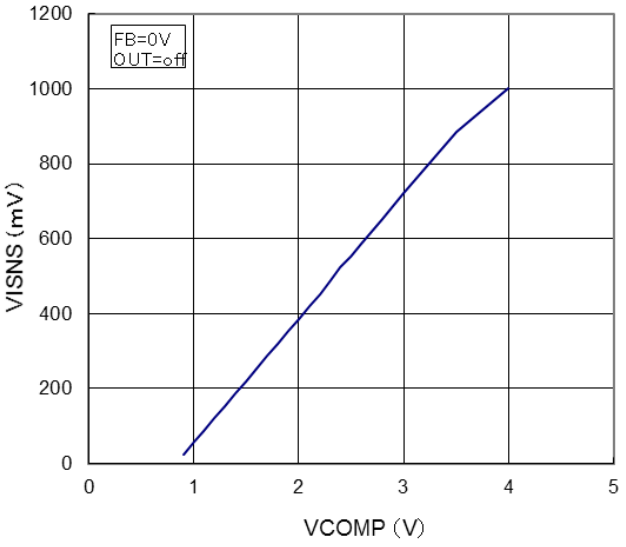
RT/CT discharge current (IdisRT/CT)
vs. Junction temperature (Tj)



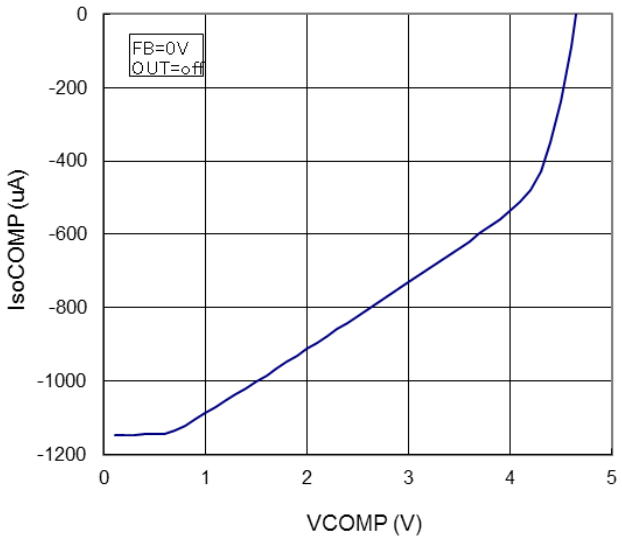
IS maximum input signal (VthISNS)
vs. Junction temperature (Tj)



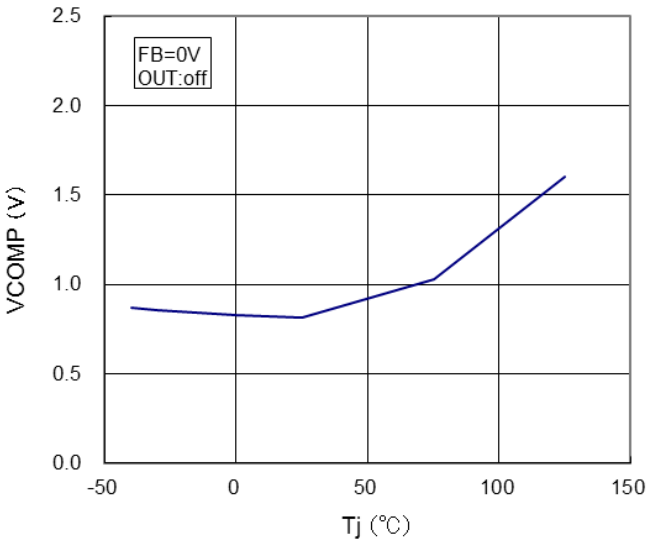
ISNS voltage (VISNS)
vs. COMP voltage (VCOMP)



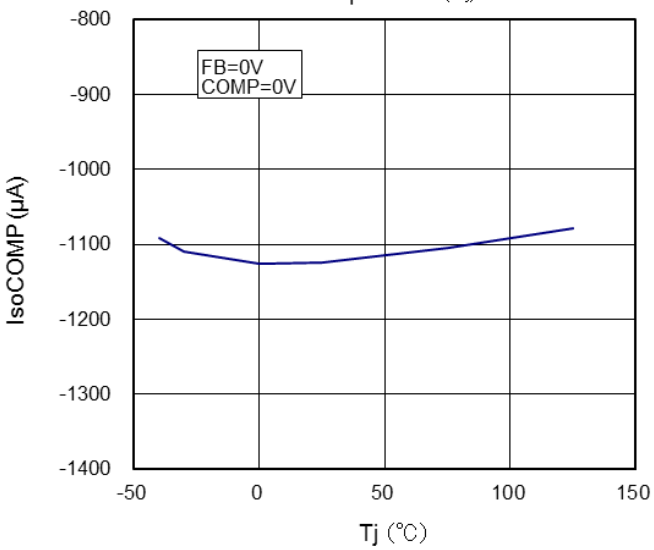
COMP source current (IsoCOMP)
vs. COMP voltage (VCOMP)



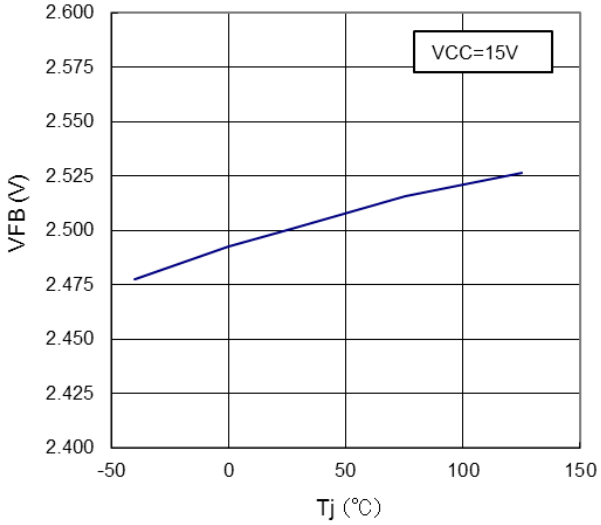
COMP voltage of OUT off (VCOMP)
vs. Junction temperature (Tj)



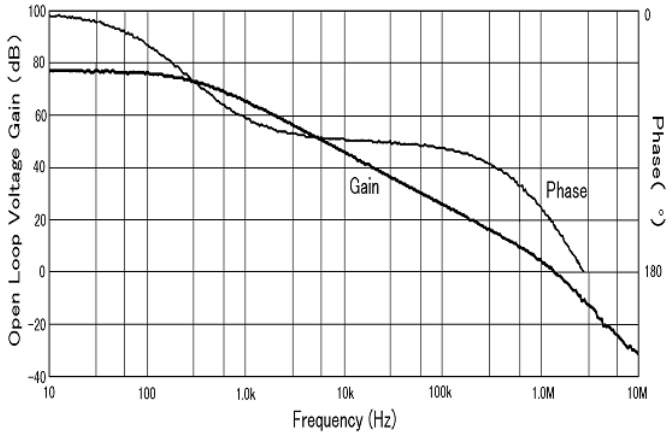
COMP source current (IsoCOMP)
vs. Junction temperature (Tj)



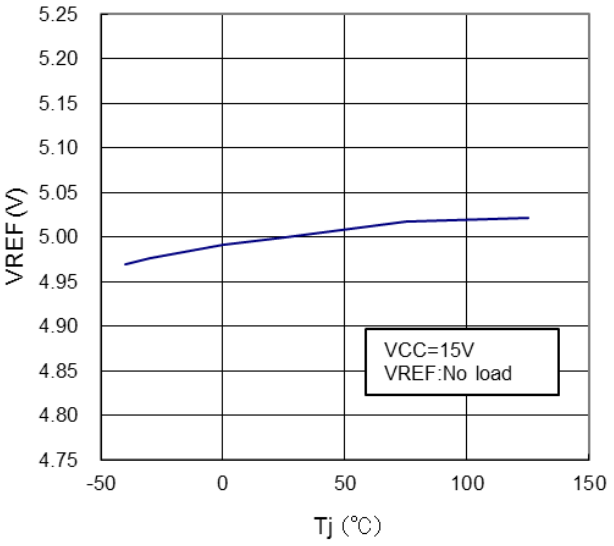
Error amplifier input voltage (VFB)
vs. Junction temperature (Tj)



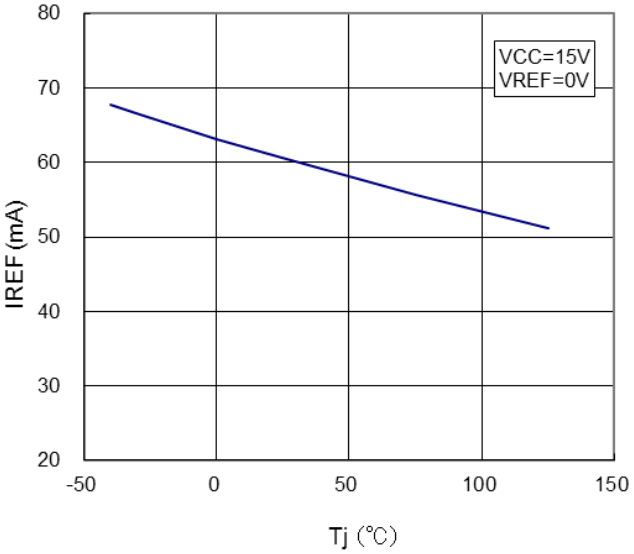
Error amp open loop gain and phase
vs. Frequency



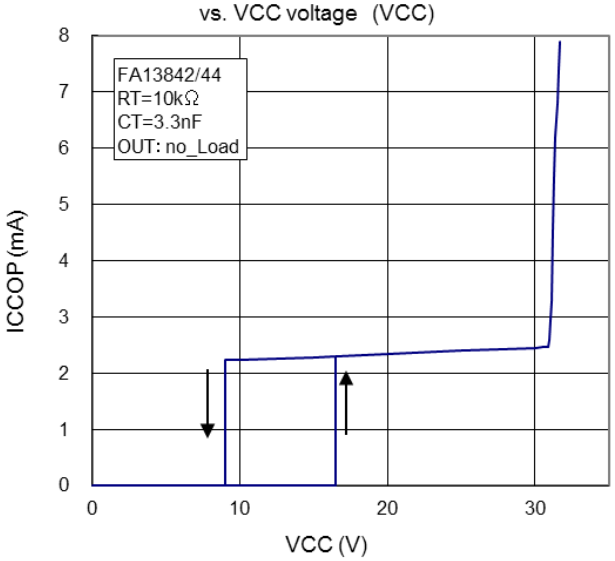
VREF output voltage (VREF)
vs. Junction temperature (Tj)



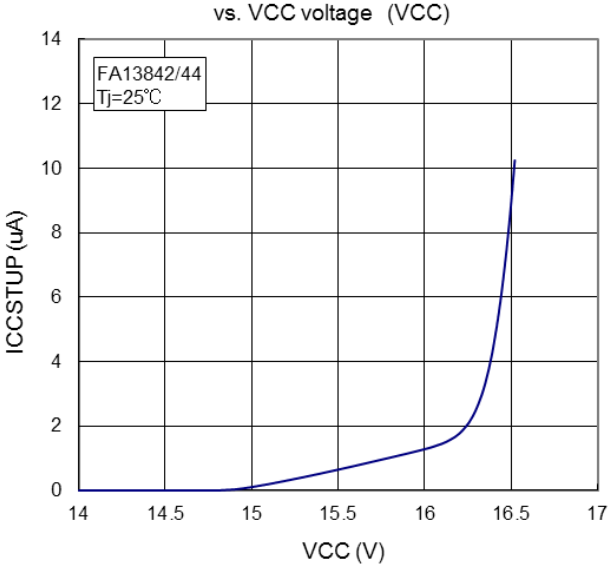
VREF short current (IREF)
vs. Junction temperature (Tj)



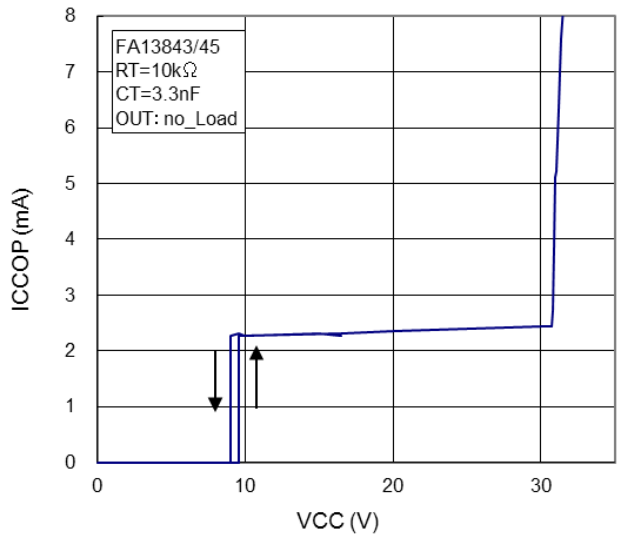
VCC supply current (ICCOP)
vs. VCC voltage (VCC)



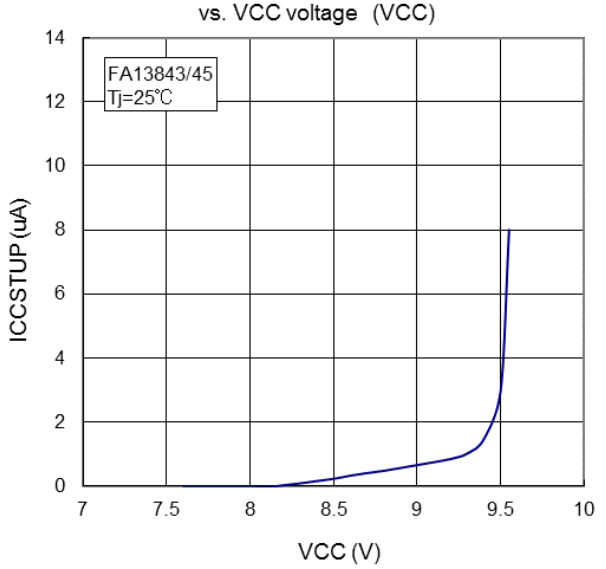
VCC startup current (ICCSTUP)
vs. VCC voltage (VCC)



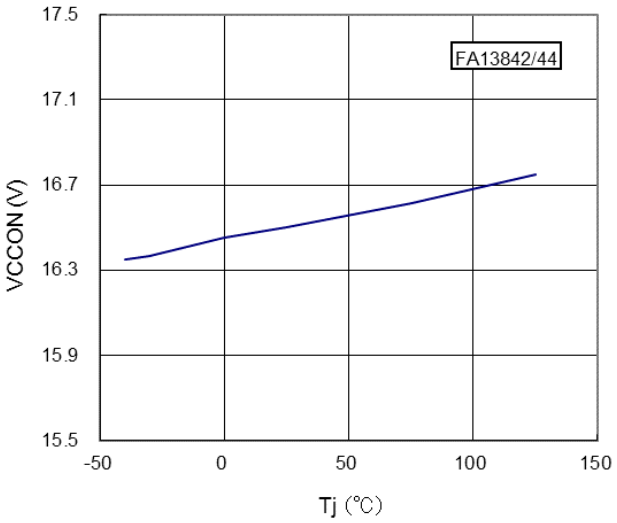
VCC supply current (ICCOP)
vs. VCC voltage (VCC)



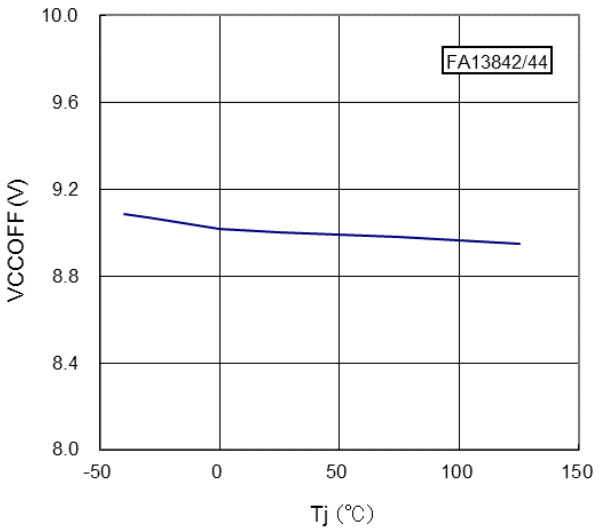
VCC startup current (ICCSTUP)
vs. VCC voltage (VCC)



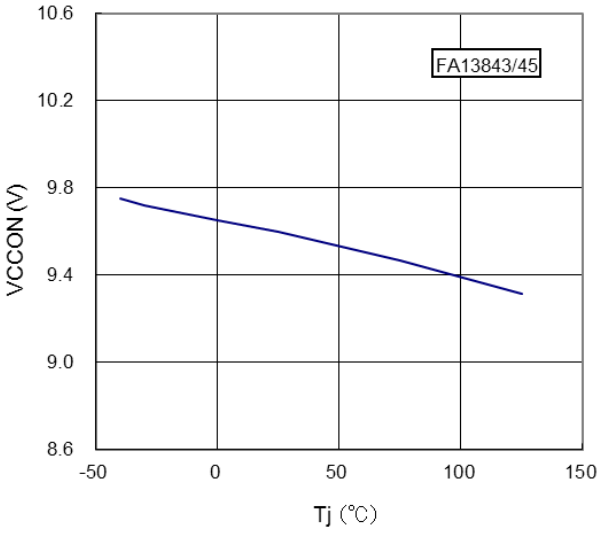
Start-up threshold voltage (VCCON)
vs. Junction temperature (Tj)



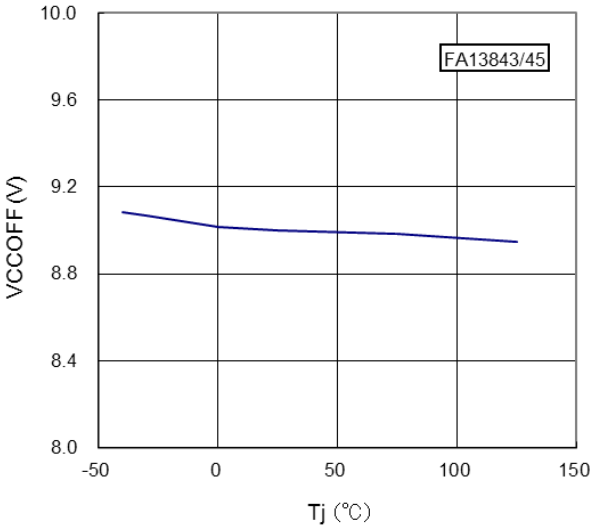
Shutdown threshold voltage (VCCOFF)
vs. Junction temperature (Tj)



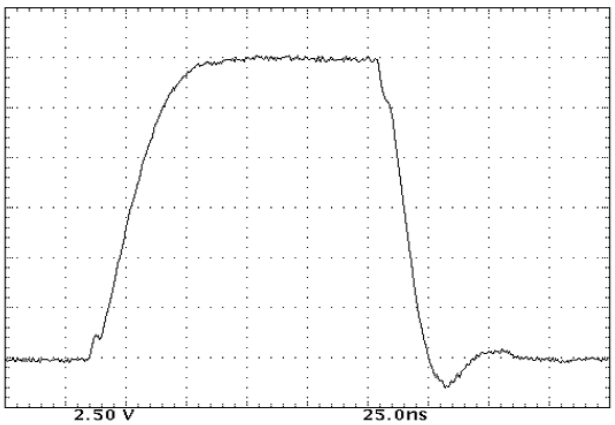
Start-up threshold voltage (VCCON)
vs. Junction temperature (Tj)



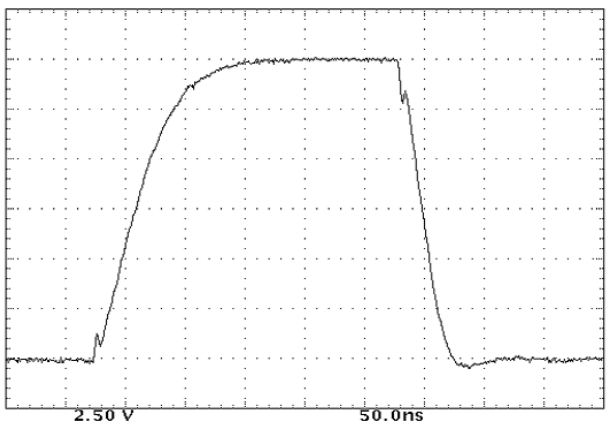
Shutdown threshold voltage (VCCOFF)
vs. Junction temperature (Tj)



OUT waveform（CL=1nF）



OUT waveform（CL=2.2nF）



8.Description of each circuit (The values in the following description are typical values unless otherwise specified.)

(1) Oscillator

The oscillation frequency is set by timing resistance Rt and timing capacitor Ct, which are connected to RT/CT pins. Ct is charged to about 3V through the Rt from the 5V reference ,and discharged to about 1.4V by the built-in discharge circuit. (See Fig. 1, 2, 3.)
Blanking pulses are generated in the interior during the Ct discharge period.
The output is fixed in the "low" state by these pulses, and a fixed dead time is produced. See the characteristics graphs shown in Fig. 1 - 4 regarding the relation among the oscillation frequency, RT and CT.

In the case of FA13844/45, a flip-flop is contained, and the output is blanked with every other cycle by this flip-flop. Therefore, the switching frequency of a power MOSFET is 1/2 of the oscillator frequency set by Rt and Ct.
(See Fig. 3.)

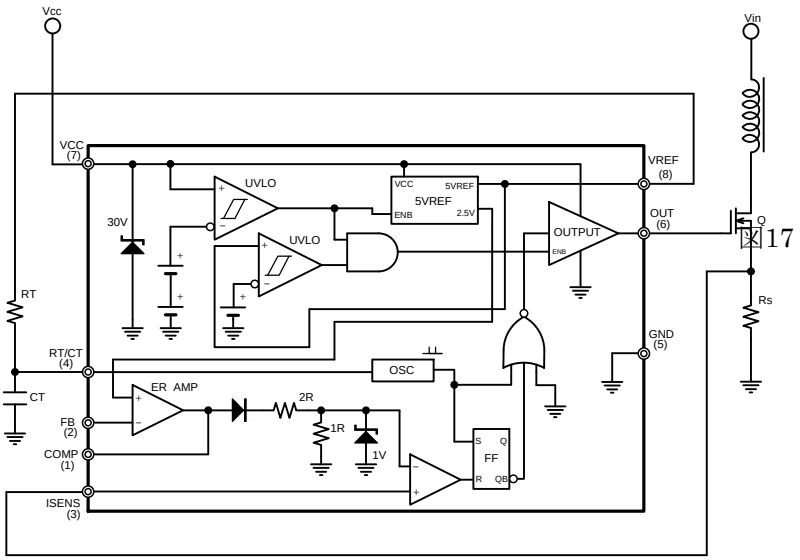


Fig.1 Block diagram of operating circuit

FA13842/43

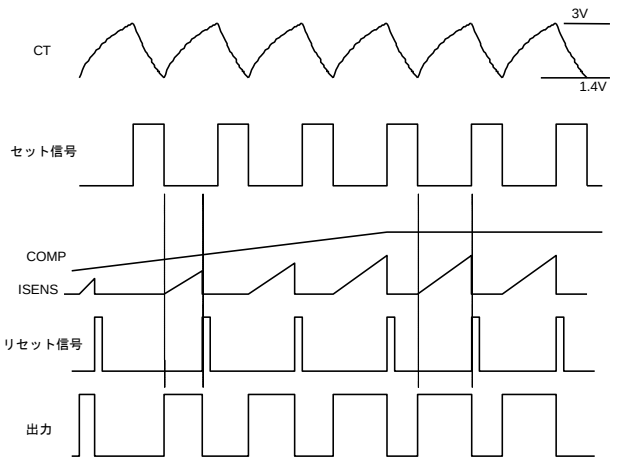


Fig2. Basic operation timing chart (FA13842/43)

FA13844/45

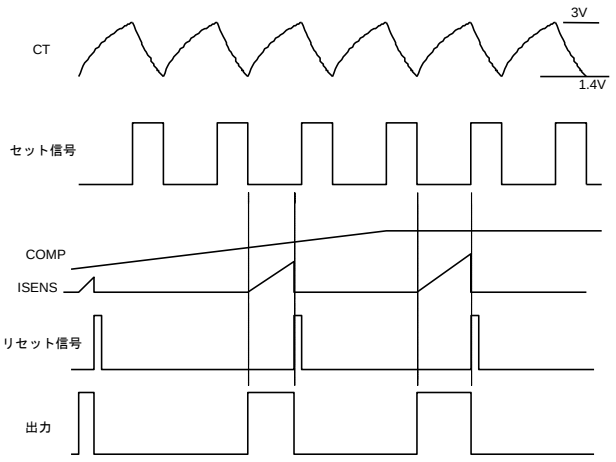


Fig3. Basic operation timing chart (FA13844/45)

(2) Error amplifier

Inverting input and output are connected to the FB pin and COMP pin respectively. The 2.5V reference is connected internally to the non-inverting input.
The output voltage is offset by diode VF voltage (=0.7V), and divided by three. The divided voltage is connected to the input of the current sense comparator.

(3) Current sense comparator and PWM latch

"High" state of OUT pin begins on the starting time of charging Ct. The state of out terminal turns to "Off" when the peak inductor current reaches the threshold level controlled by the error amplifier output (COMP pin) .
The inductor current is converted to a voltage by sense resistor Rs inserted between GND and the source of a power MOSFET. This voltage is monitored by ISNS pin
The peak current of inductor "Ipk" is expressed as follows.

Ipk=(Vcomp-0.7)/(3*Rs) 0.7≒VF
Vcomp : a voltage on COMP pin

The maximum value of the threshold level of the current sense comparator is internally clamped at 1V, therefore the maximum peak current "Ipk(max)" is as follows.

Ipk(max)=1.0V/Rs

(4) Under-voltage lockout (UVLO)

In order to set the IC in the complete operation mode before the output stage(OUT pin) is enabled, two under-voltage lockout comparators are incorporated to monitor the power supply voltage (Vcc) and reference voltage (VREF).

The threshold level of the Vcc comparator is set at 16.5V/9V for FA13842/44 and at 9.6V/9V for FA13843/45. In the standby mode which the Vcc is under ON threshold, the power supply current is kept at nearly 0 (zero). However, a current of 30μA at maximum is required to transfer from standby mode to operating mode .

The threshold level of the VREF comparator is set at about 3.2V/2.0V.
A 30V zener diode is connected Vcc and GND, to protect the IC against overvoltage .

(5) Output stage

An output stage of CMOS inverter composition is incorporated, and it is possible to fully swing the gate voltage of a power MOSFET to the Vcc.
The output stage provides the capacity of 400mA source current and 1A sink current as the peak current. (When Vcc is 15V)
The output stage is held in the "Low" state at standby mode.

(6) Reference voltage

The 5.0V(±5%) bandgap reference(Tj=25℃) is built-in.
It is possible to supply current of about 10mA to an external circuit in addition to charge current to the timing capacitor of the oscillator.
Connect a ceramic bypass capacitor of 0.1μF or higher to the VREF pin to stabilize this voltage.

9. Design advice (The values in the following description are typical values unless otherwise specified.)

(1) Start-up circuit

A typical start-up circuit is shown in Fig. 4.
The AC INPUT voltage charges capacitor C2 and supply start-up current to the IC through start-up resistance R1. When this voltage reaches the ON threshold voltage, the IC turn to the operation mode and electric power is supplied from the bias winding of the transformer thereafter.
By means of CMOS process, the start-up current is less than 30μA .
When the start-up resistance is increased, charging of capacitor C2 becomes slower and the start-up time increases. Select the optimum values of R1 and C2 for your circuit.
The relation between the start-up resistance and start-up time for the circuit indicated in Fig.4 is shown in Fig. 5.

Fig.6 indicates a method to increase the start-up resistance for reducing its loss and to shorten the start-up time. The start-up time is shortened by reducing the capacitance of C2 and the bias current is supplied from C3 after start-up.

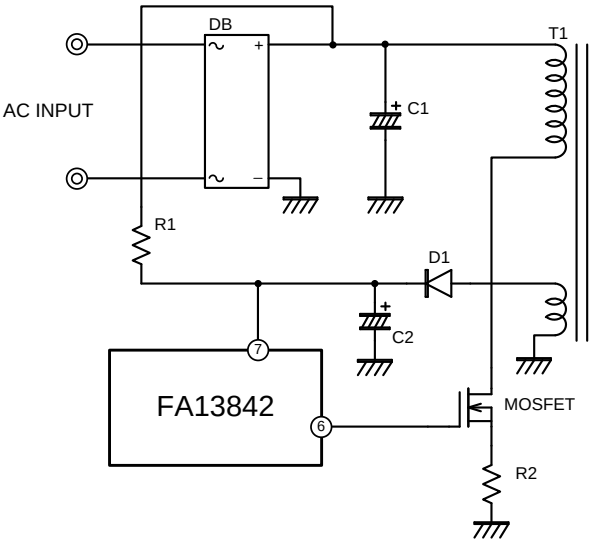


Fig.4 Start-up circuit

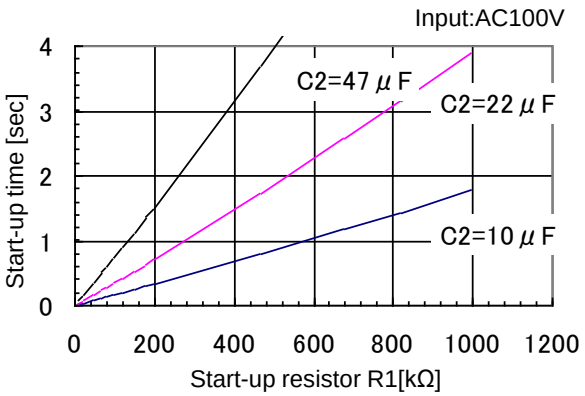


Fig.5 Start-up time vs Start-up resistor

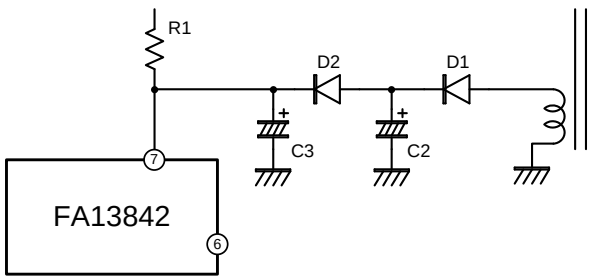


Fig.6 VCC pin circuit

(2) Synchronized operation with external signals

Synchronized operation with external signals is permitted with the circuit that is shown in Fig. 7.
Synchronized operation is started when the RT/CT pin is raised to about 3V or higher. (Synchronized at leading edge.)

It is necessary that the external synchronizing signal should be higher than the free run frequency.

In the case of FA13844/45, the output frequency of OUT pin is 1/2 of the synchronizing signal frequency

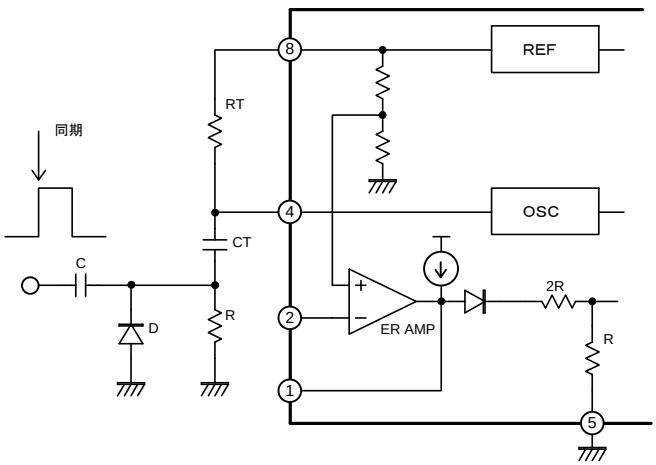


Fig.7 Synchronized operation with external signals

(2) Latched shutdown

A typical circuit for latched shutdown s shown in Fig. 8. The voltage of OUT pin is kept at low state if the voltage of COMP pin is held at low level. It is necessary that the voltage level of the COMP pin is set at 0.7V or less in the applied temperature range. (See P.9 COMP voltage of OUT off [VCOMP] vs Junction temperature[Tj] .)

The source current from COMP pin is less than about 1.3mA.

Use of such a thyristor shown in Fig. 9 is not effective because the saturation voltage of thyristor is higher than 0.7. When a thyristor is used, pull up the voltage of FB pin to over 3V as shown in Fig. 10. In the case of latched shutdown , it is necessary to supply current higher than the hold current of the thyristor composing circuit or of the thyristor. This current should be supply through a start-up resistor from AC input.

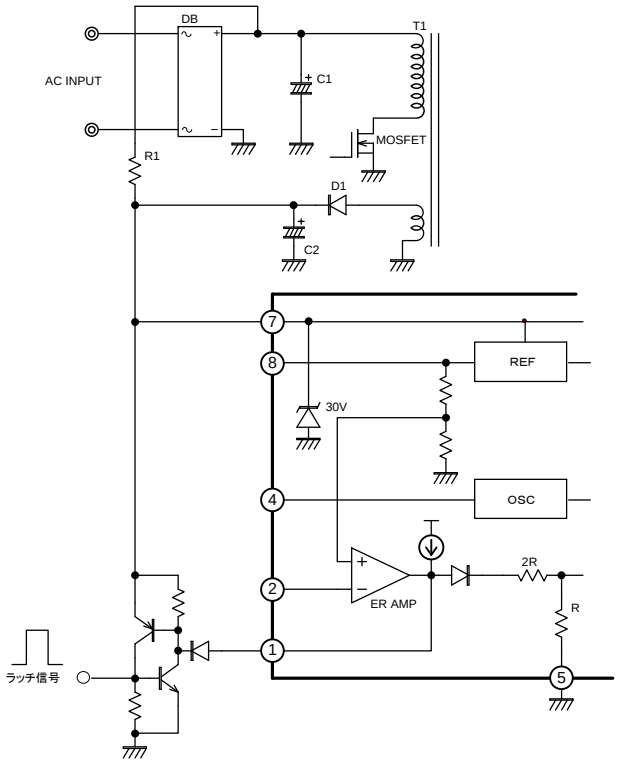


Fig.8 A typical circuit for latched shutdown

Latched shutdown by a thyristor using COMP pin is not effective.

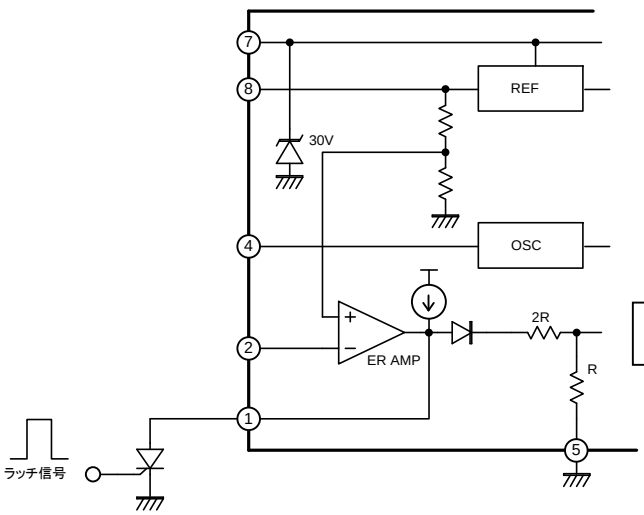


Fig.9 Bad example

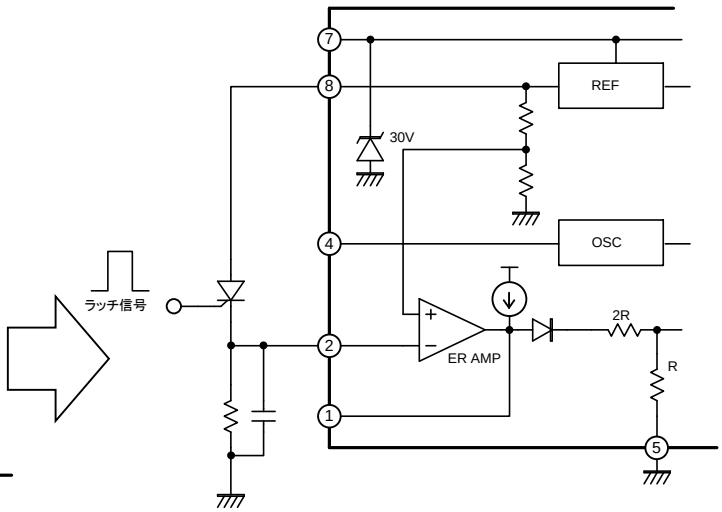


Fig.10 Good example using thyristor

①The method for detection of overvoltage

A typical circuit of latched shutdown to protect against the overvoltage detected on the primary side is shown in Fig. 11. When the secondary voltage rises in the flyback circuit, the voltage of the bias winding also rises in proportion to it. When this rise voltage is detected by zener diode ZD1, the latched shutdown is accomplished. Because the secondary voltage is detected through a transformer, the detection accuracy is not high.

② The method for detection of overvoltage (detection on secondary side)

A typical circuit of latched shutdown to protect against the overvoltage detected on the secondary side is shown in Fig. 12.
The accuracy of the detected voltage is high compared to detection of overvoltage on the primary side.

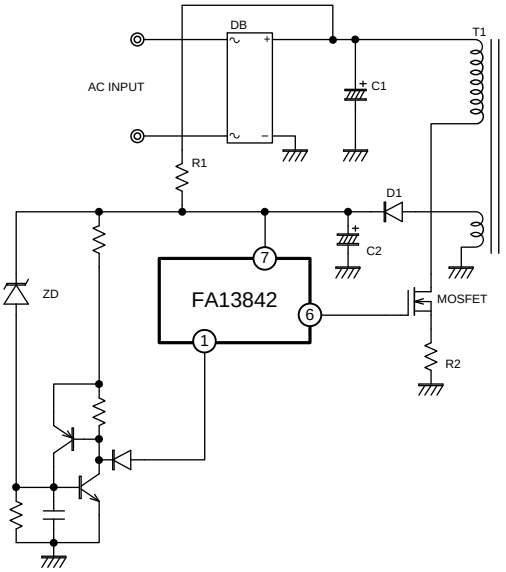


Fig.11 Overvoltage protection circuit (detection on primary side)

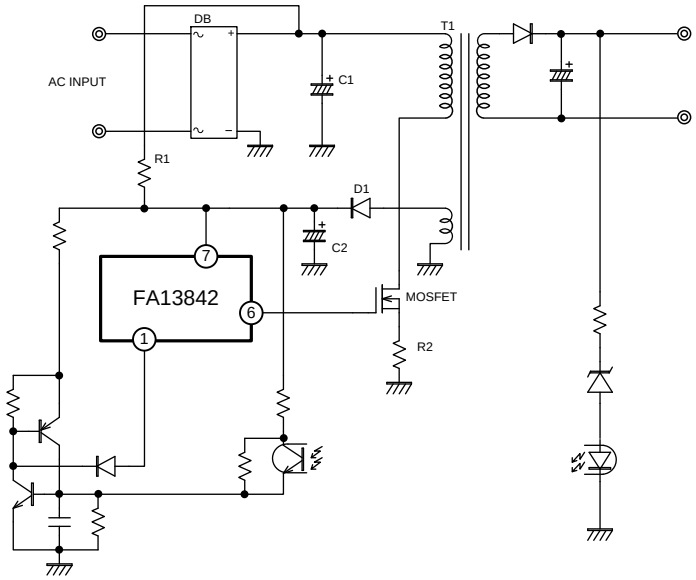


Fig.12 Overvoltage protection circuit (detection on secondary side)

③ The method for detection of overcurrent (detection of primary current)

A typical primary overcurrent detection circuit is shown in Fig. 13.

④ The method for detection of overcurrent (detection of secondary current)

A typical secondary overcurrent detection circuit is shown in Fig. 14.

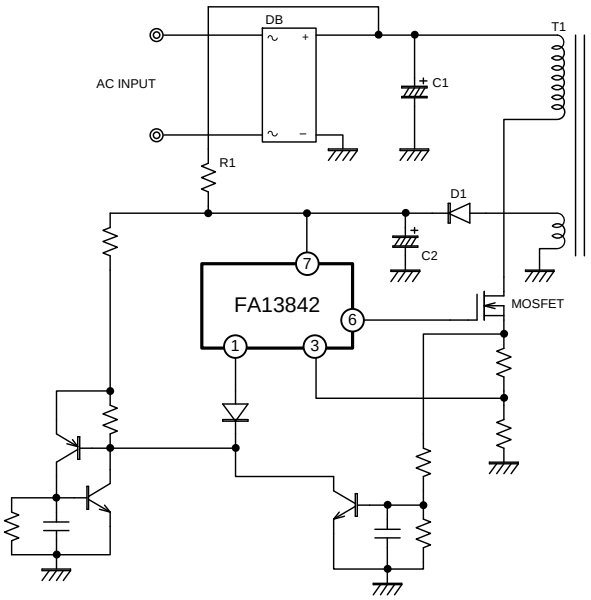


Fig.13 Overcurrent protection circuit (detection on primary side)

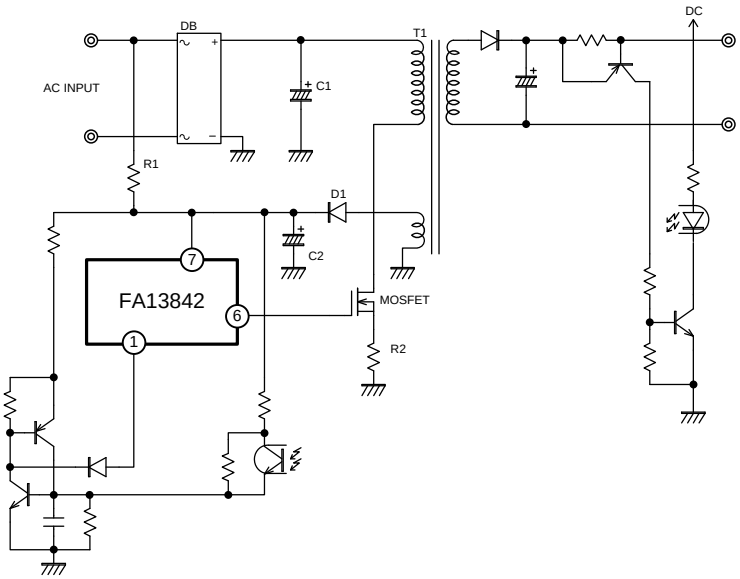


Fig.14 Overcurrent protection circuit (detection on secondary side)

(4) Soft start

A soft start circuit is shown in Fig. 15.

The soft-start time is determined by the time constant of the resistor and the capacitor.

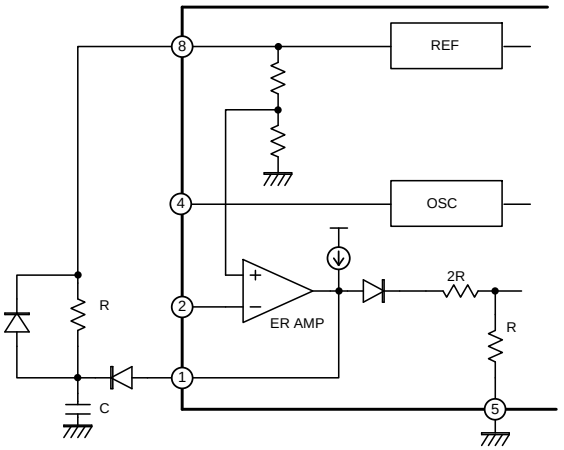


Fig.15 Soft start circuit

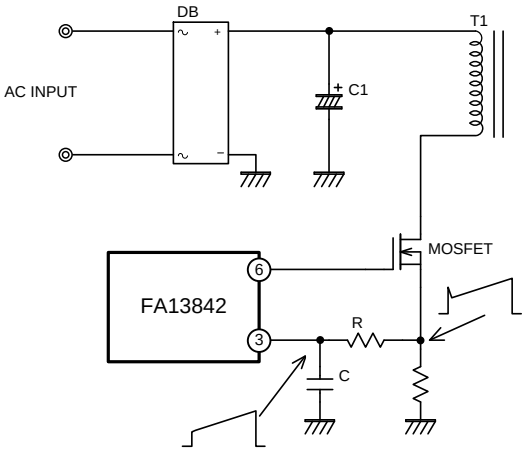


Fig.16 Suppression of noise at current sense pin

(5) Suppression of noise at current sense pin

Each cycle current value is monitored in current mode control. Therefore, there is a possibility where malfunction occurs even with relatively small noise. It is necessary to add a CR filter to reduce noise at the current sense pin. (See Fig. 16)

(6) ON/OFF circuit with an external signal

A typical ON/OFF circuit is shown in Fig. 17.

Output stage (OUT pin) is enabled when the voltage at FB pin is reduced to under 2.0V , and Output stage (OUT pin) is disabled when it rises over 3V .

Set the voltage of FB pin at 5.3V at maximum in this case.

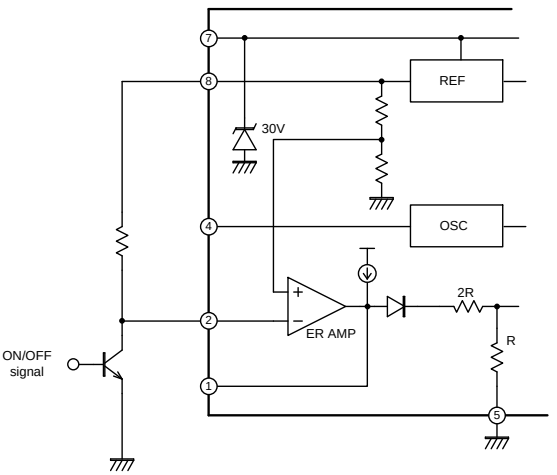


Fig.17 ON/OFF circuit

(7) Feedback circuit

①The method not using an internal ER AMP

The method not using an internal ER AMP is shown in Fig. 18. Connect FB pin to GND and connect a optocoupler to COMP pin of ER AMP output, for feedback control.

It is possible to obtain precise output voltage of power supply ,because the output voltage is monitored directly on secondary side .

Be sure to connect FB pin to GND in this case.

There is a possibility that malfunction occurs if FB pin is opened.

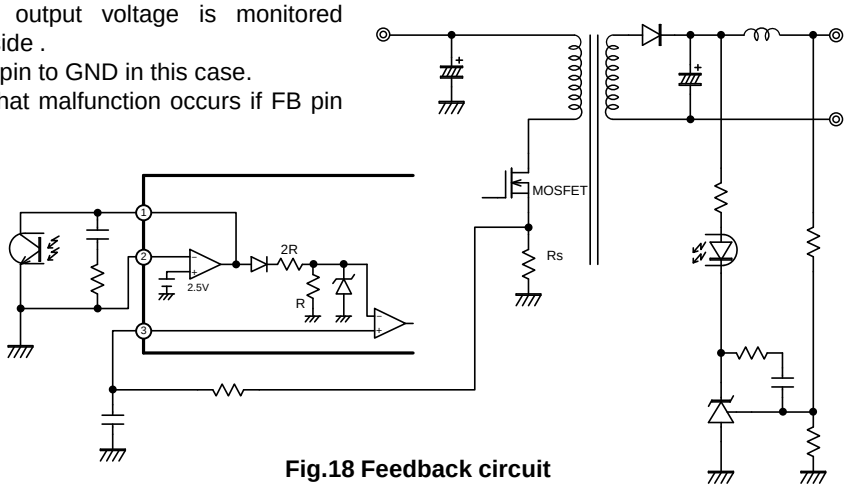


Fig.18 Feedback circuit
(The method not using an internal ER AMP)

②The method using an internal ER AMP

The method using an internal ER AMP is shown in Fig. 19.

In the flyback circuit, the bias winding voltages of transformer is proportional to the secondary winding voltage. Therefore, Vcc is approximately proportional to the DC output voltage on secondary side.

Vcc is divided by resistor and monitored at FB pin to control the output voltage.

This feedback circuit consists of minimal external components. However the regulation of the DC output voltage is not good because the output voltage is not directly monitored

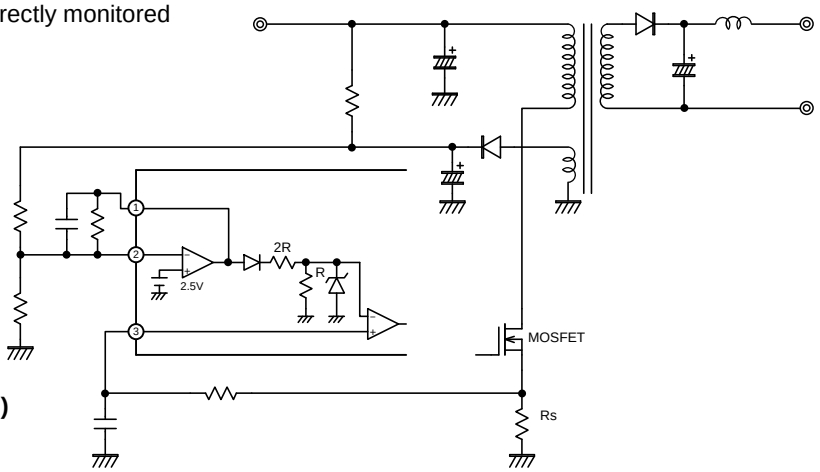


Fig.19 Feedback circuit
(The method using an internal ER AMP)

(8) Slope compensation

It is well known that a current mode converter which controls peak current can oscillate irregularly when inductor current is continuous and a duty cycle is over 50%.This irregular oscillation is called subharmonic oscillation.

The period of subharmonic oscillation is equal to integral number of switching period. This phenomenon is shown in Fig.20. Lu shows the positive slope of the inductor current and the slope is determined by the input voltage and the primary inductance value of the transformer. -Ld shows the negative slope of the inductor current and the slope is determined by the rate of energy discharge to the secondary side.

Fig. 20 indicates inductor current waveform in the case where T shows the oscillation period and Is shows the control signal of peak inductor current. TON and TOFF are varied even with the same T, Is, Lu and -Ld.

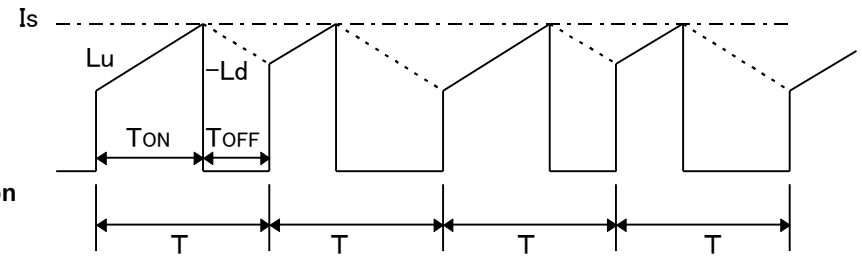


Fig.20 Subharmonic oscillation

If it is assumed in Fig.21 that the inductor current varies ΔiL at t0, the variation ΔiL' of inductor current at t1 is larger than ΔiL at t0. Thereafter, this inductor current variation is gradually increases. As a result , subharmonic oscillation occurs.

Fig.22 indicates a case when the inductor current variation ΔiL' at t1 is smaller than ΔiL at t0.

In this case,this inductor current variation is gradually converged and the inductor current will be stable.

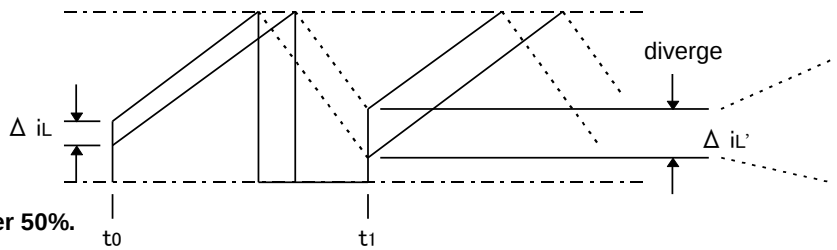


Fig.21 Operation when the duty cycle is over 50%.

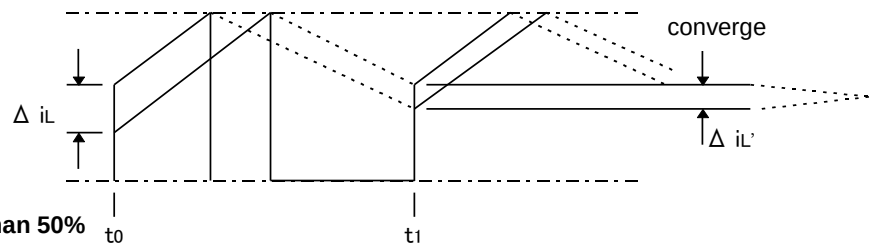


Fig.22 Operation when duty cycle is less than 50%

It is necessary to apply slope compensation to control signal in order to prevent from such subharmonic oscillation when the inductor current is continuous and the duty cycle is over 50%.

The waveform of inductor current when slope compensation is applied is shown in Fig.23 .
Slope compensation is adding negative slope of inclination -Kc to the control signal of inductor peak current.

ΔiL ' shows the variation of inductor current at t1 when slope compensation is not applied, and ΔiL 's shows the variation of inductor current at t1 when slope compensation is applied.

Thus, ΔiL ' can be changed by -Kc, and ΔIL's becomes smaller when
-Kc is large. It is necessary to apply slope compensation so that the equation ofΔiL ≧ΔiL's is satisfied to achieve stable operation, that is, the equation of -Kc≧-1/2Ld should be satisfied.

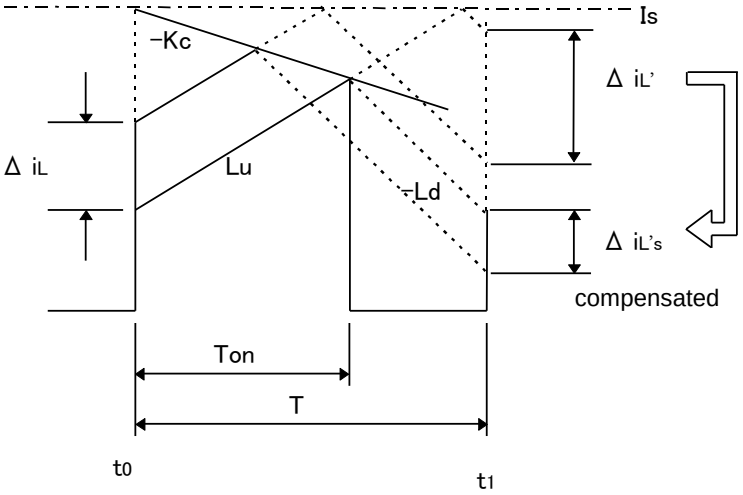


Fig.23 Slope compensation

Typical circuits are shown in Fig. 24 and 25.

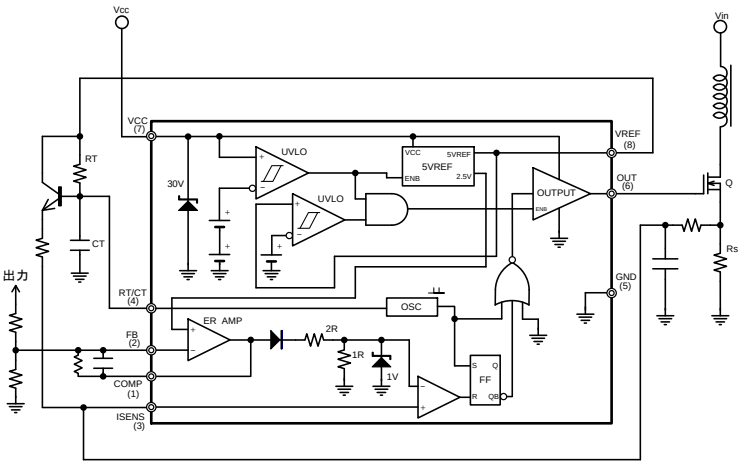


Fig.24 Slope compensation circuit(1)

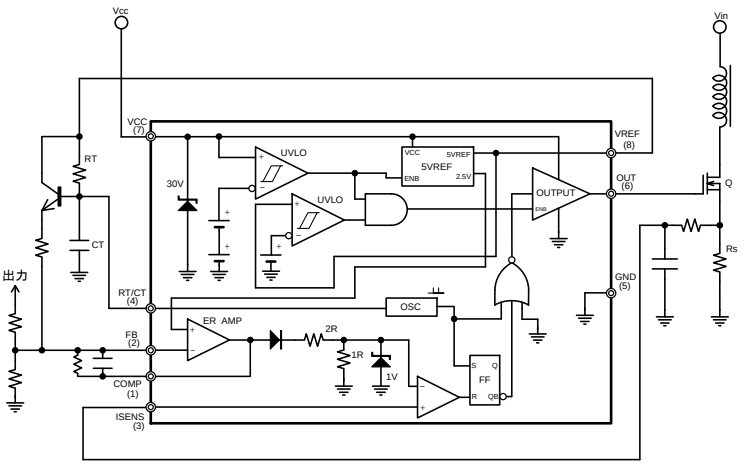
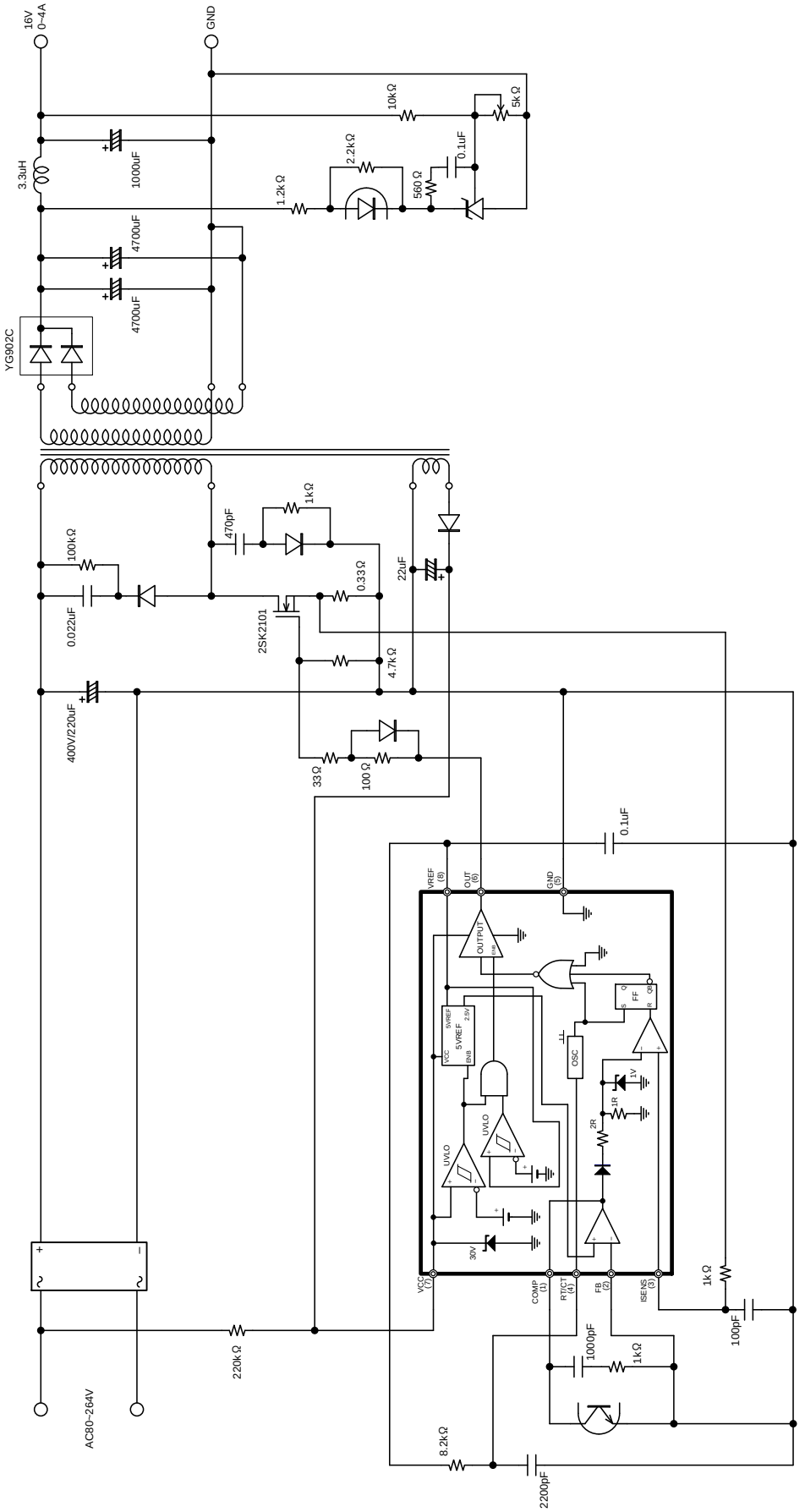


Fig.25 Slope compensation circuit(2)

11. Application circuit



Note) This application circuit is a reference material for describing typical usage of this IC, and does not guarantee the operation or characteristics of the IC.

Notice

1. The contents of this note (Product Specification, Characteristics, Data, Materials, and Structure etc.) were prepared in July 2021.The contents will subject to change without notice due to product specification change or some other reasons. In case of using the products stated in this document, the latest product specification shall be provided and the data shall be checked.

2. The application examples in this note show the typical examples of using Fuji products and this note shall neither assure to enforce the industrial property including some other rights nor grant the license.

3. Fuji Electric Co.,Ltd. is always enhancing the product quality and reliability. However, semiconductor products may get out of order in a certain probability. Measures for ensuring safety, such as redundant design, spreading fire protection design, malfunction protection design shall be taken, so that Fuji Electric semiconductor product may not cause physical injury, property damage by fire and social damage as a result.

4. Products described in this note are manufactured and intended to be used in the following electronic devices and electric devices in which ordinary reliability is required:
   - Computer - OA equipment - Communication equipment (Pin) - Measuring equipment
   - Machine tool - Audio Visual equipment - Home appliance - Personal equipment
   - Industrial robot etc.

5. Customers who are going to use our products in the following high reliable equipment shall contact us surely and obtain our consent in advance. In case when our products are used in the following equipment, suitable measures for keeping safety such as a back-up-system for malfunction of the equipment shall be taken even if Fuji Electric semiconductor products break down:
   - Transportation equipment (in-vehicle, in-ship, railways, etc.) - Communication equipment for trunk line
   - Traffic signal equipment - Gas leak detector and gas shutoff equipment
   - Disaster prevention/Security equipment - Various equipment for the safety.

6. Products described in this note shall not be used in the following equipment that require extremely high reliability:
   - Space equipment - Aircraft equipment - Atomic energy control equipment
   - Undersea communication equipment - Medical equipment.

7. When reprinting or copying all or a part of this note, our company's acceptance in writing shall be obtained.

8. If obscure parts are found in the contents of this note, contact Fuji Electric Co.,Ltd. or a sales agent before using our products. Fuji Electric Co.,Ltd. and its sales agents shall not be liable for any damage that is caused by a customer who does not follow the instructions in this cautionary statement.

- The contents will subject to change without notice due to product specification change etc.
- Application examples and component in this sheet is for the purpose of assisting in the design. Therefore, This sheet has not been made in consideration of the margin.
- Before using, Please design in consideration of the parts variation and use condition.